A 0.18 μm CMOS fluorescent detector system for bio-sensing application*

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Abstract: A CMOS fluorescent detector system for biological experiment is presented. This system integrates a CMOS compatible photodiode, a capacitive trans-impedance amplifier (CTIA), and a 12 bit pipelined analog-to-digital converter (ADC), and is implemented in a 0.18 μm standard CMOS process. Some special techniques, such as a "contact imaging" detecting method, pseudo-differential architecture, dummy photodiodes, and a T-type reset switch, are adopted to achieve low-level sensing application. Experiment results show that the Nwell/Psub photodiode with CTIA pixel achieves a sensitivity of 0.1 A/W at 515 nm and a dark current of 300 fA with 300 mV reverse biased voltage. The maximum differential and integral nonlinearity of the designed ADC are 0.8 LSB and 3 LSB, respectively. With an integrating time of 50 ms, this system is sensitive to the fluorescence emitted by the fluorescein solution with concentration as low as 20 ng/mL and can generate 7 fA photocurrent. This chip occupies 3 mm^2 and consumes 37 mW.

Key words: fluorescence detecting; contact imaging; pipelined ADC; CTIA pixel; dark current
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1. Introduction

The widespread use of DNA sequencing, immunoassays and gene expression analysis systems requires the development of portable, low cost, low power micro-array testing instruments[1,2]. One of the most popular methods for these detections is using fluorescent tags to label samples. The differences between excitation and emission spectra reveal various characteristics in the tagged samples. Usually, cooled charge coupled device (CCD) detectors or photomultipliers (PMT) are used to collect emission fluorescence of tagged samples[3,4], but they need ultra high voltage, additional instruments and optical paths, so they are not suitable for system-on-chip (SoC) application. CMOS image sensors, although having lower sensitivity and higher dark current than CCD and PMT, can be easily integrated with other functional blocks. This application-specific nature makes them especially suitable for lab-on-chip (LoC) application.

In this paper, we design and fabricate a high performance, low power CMOS fluorescent detector system for bio-sensing application. The chip integrates a CMOS process compatible photodiode, a low noise interface circuit, and a high resolution ADC and is implemented in a 0.18 μm CMOS standard process. The measured results are also illustrated.

2. System structure

In conventional imaging systems, the images of the object are captured through a series of optical elements, such as lenses, optical filters, and image sensors. The intermediary optical elements required to achieve the desired resolution in conventional imaging systems usually constrain the size, weight and cost of such systems and therefore limit their use in low-cost, high-portability, low-light detecting application. One simple method to avoid the use of these additional optical elements and paths is putting the object onto the image sensors directly, called "contact imaging". Contact imaging offers significant advantages in collection efficiency over conventional imaging. First, because of the very short distance between objects and the sensor surface, light loss in the optical path using the contact imaging method can be effectively avoided. Second, the additional optical elements themselves attenuate the optical signal seriously, so the contact imaging without these elements provides higher collection efficiency.

A CMOS fluorescent detector system chip is designed to detect the generated fluorescence, as shown in Fig.1. The Nwell/Psub photodiode is employed to convert photon to photocurrent. A capacitive trans-impedance amplifier (CTIA) is utilized to realize current-to-voltage conversion and a pipelined ADC trading off accuracy, speed and area is used for converting the optical-electronic signals into digital signals. In order to achieve high detecting sensitivity, some special techniques are used in this design:

(1) Pseudo-differential architecture is used to reduce common-mode disturbance;

(2) A dummy photodiode is used to minimize the influence of system dark current;

(3) Low reverse biased voltage for the photodiode to get low dark current performance;

(4) Using a T-type switch to avoid "off" state leakage current.

The details of the proposed detector system will be discussed later.

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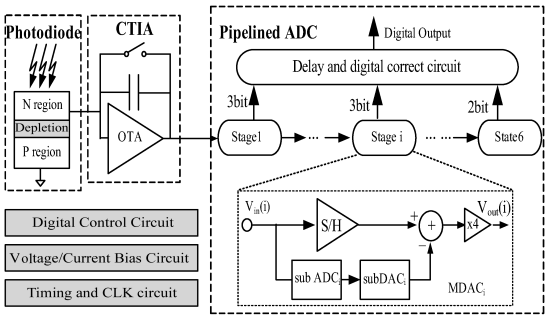

Fig.1. Block diagram of the proposed detector system.

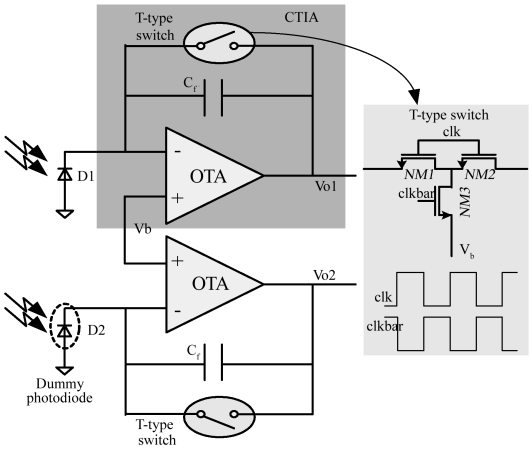

Fig.2. Pseudo-differential pixel.

3. Circuit implementations

3.1. Pseudo-differential pixel

A pseudo-differential pixel is used to achieve higher photon-electron conversion gain, lower dark current influence and some immunity to common-mode disturbances, as shown in Fig.2. The pseudo-differential pixel comprises two photodiodes and two CTIA interface circuits. The output voltage from the pseudo-differential pixel is transferred to a full-differential ADC to generate digital outputs. In Fig.2, photodiode D1 is used to realize the photon to electron conversion during the integrating period, and V_{o1} is the output voltage generated by the photocurrent and dark current. While V_{o2} is the output voltage generated only by the dark current of the photodiode D2 that is covered by various metal layers. Therefore, the output voltage of the pseudo-differential pixel can be given as

$$V_{o1} - V_{o2} = \frac{I_{pho\_D1} + I_{dark\_D1} - I_{dark\_D2}}{C_f} t_{int} , \qquad (1)$$

where I_{pho_D1} and I_{dark_D1} are the photocurrent and dark current of D1, I_{dark_D2} is the dark current of D2, C_f is the integrating capacitance, and t_{int} is the integrating time. So, the dark current influences of D1 and D2 have been partly neutralized at the output of the pixel. On the other hand, for single-ended architecture, the output voltage, V_{o1}, is easily affected by the non-ideal factor due to the schematic design and the layout, such as charge injection of the reset switch, noise from the supply voltage and ground, and disturbance and coupling from the layout. The additional CTIA makes these non-ideal factors have the same influence on V_{o1} and V_{o2}, simultaneously, so the differential voltage from the pseudo-differential pixel is much more "clean" than the output voltage from the single-ended architecture.

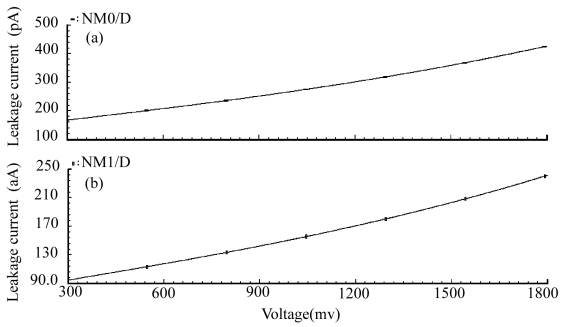

Fig.3. Leakage current of (a) NMOS switch and (b) T-type switch with different drain/source voltages.

The CTIA is used to realize photocurrent to voltage conversion, as shown in Fig.2. Compared to other interface circuits[5], this architecture has two main advantages. First, the separation of the integrating capacitor and sensing capacitor makes the CTIA pixel have higher conversion gain and larger sensing area simultaneously, which enhances the weak-light detecting ability. Second, the CTIA pixel is easy to supply a low reverse biased voltage for photodiodes, which helps the photodiodes to get a better dark current performance[6]. A T-type reset switch is used to reduce the leakage current effect during "off" state. For example, take an nMOS reset switch, although the gate/source voltage is zero, the drain/source current is not zero because of the sub-threshold current during its "off" state, which is given by[7]

$$I_{DS} \approx I_{DO} \frac{W}{L} e^{V_{GS}/nV_T} (1 - e^{-V_{DS}/V_T}) , \qquad (2)$$

where I_{DS} is the drain/source sub-threshold leakage current, I_{DO} is the saturation current, $V_{GS}(V_{DS})$ is the gate/source (drain/source) voltage, W is the switch width, L is the switch length, and n is a process dependent parameter. With a large drain/source voltage, the leakage current can be over a few hundreds pico-amperes which is much larger than the photocurrent generated by fluorescence. Therefore, normal operation of the integrator could not be established for a small fluorescent signal with an nMOS reset switch. The T-type reset switch (as shown in Fig.2) employs two additional nMOS switches, NM2 and NM3, to make the drain/source voltage of NM1 near zero during the "off" state. Figure 3 shows the leakage current simulations of the nMOS switch and T-type switch with different drain/source voltages. Both switches have a width of 5 μm and a length of 0.18 μm. We can see that the leakage current of the nMOS switch varies a few hundreds pico-amperes, nevertheless, the leakage current of the T-type switch can be below 1 fA.

3.2. Analog digital converter

We use a 12 bit 10 MSample/s pipelined ADC to digitize the pseudo-differential outputs from the pixel. In a conventional pipelined architecture, a dedicated S/H stage is always

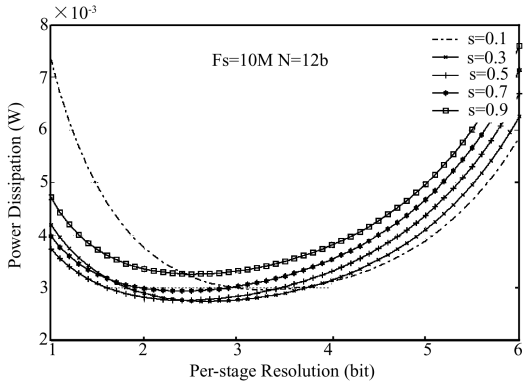

Fig. 4. Relationship between per-stage resolution and power

used to sample the input signal and provides a stable voltage for the next stage. However, the S/H stage not only consumes a large portion of overall power consumption to drive the next stage to a required accuracy but also adds noise and distortion to the input signal. Therefore, in this design, we eliminate the S/H stage to further reduce power consumption and the chip area. The aperture error due to the absence of the S/H stage can be avoided by careful schematic and layout design.

The per-stage resolution, n, is one of the most important design parameters in a pipelined ADC. A low per-stage resolution results in more stages and OTAs that consume a lot of static power and chip area. The low inter-stage gain because of the low per-stage resolution also requires a larger capacitance to satisfy the noise demand, and therefore more current and chip area must be consumed. On the contrary, although the high per-stage resolution reduces the stage number and relaxes the capacitor requirement of each stage, the per-stage power increases exponentially due to the reduction of the feedback factor of the residue amplifier. The optimized per-stage resolution can be obtained by minimizing the static power in the ADC. The OTA in each stage should have an adequate bandwidth to guarantee that the output voltage of the stage settles within the specified error in the period available. Therefore, the OTAs consume most of the static power in the ADC. Generally, the stage circuit during the hold phase can be treated as a single pole closed loop system. Therefore, in each stage, in order to achieve an M-bit settling accuracy, the bandwidth of the closed loop system must at least be:

$$\omega_{\text{close}} = \ln(2^M)\frac{F_{\text{s}}}{\delta}\,, \tag{3}$$

where F_{s} is the sampling frequency, δ is the duty cycle of the sampling period, and M is the conversion accuracy for the following stages. Meanwhile, the bandwidth of the closed loop system can also be expressed as

$$\omega_{\text{close}} = \beta\frac{g_{\text{m}}}{C_{\text{L}}} = \beta\frac{2I_{\text{B}}}{V_{\text{dsat}}C_{\text{L}}}\,, \tag{4}$$

where I_{B} is the biased current of the OTA in stage, C_{L} is the load capacitances at the output of stage, β is the feedback factor, and V_{dsat} is the overdrive voltage. The biased current of the OTA in each stage is at least:

$$I_{\text{B}} = \frac{1}{2\beta}V_{\text{dsat}}C_{\text{L}}\ln(2^M)\frac{F_{\text{s}}}{\delta}\,. \tag{5}$$

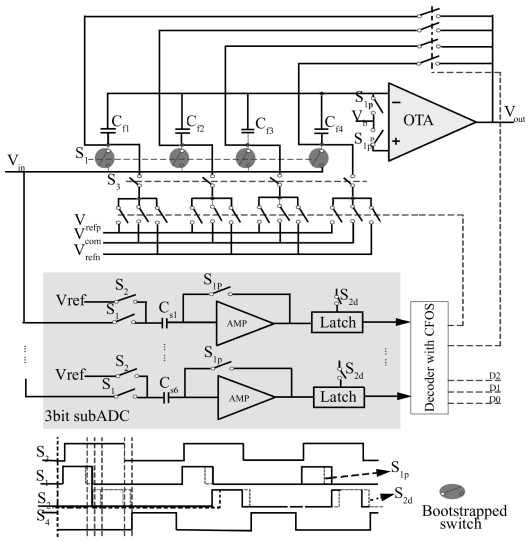

Fig.5. Front-end stage of the proposed ADC

The load capacitor, C_{L}, in each stage mainly comprises of the sampling capacitors of the local and following stages. The sampling capacitors should be carefully chosen to guarantee that the equivalent input noise from each stage is below the quantization noise of the ADC [8,9], thus, the effective bits of resolution of the ADC will be not affected by the noise from each stage. Finally, the total power dissipation of the OTAs can be expressed as

$$P_{\text{OTA}} = V_{\text{DD}}\sum_{i=1}^{P} I_{\text{B}i}\,, \tag{6}$$

where P is the number of stages. For a 12 bit, 10 MS/s pipelined ADC without the S/H stage, the relationship between per-stage resolution and power with different scaling factor[9], s, is shown in Fig.4.

Figure 4 shows that the power dissipation with $n = 2$ or $n = 3$ is much lower than other per-stage resolutions. However, as the per-stage resolution increases, the input parasitic capacitor of the SubADC increases exponentially and the digital correction voltage range decreases exponentially too. More power dissipation will be consumed to solve these problems. Therefore, we use a per-stage resolution of two in this design. The front-end stage of the proposed ADC is shown in Fig.5. The 2.5 bit MDAC uses a fully differential cascode amplifier with additional gain-boosting stages to get high DC gain, low power and excellent stability. The 3 bit flash ADC that comprises sin comparators generates thermometer digital codes for the MDAC. The amplifier in each comparator attenuates the offset voltage influence and kickback noise from latches. The CFCS technique is used to reduce the capacitors mismatch requirement in the MDAC[10]. Figure 5 also shows the detailed timing diagrams of the front-end stage.

4. Measurement results and discussion

The proposed CMOS detector system for fluorescent biosensing application was implemented in a 0.18 μm standard CMOS process. The die photograph is shown in Fig.6. This chip occupies 3 mm^2 and consumes 37 mW.

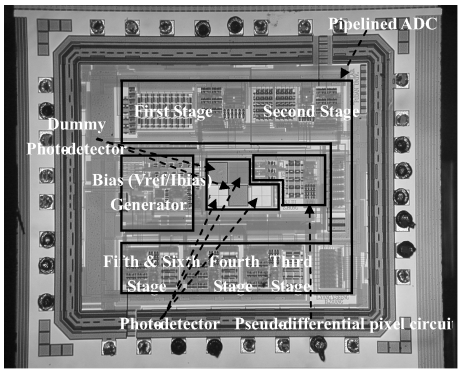

Fig.6. Die photograph of the detecting chip.

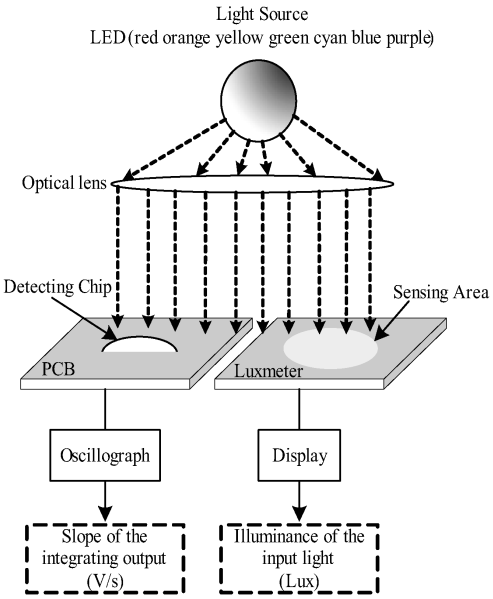

Fig.7. Testing method of the spectrum characteristic.

The sensitivity of a photodiode is defined as the ratio of generated photocurrent to light intensity, and the sensitivities with different light wavelengths are considered as the spectrum characteristic of the photodiode. The method to get the spectrum characteristic of photodiodes is shown in Fig.7. Input light with different wavelengths are irradiated onto the surface of the detecting chip and a luxmeter (TES-1332A in this experiment) through an optical lens. The slope of the integrating voltage ($\Delta V_o/\Delta t$) can be gotten from the oscilloscope, so the photocurrent within the photodiode can be obtained by

$$I_{pho} = C_f \frac{\Delta V_o}{\Delta t}, \tag{7}$$

where C_f is the integrating capacitance. On the other hand, the luxmeter helps to get the light illuminance on the surface of the detecting chip. The relationship between illuminance and intensity of the input light can be expressed as[11]

$$P_{in} = \frac{\psi S}{683 V(\lambda)}, \tag{8}$$

where ψ is the light illuminance, S is the active area of the detecting chip, and $V(\lambda)$ is an optical constant[11]. The sensitivity of the photodiode can be calculated according to Eqs.(7) and (8). In our experiment, an Nwell/Psub photodiode with an active area of $100 \times 100\ \mu m^2$ is used because of its higher

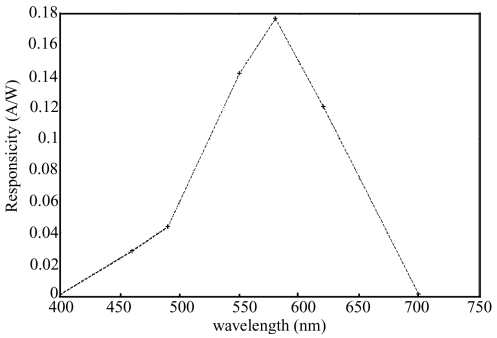

Fig.8. Spectrum characteristic of the Nwell/Psub photodiode.

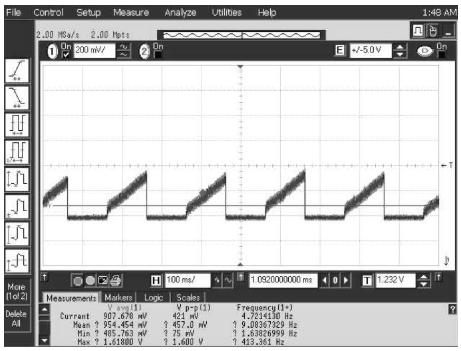

Fig.9. Transient dark current integrating output of the Nwell/Psub photodiode.

sensitivity and lower dark current than the other two CMOS compatible photodiodes (N+/Psub photodiode and P+/Nwell photodiode)[12]. Figure 8 shows the spectrum characteristic of the proposed photodiode. Seven commercially available LEDs with different colors are used as the light source. From Fig.8, we can see that the Nwell/Psub photodiode has a sensitive wavelength range from 400 to 700 nm and has its maximum sensitivity (about 0.175 A/W) at the wavelength of 580 nm. The dark current is also derived by making the photodiode work under a dark environment for a long time. Figure 9 shows the transient dark current integrating output of the Nwell/Psub photodiode. With an integrating of 100 ms time and an integrating capacitance of 100 fF, the Nwell/Psub photodiode with CTIA achieves a dark current of 300 fA with 300 mV reverse biased voltage.

The static performances of the pipelined ADC, such as DNL and INL, are also measured and shown in Fig.10. With 10 MHz sampling frequency and 4 million samples, the designed ADC has a maximal DNL of 0.8 LSB and INL of −3 LSB. These results show that the designed ADC is monotone and achieves an effective conversion accuracy of above 10 bit.

The proposed chip is used in a fluorescent detecting experiment, as shown in Fig.11. The fluorescence is generated by a commercially available fluorescein, which has an excitation wavelength of 468 nm and an emission wavelength of 515 nm. A blue LED is used as the light source to excite the fluorescein. The generated fluorescence is close to green light, as shown in Fig.11. A band-pass optical filter with a center wavelength of 468 nm is used next to the LED to filter out other wavelength light. The filtered exciting light penetrates into the fluorescein solution, and then the exciting light and the fluorescence go

Table 1. Parameter summary and comparisons.

	This work	Ref.[13]	Ref.[14]	Ref.[15]
Proces	0.18 μm	5 μm	0.5 μm	0.25 μm
Photo-detector type	Nwell/Psub PD	Photogate	N/A	N/A
Sensing area	100×100 μm^2	300×300 μm^2	500×500 μm^2	10×10 μm^2
Dark current	300 fA(3nA/cm^2)	>1 pA	80 pA/cm^2	N/A
Minimum detectable fluorescent intensity	3.5 nW/cm^2	30 nW/cm^2	5 nW/cm^2	N/A
Minimum detectable solution	20 ng/mL (60 nM)	10 μm	N/A	100 μm

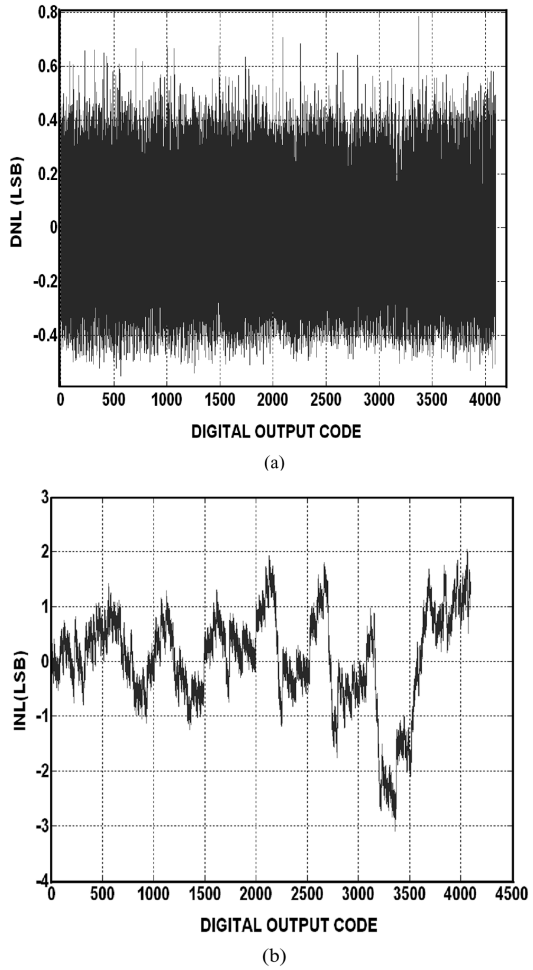

Fig.10. Static characteristic of the proposed ADC: (a) DNL; (b) INL.

through another band-pass optical filter with a center wavelength of 515 nm placed above the sensing area of the chip directly. The second filter helps to select the generated green fluorescence into the chip and attenuate the exciting light. The output of this experiment is the digital codes from the pipelined ADC. We use an integrating time of 50 ms in this experiment. About 2^{12} codes are collected to average the noise from the integrated circuit and environment for each fluorescein solution concentration. Figure 12 shows the relationship between the fluorescein solution concentration and the normalized digital output from the designed ADC. The measured results show that, with 2 mL solution volume, the detector system is able to detect the fluorescein solution concentration as low as 20 ng/mL. The minimum detectable fluorescent intensity and photocurrent are 3.5 nW/cm^2 and 7 fA, respectively. Other parameters of the detector system and the comparisons with other references are summarized in Table 1.

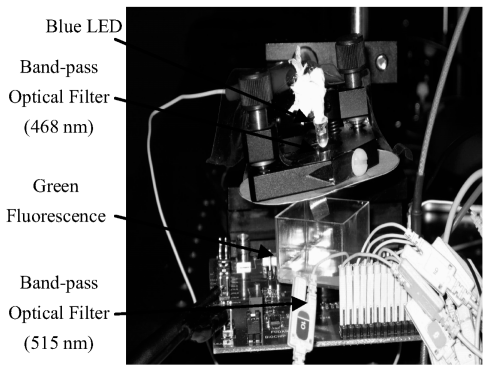

Fig.11. Fluorescence detecting experiment photograph.

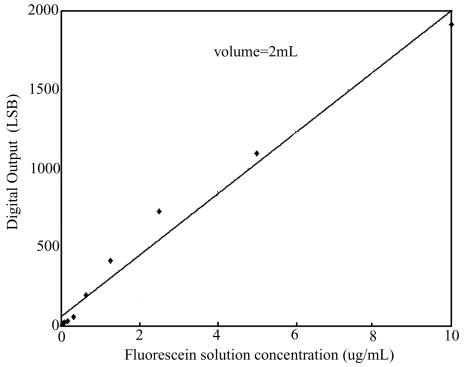

Fig.12. Relationship between digital outputs and solution concentration.

5. Conclusion

In this paper, we presented a CMOS detector system to detect a fluorescence signal. Special techniques, such as a "contact imaging" detecting method, pseudo-differential architecture, dummy photodiodes and a T-type reset switch, were used to achieve low-level sensing application. Experiment results show that, with 50 ms integrating time, this chip is sensitive to the fluorescence emitted by the fluorescein solution with concentration as low as 20 ng/mL and can generate a photocurrent of 7 fA. With the helps of optical paths, tagged samples and DSP, a lab-on-chip (LoC) system can be established for biological test application with less testing time, labor and cost.

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