Design and measurement of a 53 GHz balanced Colpitts oscillator

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Abstract: A 53 GHz Colpitts oscillator implemented in a SiGe:C BiCMOS technology is presented. Limited by a 26.5 GHz frequency analyzer, the oscillator was measured indirectly through an on-chip mixer. The mixer down-converted the oscillating frequency to an intermediate frequency (IF) below 26.5 GHz. By adjusting the local oscillating (LO) frequency and recording the changes of IF frequency, the oscillator's output frequency (RF) was determined. Additionally, using phase noise theory of mixers, the oscillator's phase noise was estimated as −58 dBc/Hz at 1 MHz offset and the output power was about –21 dBm. The chip is 270×480 μm in size.

Key words: Colpitts; negative resistance; oscillator; phase noise
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1. Introduction

The rapid development of the information technology industry has over the past decade inspired a massive amount of research on balanced voltage controlled oscillators (VCO). As the topology of analog and RF circuits has shifted from single-ended to differential in modern communication systems, the evolution of oscillators or VCO from single-ended to the balanced structure has also taken place, leading to better noise rejection and stable performance. In the RF frequency band, balanced VCOs in CMOS technologies have recently been reported in mainland China[1−4]. In the higher frequency band, a single-end Ka-band VCO was demonstrated in GaAs PHEMT[5], and a 36 GHz balanced VCO was also fabricated in GaAs technology[6]. Although GaAs is the most popular technology to fabricate oscillator circuits due to its high performance at high frequencies, its high cost and low yield rate impact on its wider application. In the millimeter wave frequency band, SiGe-based technologies are promising for the fabrication of high performance, low cost devices because of their excellent high-frequency response. However, there is little research on SiGe-based millimeter wave oscillators with balanced structures being carried out in mainland China. The aim of this paper is to demonstrate a balanced 53 GHz oscillator in a SiGe-based technology for application in the clock-recovery circuit of next-generation optical communication systems, and to propose a method of millimeter wave frequency measurement with limited equipment. This new topology is modified from a traditional Colpitts oscillator by inserting two emitter followers and two compensation inductors. The oscillator was fabricated with IHP 0.25 μm SiGe:C BiCMOS, which provides four metal layers with a 2 μm-thick top metal. The average cutoff frequency is 180 GHz.

2. Analysis

The circuit diagram of a conventional differential Colpitts oscillator is shown in Fig.1 (a). A differential emitter capacitively coupled current logic (DEC^{3}L) is formed by the transistors Q1 and Q2, and the capacitors C_c and $C_{c'}$, which generates negative resistance to compensate the loss of resonating inductors L and L'. This topology is widely used at millimeter wave frequencies, but its negative resistance is still weak in the high-frequency band. To overcome this disadvantage, a novel topology, shown in Fig.1 (b), has been proposed[7]. Two emitter followers were inserted between the bases of the DEC^{3}L and the circuit of the resonating inductors, L and L'. For the simulation, a VBIC-model of the bipolar transistor is used. The comparison of two topologies' negative resistance is shown in Fig.1 (c). This figure indicates that the proposed topology exhibits stronger negative resistance in the high-frequency band than the conventional topology, and weaker negative resistance at low frequencies. Therefore, the proposed topology is more suitable for high-frequency application than the conventional one. Compared with the traditional topology, the only disadvantage is the greater power consumption by the two emitter followers, Q3 and Q4, but this extra power is all used to increase performance in the high-frequency band.

3. Circuit design

3.1. Oscillator

The circuit diagram of our newly designed oscillator is depicted in Fig.2. Two emitter followers, Q3 and Q4, are used to improve the poor performance of the DEC^{3}L in the higher-frequency band. All the transistors are biased by nMOS current sources. Since the output impedance (Z_{DS}) of the nMOS transistor is not infinite, the two emitter followers impact severely on the negative resistance when the circuit operates at millimeter wave frequencies. Therefore, we introduced two symmetrical inductors L_1 and L_2 to compensate the capacitive reactance of Z_{DS}, which effectively improves the output impedance of the nMOS current sources. To obtain a higher quality factor, the resonating inductors, L_{T1} and L_{T2}, are

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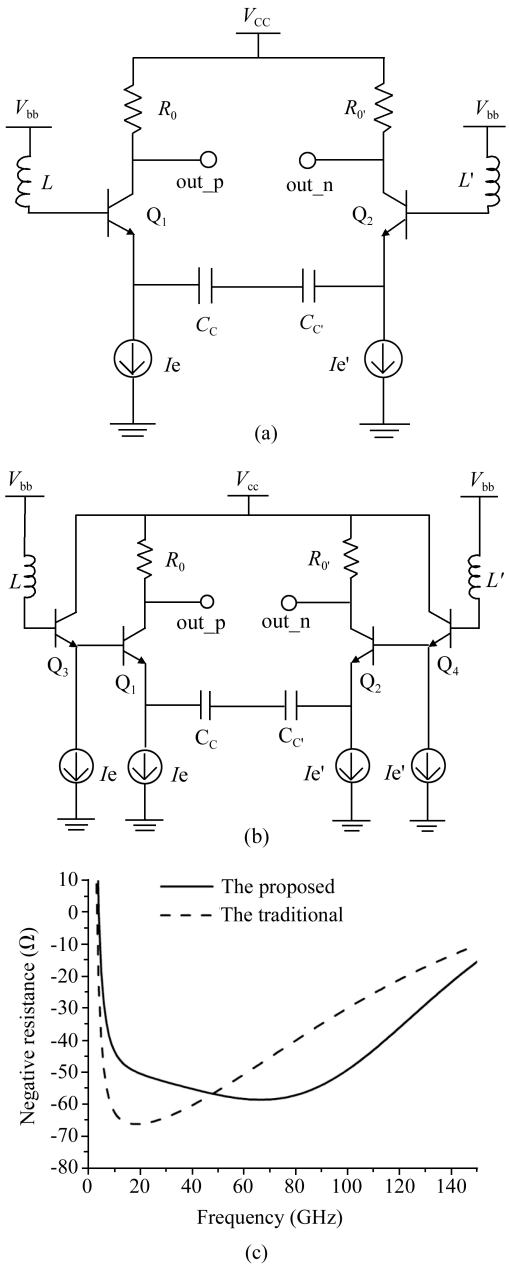


Fig.1. (a) Topology of the traditional Colpitts oscillator; (b) Topology of the proposed oscillator; (c) Comparison of negative resistance.

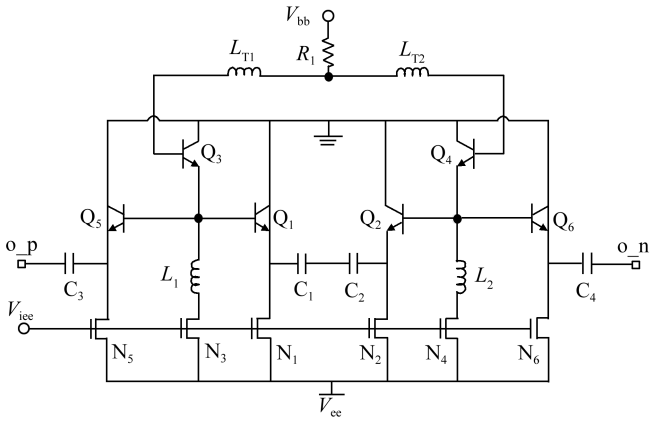


Fig.2. Circuit diagram of the oscillator core.

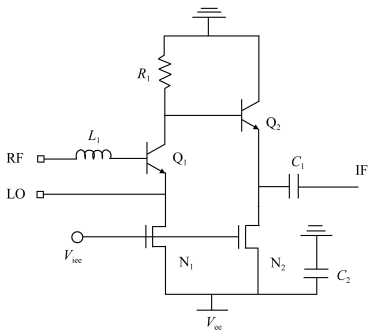


Fig.3. Circuit diagram of the mixer.

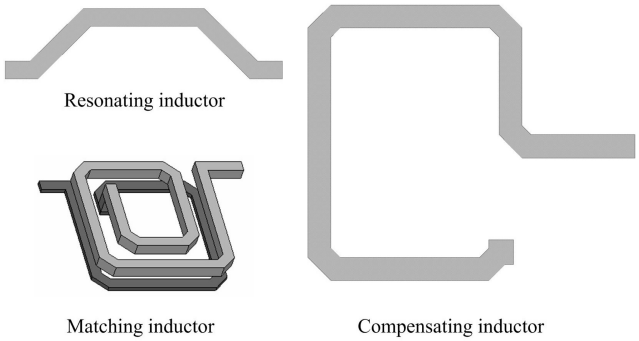


Fig.4. Inductors in the design.

combined to form a center-tapped differential inductor. The output emitter followers, Q5 and Q6, are designed with a small emitter area to exhibit large input impedance, improving the isolation from the loads to the oscillator core. In operation, the oscillator works in the odd mode, such that the oscillations are 180 ° out of phase. Operation in the even mode is not possible because of the high impedance at node V_{bb} (R_1 = 500 Ω).

3.2. Mixer

In order to directly measure the oscillator by means of a 26.5 GHz spectrum analyzer, we inserted a mixer after the outputs of the oscillator to down-convert the oscillating frequency to IF. The mixer uses two stages of HBT transistors as shown in Fig.3. The oscillating frequency (RF) is applied to the base of Q1, and the LO signal is injected into the emitter, increasing the RF–LO isolation. A spiral inductor (L_1) is placed between the oscillator and the mixer for impedance matching. Q2 drives the mixed products to the output pad. The LO signal is even mode for the mixer, which unavoidably produces an interfering signal fluctuating in the power supply and ground, so a capacitor (C_2) is necessary to shunt the even-mode interfering signal from V_{ee} to ground. The size of C_2 used here is determined by its SRF, at which the impedance of C_2 exhibits "zero" at the LO frequency[8].

3.3. Inductors

In total, three types of inductors are integrated into the design, including a resonating inductor, two compensating inductors, and two matching inductors, as shown in Fig.4. Both 2.5-dimensional and 3-dimensional EM field simulators were used to properly estimate both the inductance and Q-factor. Theoretically, an inductor of a transmission-line type, either a microstrip or a coplanar waveguide, cannot be adapted for high-frequency applications because its distributed capacitance to ground reference metal dominates performance in the

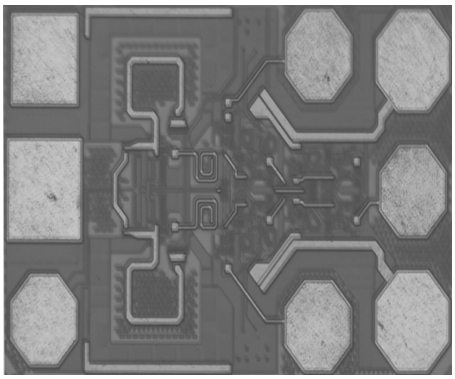


Fig.5. Micrograph of the VCO.

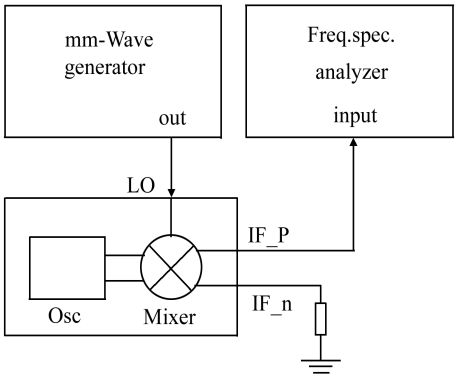
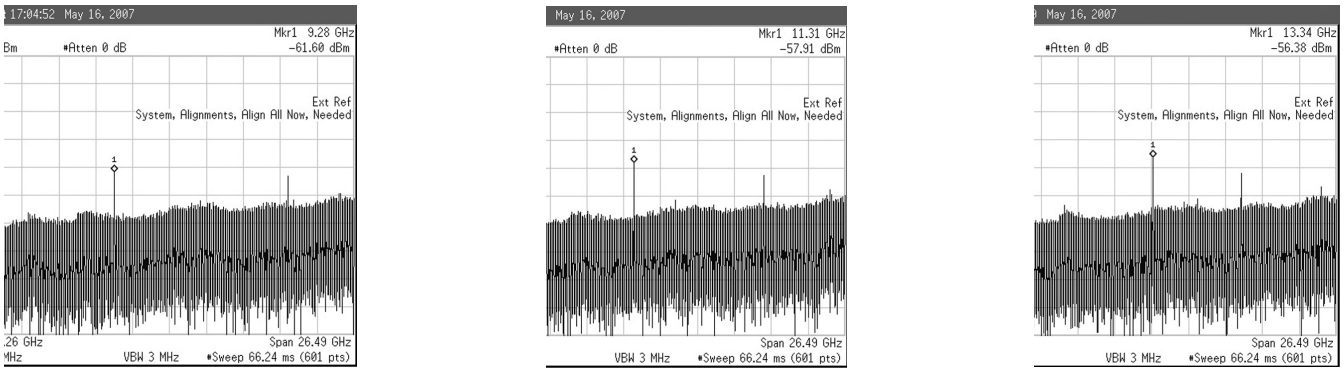


Fig.6. Measurement setup.



(a) (b) (c)

Fig.7. Measured IF spectrum with different f_{LO}: (a) f_{LO} = 31 GHz; (b) f_{LO} = 32 GHz; (c) f_{LO}= 33 GHz.

high-frequency band and makes the SRF too low. Therefore, the resonating and compensating inductors, were fabricated on the top metal with no ground-reference metal below, and placed far from any other signal metals. The matching inductors between the oscillator and the mixer, considering the chip area, were constructed as a stack giving a very compact size.

4. Implementation and measurement

Figure 5 shows a micrograph of the chip of the fabricated oscillator, whose size is only $270 \times 480\ \mu m^2$. The oscillator core, the mixer, and the bias circuits are designed symmetrically.

The oscillator was measured on-wafer using an Agilent E4440A frequency spectrum analyzer with the frequency range from 3 Hz to 26.5 GHz. An R&S SMP04 millimeter wave signal generator (from 10 MHz to 40 GHz) provided the LO signal. Figure 6 describes the measurement setup where the block on the lower left is the oscillator chip. The IF frequency can be calculated by

$$f_{IF} = \pm m f_{RF} \pm n f_{LO}, \tag{1}$$

where f_{RF}, f_{LO} and f_{IF} are the frequencies of the LO, RF (the oscillator's output signal) and IF signals, respectively. Through stepping f_{LO}, measuring the step of f_{IF}, and considering the shifting direction of f_{IF}, the sign "±" and harmonic number m and n can be determined. Thus the oscillating frequency can be accurately measured using the on-chip mixer.

As shown in Fig.7, when f_{LO} is increased from 31 to 33 GHz in 1 GHz steps, f_{IF} increases from 9.3 to 13.3 GHz in 2 GHz steps. Therefore, the sign before the term nf_{LO} in Eq.(1) has to be "+", and n = 2 because f_{IF} steps twice as fast as f_{LO} in the same direction. Thus, Equation (1) can be rewritten as

$$f_{IF} = 2f_{LO} - mf_{RF}. \tag{2}$$

Since no carrier spectrum was recorded in the full span of the frequency analyzer without the injection of the LO signal, f_{RF} must be higher than the upper limit of the equipment (26.5 GHz), which means m is 1. So the oscillating frequency is calculated as 52.7 GHz.

The phase noise of the oscillator output signal can be estimated from the phase noise of the LO signal and the IF signal using a previously published theory[9]. Let the LO signal have power P_{LO} and a phase noise power density function $p_{LO}(x)$, where x is the frequency offset from the carriers. The same parameters for the RF carrier are P_{RF} and $p_{RF}(x)$, respectively. We let the desirable output IF signal be at the lower frequency with $P_{IF} = P_{RF}/K_1$ and phase noise power density of $p_{IF}(x)$. In our application, the approximated phase noise of the IF signal is rewritten here as

$$\left[\frac{p_{IF}(x)}{P_{IF}}\right] \approx \left[\frac{p_{RF}(x)}{P_{RF}}\right] + n^2 \frac{2K_1}{K_3}\left[\frac{p_{LO}(x)}{P_{LO}}\right], \tag{3}$$

where K_1 and K_3 are defined constants and $2K_1/K_3$ approximately equals unity[9]. Thus

$$\left[\frac{p_{RF}(x)}{P_{RF}}\right] \approx \left[\frac{p_{IF}(x)}{P_{IF}}\right] - n^2\left[\frac{p_{LO}(x)}{P_{LO}}\right]. \tag{4}$$

The measured phase noise of the IF signal is –58.4 dBc/Hz at 1 MHz offset, and that of the LO signal is –115 dBc/Hz at 1 MHz offset. Converting dBc into normal scale, we have $p_{IF}(x)/P_{IF} = 1.2 \times 10^{-3}$, and $p_{LO}(x)/P_{LO} = 1.78 \times 10^{-6}$. Therefore, $p_{RF}(x)/P_{RF} \approx p_{IF}(x)/P_{IF}$ = –58.4 dBc/Hz at 1 MHz offset. The phase noise can be further decreased by employing the following methods. First, one replaces the nMOS transistors in the tail current sources with npn transistors or resistors, because the nMOS transistors contribute more $1/f$ noise to the phase noise[10]. Next, one increases the resonating inductance, L_{T1} and L_{T2}, while decreasing the emitter coupled capacitance, C_1 and C_2, to maintain the same oscillating frequency, but increase the voltage amplitude at L_{T1} and L_{T2}, thus lowering the phase noise[11]. Finally, one may place large capacitors at the bias and power nodes (V_{bb}, V_{iee}, and V_{ee}) to filter the noise from the power supply.

Considering the conversion loss of the on-chip mixer, the insertion loss of transmission line, mismatching between the mixer and the external load, and measurement coaxial line loss, the oscillator's output power is estimated as −21 dBm. The oscillator core consumes 56 mA from a −4.5 V supply.

5. Conclusion

A differential Colpitts oscillator operating at 53 GHz was demonstrated using SiGe:C BiCMOS technology. Within the limits of the equipment, a practical method was proposed to measure the oscillating frequency precisely, and the phase noise can be well estimated using the phase noise theory of mixers. Further optimization in the mixer and output matching should allow generation of signals with higher output power at lower DC supply.

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