A novel GAAC FinFET transistor: device analysis, 3D TCAD simulation, and fabrication

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Abstract: We report the analysis and TCAD results of a gate-all-around cylindrical (GAAC) FinFET with operation based on channel accumulation. The cylindrical channel of the GAAC FinFET is essentially controlled by an infinite number of gates surrounding the cylinder-shaped channel. The symmetrical nature of the field in the channel leads to improved electrical characteristics, e.g. reduced leakage current and negligible corner effects. The $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of the device can be larger than 10^6, as the key parameter for device operation. The GAAC FinFET operating in accumulation mode appears to be a good potential candidate for scaling down to sub-10 nm sizes.

Key words: accumulation mode; GAAC FinFET; device analysis; TCAD simulation; fabrication
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1. Introduction

With a continuously scaled gate length in a conventional planar CMOS transistor it is increasingly difficult to maintain high drive currents with low off-current leakage, as well as the stability of the threshold voltage. The short-channel effect is known to degrade device performance and sets a limit for further scaling down of conventional planar CMOS devices. One key development for further scaling down of CMOS transistors is the greater control of channel conductance by the gate electrode instead of influence from the fringe field from the drain electrode. For SOI devices, from partial depletion mode to full depletion mode, this is achieved by reducing the silicon body thickness. Double gate transistor[1], tri-gate transistor[2], and omega FinFET[3] are alternative device structures with greater gate control over channel area (than planar CMOS) and lead to excellent scalibility into the short channel beyond the 32 nm node. Gate-all-around (GAA) FinFET is one of the most promising structures to extend the scaling down of CMOS devices as it provides the best channel electrostatic control, which improves further with decreasing channel thickness[4,5]. However, it is still subject to the SCE effect if the device is designed to work in inversion mode, as the source/drain are doped with different dopants to the channel and are subject to leakage. In this work, for the first time, we propose a new GAAC FinFET device operating in accumulation mode for the sub-10 nm CMOS node, where the analytically calculated I–V characteristics agree well with 3D TCAD simulation.

2. Device architecture

Figure 1 illustrates a simplified perspective and cross-sectional view of a GAAC FinFET device structure. The source, drain and channel regions are doped with the same type of dopant. Thus, there is no pn junction along the channel length and the leakage current is thus reduced. Cross-sectional views parallel and perpendicular to the channel directions are shown in Fig.2. The ultimate GAAC FinFET device uses a physical oxide with a large bandgap to isolate the gate from the conducting channel area. By applying gate voltage to accumulate or deplete majority carriers in the channel, we can modulate the channel conductance for controlling the channel current as a switch between the source and drain.

3. GAAC FinFET device analysis

The current–voltage (I–V) characteristics of the GAAC FinFET are analyzed below. Consider a p-channel GAAC FinFET with the geometry shown in Fig.2. The differential resistance $\mathrm{d}R$ of the channel with differential length $\mathrm{d}z$ at a point z in the channel is[6]

$$\mathrm{d}R=\rho \mathrm{d}z/A(z)\,, \tag{1}$$

where ρ is the resistivity and $A(z)$ is the cross-sectional area. If we neglect the minority carrier electrons in the p-channel, the channel resistivity is

$$\rho = 1/(e\mu_{\mathrm{p}}N_{\mathrm{A}})\,. \tag{2}$$

The cross-sectional area is given by

$$A(z)=\pi[a-w(z)]^2\,, \tag{3}$$

where a is the radius of the cylinder channel and $w(z)$ is the depletion width at point z. Thus, the differential resistance of the channel can be expressed by

$$\mathrm{d}R = \mathrm{d}z/\left[\pi e\mu_{\mathrm{p}}N_{\mathrm{A}}(a-w)^2\right]\,. \tag{4}$$

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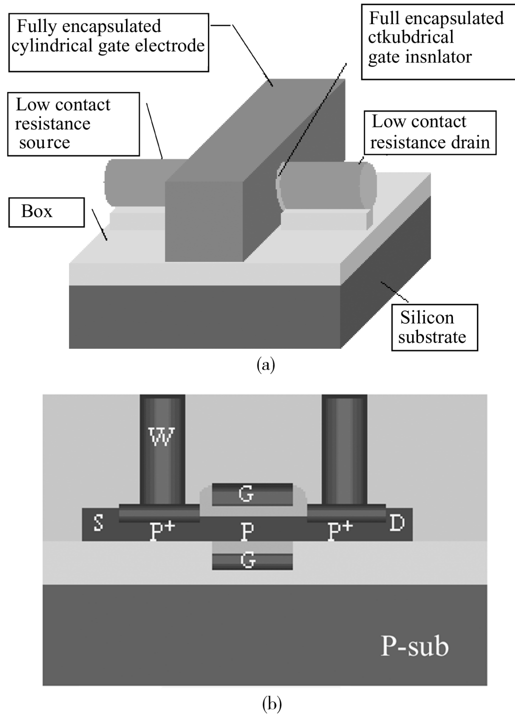

Fig.1. (a) Simplified perspective and (b) cross-sectional view of a GAAC FinFET device architecture. The source, drain and channel regions are doped with the same type of dopant (p-type in this figure).

The differential voltage across a differential length dz can be expressed as

$$\mathrm{d}V(z) = I_{\mathrm{D}}\mathrm{d}z/\left[\pi e\mu_{\mathrm{p}}N_{\mathrm{A}}(a-w)^2\right], \tag{5}$$

or

$$I_{\mathrm{D}}\mathrm{d}z = \pi e\mu_{\mathrm{p}}N_{\mathrm{A}}(a-w)^2\mathrm{d}V(z), \tag{6}$$

where the drain current I_{D} is a constant through the channel. The relationship between the potential in the channel due to the drain-to-source voltage $V(z)$ and the depletion width $w(z)$ is given by

$$V(z) + V_{\mathrm{G}} = V_{\mathrm{ox}} + \psi_{\mathrm{s}} = \frac{eN_{\mathrm{A}}wd}{\varepsilon_{\mathrm{ox}}} + \frac{eN_{\mathrm{A}}w^2}{2\varepsilon_{\mathrm{s}}}, \tag{7}$$

where V_{ox} and ψ_{s} are the potential drop in the gate oxide and the semiconductor surface, respectively. Taking the differential of Eq.(1), we have

$$\mathrm{d}V = \left(\frac{eN_{\mathrm{A}}d}{\varepsilon_{\mathrm{ox}}} + \frac{eN_{\mathrm{A}}}{\varepsilon_{\mathrm{s}}}w\right)\mathrm{d}w. \tag{8}$$

Then Equation (6) becomes

$$I_{\mathrm{D}}\mathrm{d}z = \pi e\mu_{\mathrm{p}}N_{\mathrm{A}}(a-w)^2\left(\frac{eN_{\mathrm{A}}d}{\varepsilon_{\mathrm{ox}}} + \frac{eN_{\mathrm{A}}}{\varepsilon_{\mathrm{s}}}w\right)\mathrm{d}w. \tag{9}$$

Assuming the current and the mobility are constants through the whole channel, the drain current I_{D} can be derived by integrating Eq.(3) along the channel length as below:

$$I_{\mathrm{D}} = \frac{1}{L}\int_{W_1}^{W_2}\pi e\mu_{\mathrm{p}}N_{\mathrm{A}}(a-w)^2\left(\frac{eN_{\mathrm{A}}d}{\varepsilon_{\mathrm{ox}}} + \frac{eN_{\mathrm{A}}}{\varepsilon_{\mathrm{s}}}w\right)\mathrm{d}w. \tag{10}$$

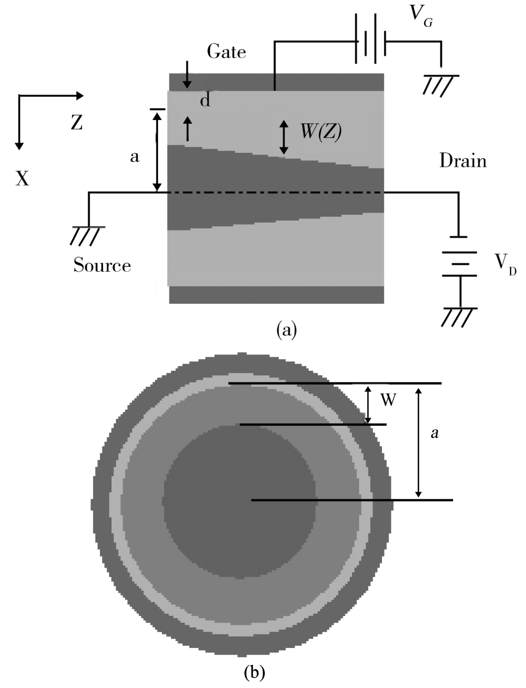

Fig.2. Cross-sectional view of the p-channel GAAC FinFET: (a) Along the channel length; (b) Perpendicular to the channel length.

Finally, we obtain

$$\begin{aligned} I_{\mathrm{D}} = \frac{\pi\mu_{\mathrm{p}}(eN_{\mathrm{A}})^2}{\varepsilon_{\mathrm{s}}L}\Big[&\frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}da^2w_2 + \\ &\left(\frac{a^2}{2} - \frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}da\right)w_2^2 + \left(\frac{\varepsilon_{\mathrm{s}}d}{3\varepsilon_{\mathrm{ox}}} - \right. \\ &\left.\frac{2a}{3}\right)w_2^3 + \frac{1}{4}w_2^4 - \frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}da^2w_1 - \left(\frac{a^2}{2} - \right. \\ &\left.\frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}da\right)w_1^2 - \left(\frac{d\varepsilon_{\mathrm{s}}}{3\varepsilon_{\mathrm{ox}}} - \frac{2a}{3}\right)w_1^3 - \frac{1}{4}w_1^4\Big], \end{aligned} \tag{11}$$

and

$$w_1 = \sqrt{\left(\frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}d\right)^2 + \frac{2\varepsilon_{\mathrm{s}}V_{\mathrm{G}}}{eN_{\mathrm{A}}}} - \frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}d,$$

$$w_2 = \sqrt{\left(\frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}d\right)^2 + \frac{2\varepsilon_{\mathrm{s}}(V_{\mathrm{G}}+V_{\mathrm{D}})}{eN_{\mathrm{A}}}} - \frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}}d,$$

where w_1 and w_2 represent the depletion width at the source and drain biased at V_{D} and V_{G} respectively. a is silicon cylinder radius, d is gate dielectric thickness, L is gate length, N_{A} is density of acceptor impurity atoms, μ_{p} is hole mobility, e is electronic charge, ε_{s} is the relative dielectric constant of silicon, and $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of silicon oxide.

The drain current becomes saturated when the drain side is pinched-off, i.e. the depletion width at the drain side equals the radius of the cylindrical channel:

$$V_{\mathrm{D}} = V_{\mathrm{Dsat}} = \frac{eN_{\mathrm{A}}ad}{\varepsilon_{\mathrm{ox}}} + \frac{eN_{\mathrm{A}}a^2}{2\varepsilon_{\mathrm{s}}} - V_{\mathrm{G}}. \tag{12}$$

The saturation drain current is independent of the drain-to-source voltage in Eq.(6). Figure 3 shows the calculated analytical curves of I_{D} versus V_{D} of a p-channel GAAC FinFET. The ideal current-voltage characteristics of I_{D} versus V_{G} for a p-channel GAAC FinFET are shown in Fig.4.

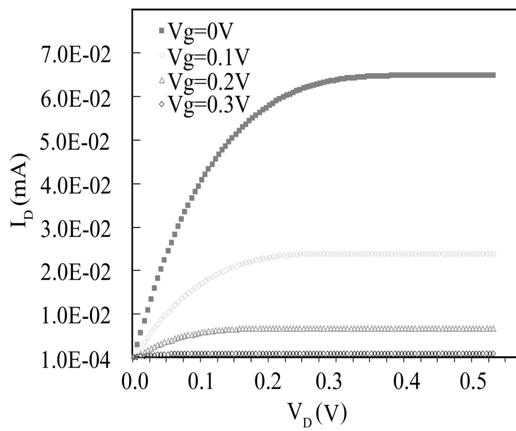

Fig.3. Calculated curves of I_D versus V_D for a p-channel GAAC FinFET with a = 5 nm, L = 10 nm, d = 1 nm and $N_A = 10^{19}$ cm^{-3}.

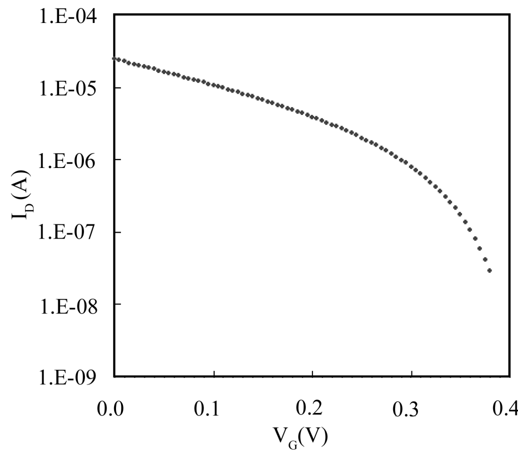

Fig.4. Calculated curves of I_D versus V_G of a p-channel GAAC FinFET with a = 5 nm, L = 10 nm, d = 1 nm, $N_A = 10^{19}$ cm^{-3} and $V_D = -50$ mV.

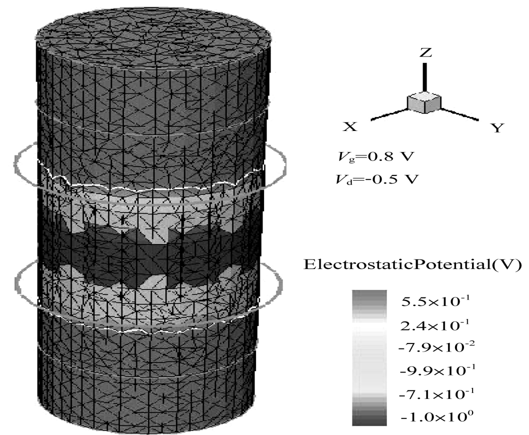

Fig.5. View of the simulated 3D GAAC FinFET structure with simulation grid of electrostatic potential distribution.

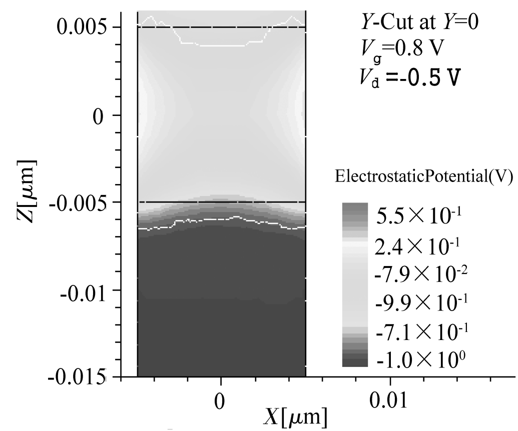

Fig.6. Cross-sectional view along Y (Y-cut at Y = 0) of simulated electrostatic potential for a fully encapsulated GAAC. V_D and V_G are biased at −0.5 and 0.8 V respectively; a = 5 nm, L = 10 nm, d = 1 nm and $N_A = 10^{19}$ cm^{-3}.

4. GAAC FinFET 3D TCAD simulation

As technologies become more complex, the semiconductor industry relies increasingly on TCAD simulation for speed and lower cost in the research and development of novel devices. Genpei *et al.* used the 3D TCAD simulation tool for DG MOSFET sub-threshold characteristic analysis[7]. In this paper, SYNOPSYS 3D FLOOPS-DEVISE and DESSIS are used in our simulation. A floating silicon body acts as the device channel, with gate dielectrics and metal gate wrapped around. Doping dependence and surface roughness mobility degradation models are switched on in our simulation. Figure 5 shows a view of the simulated 3D GAAC FinFET structure *i*th simulation grid.

Figures 6 and 7 show the simulated cross-sectional view of electrostatic potential and hole density distribution respectively of a p-channel GAAC FinFET cut along Y. The cross-sectional view of simulated hole density for a fully encapsulated GAAC FinFET cut along Z in the middle of the channel is given in Fig.8.

Figure 9 shows the simulated plot of I_D versus V_D for a p-channel GAAC FinFET. It agrees well with our theoretical calculations shown in Fig.3. The TCAD current is slightly lower than that of the theoretical calculation, which may be due to the surface scattering in our TCAD mobility model.

The simulated plot of I_D versus V_G is given in Fig.10. From the curve, we can see that this device performs well due to the uniformity of the gate dielectric and the electrical integrity around the channel. The I_{on}/I_{off} ratio is more than 10^6 which is essential for device operation. This suggests that the GAAC FinFET structure may be suitable for scaling down to sub-10 nm sizes. In short, the GAAC FinFET appears superior to conventional multi-gate FinFETs, further improving device performance and scalability. With gate-all-around cylindrical architecture, the transistor is controlled by an essentially infinite number of gates surrounding the entire cylinder-shaped channel. The electrical integrity within the channel is improved by the symmetrical field (e.g. reduced current leakage by eliminating the corner effect due to field concentration).

5. GAAC FinFET fabrication procedure

A GAAC FinFET has been developed in which the gate region surrounds the channel region completely, without leaving a gap as in previous multi-gate devices. Unlike other

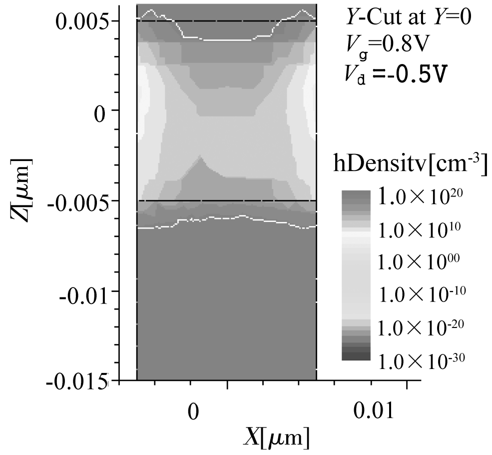

Fig.7. Cross-sectional view along Y (Y-cut at Y =0) of simulated hole density for a fully encapsulated GAAC FinFET. V_D and V_G are biased at −0.5 and 0.8 V respectively; a = 5 nm, L = 10 nm, d = 1 nm, $N_A = 10^{19}$ cm^{-3}.

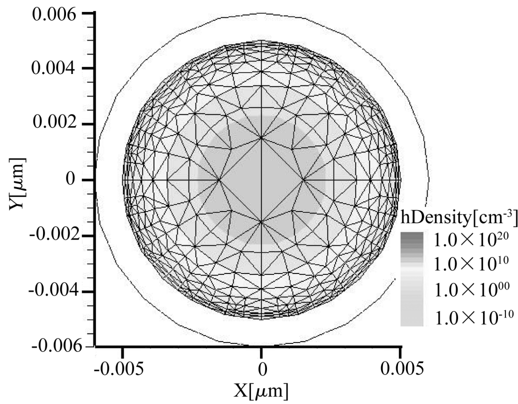

Fig.8. Cross-sectional view (Z-cut at Z=0, mid-channel) of simulated hole density for a fully encapsulated GAAC FinFET when V_D and V_G are biased at −0.05 and 0.8 V respectively; a = 5 nm, L = 10 nm, d = 1 nm, $N_A = 10^{19}$ cm^{-3}.

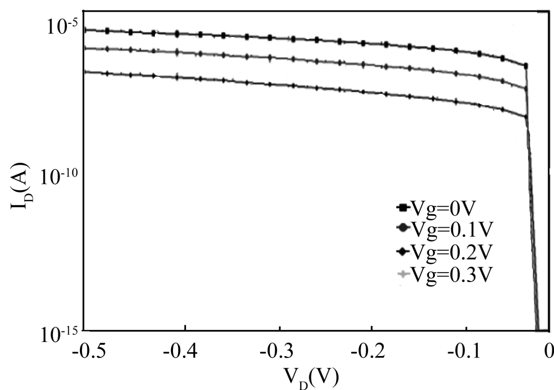

Fig.9. Simulated plot of I_D versus V_D for a p-channel GAAC FinFET; a = 5 nm, L = 10 nm, d = 1 nm, $N_A = 10^{19}$ cm^{-3}.

fabrication processes[8−12], our fabrication method includes forming an undercut structure in the buried oxide layer of an SOI wafer underneath the wire pattern and selectively removing the undercut structure beneath the middle-section to form a cavity with unit length and height. The method includes forming a channel region by shaping the middle section above the

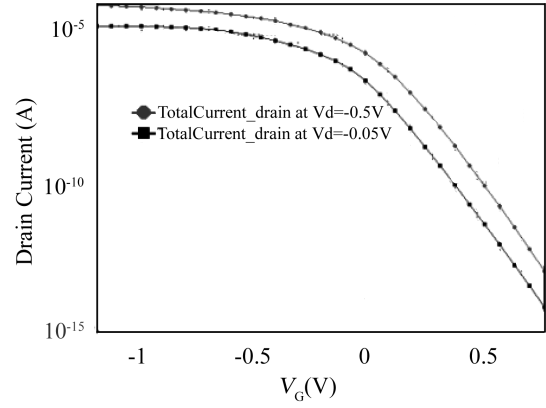

Fig.10. Simulated plot of I_D versus V_G for a p-channel GAAC FinFET; a = 5 nm, L = 10 nm, d = 1 nm, $N_A = 10^{19}$ cm^{-3}.

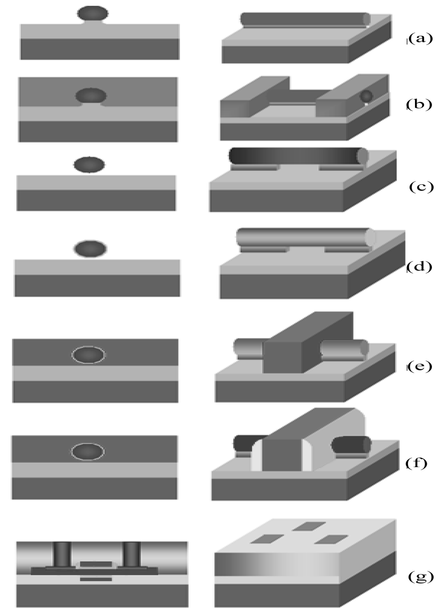

Fig.11. Process flow for GAAC FinFET illustrated in cross-sectional and perspective views: (a) Define silicon fin by lithography and silicon active area etch (dry and wet etch); (b) Define the pattern by lithography to expose the fin channel and oxide underneath; (c) Lateral etching of the oxide underneath the channel by buffered oxide etchant (BOE) to form a tunnel; (d) Gate oxide growth; (e) Gate formation by gate material deposition, patterning and etching; (f) ONO spacer formation, source/drain implant and nickel silicide S/D and gate formation; (g) ILD and contact formation.

cavity into a cylindrical shape. The process flow for making this architecture, with detailed cross-sectional and perspective views, is illustrated in Fig.11. The flow is characterized by its simplicity and full compatibility with conventional planar CMOS technology.

6. Conclusion

The GAAC FinFET device provides the best gate electric field control as it has a virtually “infinite” number of gates, with all gates in close proximity to the channel and enhanced electrostatic control from the gate electrode over the charge carriers in the channel. Thus, the short channel effect is eliminated in the accumulation mode. The I_{on}/I_{off} ratio of the de-

vice can be greater than 10^6 as a key parameter for device operation. In particular, the performance and scalability of the GAAC device are improved in relation to conventional multi-gate FinFETs. Our proposed fabrication flow for the GAAC FinFET is simple and compatible with planar CMOS technology. It is a promising candidate for continuing CMOS technology beyond the "end of the silicon technology roadmap" by shrinking the gate length along the cylindrical silicon diameter. Device fabrication is ongoing.

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