Design of a 4.6 GHz high-performance quadrature CMOS VCO using transformer couple*

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Abstract: A CMOS quadrature LC-tank voltage-controlled oscillator topology which uses a planar spiral transformer as coupling elements has been implemented in mixed-signal and RF 1P6M 0.18 μm CMOS technology of SMIC. The measured phase noise is –125.7 dBc/Hz at an offset frequency of 1 MHz from the carrier of 4.6 GHz while the VCO core circuit draws only of 10 mW from a 1.8 V supply. The measured phase error is approximately 1.5° based on the time domain outputs and the output power is about –2 dBm. The VCO can cover the frequency range of 4.36–4.68 GHz. The tuning range is 320 MHz (7.0%) and the FOM is –189 dB.

Key words: low-phase-noise; transformer; quadrature; voltage-controlled oscillator; couple
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1. Introduction

Recently, the research and development of the direct conversion radio (zero-IF) and low-IF image reject architecture transceivers have dramatically increased due to the need for low-power, low-cost, and large-scale integration[1]. These architectures require quadrature local oscillator (LO) signals. So far, many techniques have been proposed to generate the quadrature carrier signals, such as RC–CR phase shift network, poly-phase network, positive and negative edge triggered flip-flop, even-stage ring oscillator, and LC coupled quadrature oscillator. Among them, the LC coupled quadrature oscillator shows a lower phase noise in comparison to others, and is widely used in RF transceivers[2–4].

The cross-coupling architecture is popular quadrature generation technique. The I- and Q- phase signals are generated by cross-coupling of two symmetric differential VCOs. The conventional cross-coupling method, as shown in Fig.1 (a), adopts parallel coupling transistors as core transistors[5]. The size ratio between the coupling transistor, Mc, and the switching transistor, Ms, is critical for the phase accuracy. In such an architecture, there is a tradeoff between the accuracy of the quadrature phase and the phase noise, but the additional transistors tend to dissipate rather high power. In the case of a series-coupled quadrature VCO, as shown in Fig.1 (b), the coupling transistors are connected in series with the switching transistors[6]. The size of the coupling transistors can be increased to acquire better phase accuracy without increasing much current consumption.

Based on the topology shown in Fig.1, many works have been reported to reduce the phase noise and the power dissipation. However, on the aspects of the phase noise and the power dissipation, the presence of the additional coupling transistors makes it inherently inferior to the quadrature LC-VCO topology proposed in this paper, which enables quadrature coupling without additional transistors[7,8]. In this paper, an alternative method to obtain quadrature oscillators based on the differential coupling at the second harmonics of two differential oscillators is also presented. In fact, if there is a phase shift of 180° between the second harmonics of two oscillators, their fundamental frequency components will be in quadrature. To analyze the proposed design, concepts about injected and coupled oscillators are revised.

2. Circuit design

2.1. Circuit topology

Rategh and Lee have shown that in differential oscillators, common-mode nodes can be used to inject a frequency close to twice the fundamental frequency of an oscillator and lock the oscillator to this injected signal[9]. As long as both oscillators keep locked, any change in the injected signal will be transmitted to the injected oscillator at the fundamental frequency. From this point of view, the oscillator is working as an analog frequency divider if the fundamental harmonic is considered as the circuit output. As a consequence, if two oscillators are injected by two second harmonics with a phase shift of 180°, their fundamental output will be in quadrature. A simplified schematic of the quadrature oscillator is shown in Fig.2. Compared to the topology shown in Fig.1, the coupling transistors are removed and two identical LC oscillators coupled through an integrated transformer to generate the quadrature outputs. The single side oscillator is the classical differential LC oscillator and consists of the complementary cross-coupled CMOS differential pairs and the LC-tank. The differential transistor pairs generate the negative resistances to compensate the losses of the LC-tank. LC-tank circuit consists

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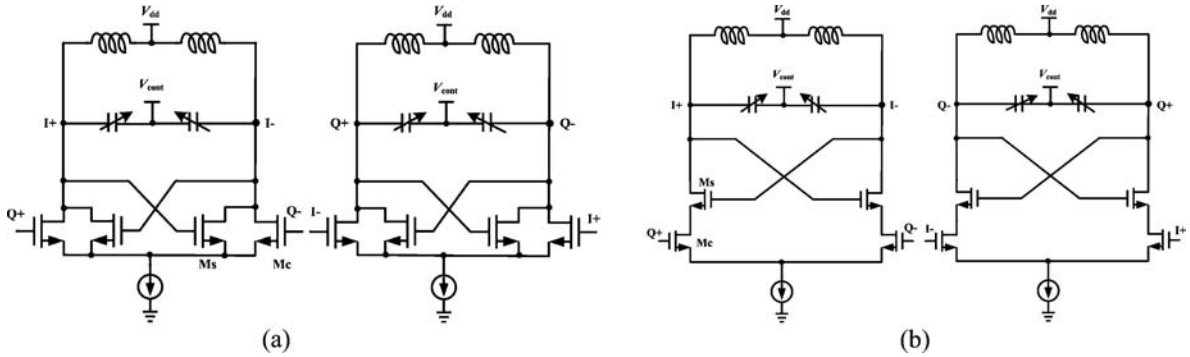

Fig.1. Schematic of the QVCO: (a) Parallel coupled QVCO; (b) Series coupled QVCO.

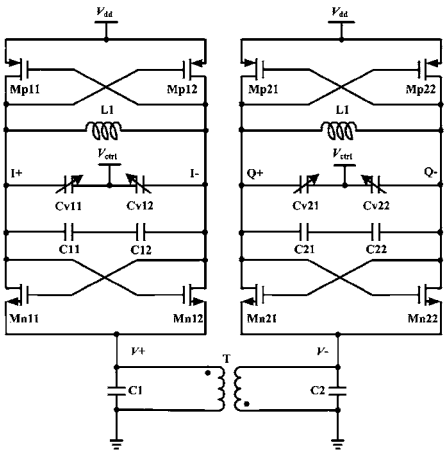

Fig.2. LC-QVCO schematic with transformer coupling.

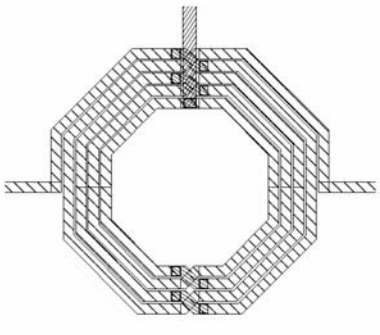

Fig.3. Layout of the transformer.

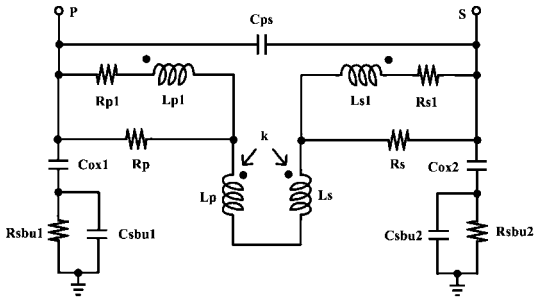

Fig.4. Proposed equivalent circuit model of the transformer.

of the on-chip differential inductor, the on chip MIM capacitors and the MOS varactors. The relative sizes of Mn1 and Mp1 are selected to make the DC value of LC-tank be equal to about half of voltage source. It was found that when Mn1 and Mn2 share the same (minimum) length, the size of Mp1 should be three and four times as large as Mn1 for optimal phase-noise performance[10]. PMOS varactors are used in inversion mode because of the wide capacitor variation that can be obtained with a low variation of source to gate bias voltage[11].

The semi-empirical model proposed in Ref.[12], known also as the Leeson–Cutler phase noise model, is based on an LTI assumption for tuned tank oscillators. It predicts the following behavior for $L(\Delta f)$:

$$L(\Delta f) = 10\lg\left\{\frac{2FkT}{P_{\rm s}}\left[1+\left(\frac{f_0}{2Q_{\rm L}\Delta f}\right)^2\right]\left(1+\frac{\Delta f_{1/f^3}}{|\Delta f|}\right)\right\}, \quad (1)$$

where F is an empirical parameter, k is the Boltzmann's constant, T is the absolute temperature, $P_{\rm s}$ is the average power dissipated in the resistive part of the tank, f_0 is the oscillation frequency, $Q_{\rm L}$ is the effective quality factor of the tank with all the loadings in place, Δf is the frequency offset from the carrier, and $\Delta f_{1/f^3}$ is the frequency of the corner between the $1/f^3$and $1/f^2$ regions in the sideband spectrum of the phase noise of the VCO. From Eq.(1), the phase noise is inversely proportional to the square of $Q_{\rm L}$ and to the signal power. The oscillating amplitude and signal power could be maximized at the resonant frequency given bias condition. As a result, to realize VCOs with low-power and low-phase-noise, small series loss and large L/C ratio of the LC-tank are desirable[13]. The transformer is connected between the common-mode nodes at the sources of NMOS transistors and ground to substitute the injection oscillator. This transformer plays a fundamental role because the required phase shift of 180° at the second harmonics frequency can be obtained at the sources of NMOS transistors through the transformer. The transformer also serves as a filtering network for the LC oscillators, the phase noise performance of the quadrature signals is better than the LC oscillator itself. Obviously, the transformer characteristics play an important role in the proposed circuit, so the design and optimum of the transformer is the key step to achieve an accurate low phase noise quadrature VCOs.

2.2. Transformer model and parameters extraction

The transformer is a symmetrical spiral inductor with center-tap indeed, which tries to make the signals at nodes $V+$ and $V-$ differential. It consists of two closely-coupled loops of 4.5 turns with a metal width of 8 μm, a turn-to-turn spacing of 1.5 μm and an outer dimension of 212 μm resulting in a coupling factor large than 0.75, as shown in Fig.3. A lumped

Table 1. The extracted equivalent circuit parameters of the transformer.

L_p (nH)	R_p (Ω)	L_{p1} (nH)	R_{p1} (Ω)	R_{sub1} (Ω)	C_{sub1} (fF)	C_{ox1} (fF)	C_{ps} (fF)	k
2.05	4.92	0.99	3.04	767	18	23	99	0.76

Table 2. Comparison of the most recent state-of-the-art quadrature VCOs.

Reference	[2]	[3]	[5]	[7]	This work
Technology and remarks	0.18-μm CMOS	0.25-μm CMOS	0.18-μm CMOS	0.25-μm CMOS	0.18-μm CMOS
Supply voltage (V)	1.7	2	1.8	2.5	1.8
Power (mW)	8.6	30	5.4	22	10
Oscillation frequency (GHz)	4.505	1.57	1.1	4.88	4.56
Turning range (GHz)	4.12–4.89	1.36–1.69	1.047–1.39	4.60–5.20	4.36–4.68
Phase noise @1MHz (dBc/Hz)	−115.06	−133.5	−120	−125	−125.7
FOM (dB)	−180.5	−187.1	−173.5	−185	−189
Measured phase error (°)	–	–	–	2.6	1.5

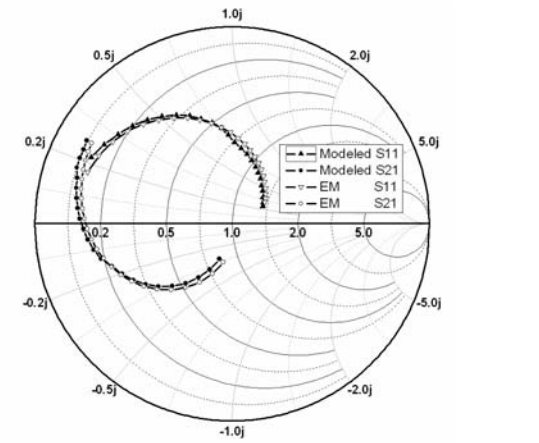

Fig.5. Comparison of modeled and EM simulated S-parameters.

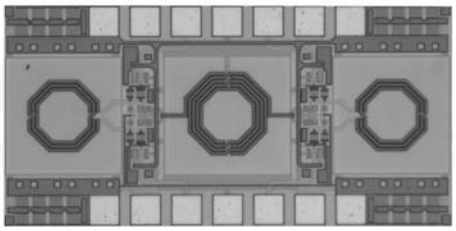

Fig.6. Microphotograph of the QVCO.

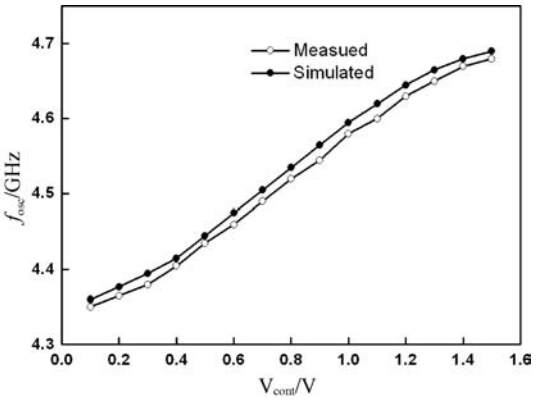

Fig.7. Voltage-control-frequency curve.

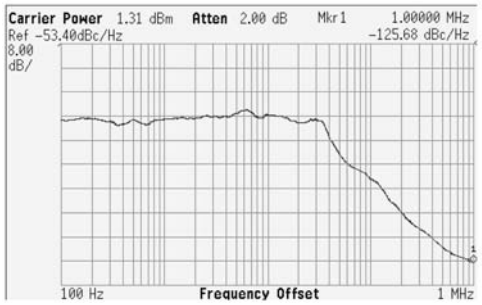

Fig.8. Measured phase noise.

RLC equivalent circuit of the transformer shown in Fig.4 was obtained from the 0.18-μm mixed-signal 1P6M salicide 1.8 V/3.3 V RF Spice models. The definitions of the parameters in the model can be found in the RF Spice models too. The most important aspect for modeling an on-chip transformer is the extraction or fitting of model parameters. The layout structure EM simulation and the lumped elements parameters extraction were finished by commercial software Agilent ADS 2003. The extracted equivalent circuit parameters of the transformer are listed in Table 1. Figure 5 compares the modeled and EM simulated S-parameters for the transformer in the frequency range of 500 MHz–10 GHz. The modeled results show a high agreement with the EM simulated up to 10 GHz.

3. Measurement results

For demonstration, the presented VCO circuit has been fabricated in SMIC's 0.18 μm CMOS process. The process has six metal layers with a thick top metal of 2.17 μm, The threshold voltages of the NMOS and PMOS devices are about 0.45 and −0.55 V, respectively. According to the ISF theory[14], the phase noise can be significantly reduced if certain symmetry properties exist in the waveform of the oscillation. So any asymmetry in the coupling circuits or the individual oscillators will result in a steady-state operation of the unilaterally coupled oscillators that differs from the ideal. Thus, the layout of the QVCO design must be focused on the full symmetry. The chip microphotograph is shown in Fig.6. The size of the chip including the pads is 0.55×1.1 mm^2. The output inverter buffers were used for measurement with an Agilent E4440A spectrum analyzer. Figure 7 shows the tuning range of the VCO as a function of control voltage. The tuning range is 320 MHz, from 4.36 to 4.68 GHz, with the control voltage from 0.2 to 1.5 V. Figure 8 shows a plot of the measured phase noise versus offset frequency at 4.6 GHz

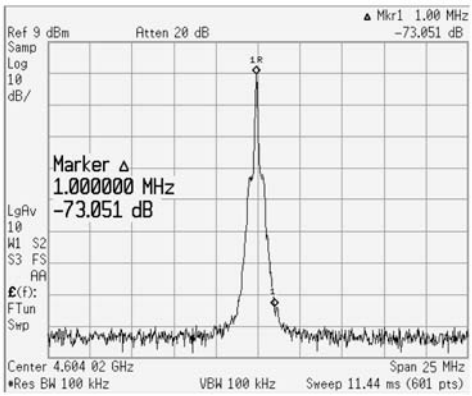

Fig.9. The measured output spectrum of the QVCO.

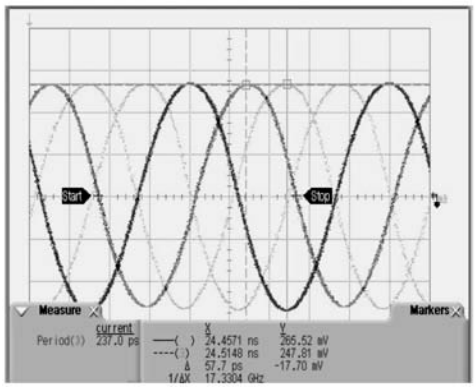

Fig.10. The measured output waveforms of the QVCO.

oscillation. The phase noise at 1 MHz offset is –125.7 dBc/Hz while dissipating 5.5 mA for the VCO core circuit under a 1.8 V supply. Figure 9 shows the measured output spectrum of the quadrature oscillator at 4.6 GHz, and the output power is about −2 dBm. The output impedance of inverter buffer is higher than the input impedance of spectrum analyzer (usually is 50 Ω), which can induce the lower power output and efficiency, but the actual output power of the signal is larger than the measurement result. The phase accuracy of the quadrature oscillator is another important performance parameter. There are no effective methods to measure the phase error because the present oscillograph could not measure the phase error between four-channel several GHz signals. Figure 10 shows the time domain outputs measured by Agilent E86100 samples oscillograph. Based on the time domain outputs, the measured phase error and quadrature amplitude error are approximately 1.5° and 0.3 dB, respectively, and the real amplitudes of the signals are around 250 mV at 4.4 GHz.

A figure of merit (FOM) has been defined to compare VCOs performances:

$$\mathrm{FOM} = L(f_0, \Delta f) + 10\lg\left[\left(\frac{f_0}{\Delta f}\right)^2 \frac{P_{\mathrm{VCO}}}{[\mathrm{mW}]}\right], \qquad (2)$$

where $L(f_0, \Delta f)$ is the single side band phase noise at the offset frequency Δf from the carrier frequency f_0. P_{VCO} denotes the total power consumption of the VCO. The proposed QVCO achieve FOM of –189 dB based on Eq.(2) from the carrier of 4.6 GHz. Table 2 summarizes the performance comparison of the most recent state-of-the-art quadrature VCOs. It is obvious that the proposed VCO has the best FOM value and low phase noise compared to the published results in Refs.[2, 5]. The measured phase error and the power consumption of the proposed VCO are less than the published results in Ref.[7]. The measured phase error in Ref.[7] is too large to meet the demands of the direct conversion radio and low-IF image reject architecture transceivers. Furthermore the measured results of phase error are not given in Refs.[2, 3, 5].

4. Conclusion

A low-phase-noise quadrature oscillator with transformer couple was presented. It has been implemented in SMIC's 0.18-μm CMOS process. The measured results show that the proposed oscillator can achieve a phase noise of –125.7 dBc/Hz at 1 MHz offset from 4.6 GHz carrier. The tuning range is 320 MHz from 4.36 to 4.68 GHz and the FOM is –189 dB with a power dissipation of 10 mW under a 1.8 V supply. The measured phase error is about 1.5° based on the time domain outputs.

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