A CMOS image-rejection mixer with 58-dB IRR for DTV receivers*

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Abstract: The design, implementation, and characterization of an image-rejection double quadrature conversion mixer based on RC asymmetric polyphase filters (PPF) are presented. The mixer consists of three sets of PPFs and a mixer core for quadrature down conversion. Two sets of PPFs are used for the quadrature generation and the other one is used for the IF signal selection to reject the unwanted image band. Realized in 0.18-μm CMOS technology as a part of the DVB-T receiver chip, the mixer exhibits a high image rejection ratio (IRR) of 58 dB, a power consumption of 11 mW, and a 1-dB gain compression point of –15 dBm.

Key words: mixer; image rejection; polyphase filter
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1. Introduction

Recent research on system on one chip (SoC) transceivers shows a trend of eliminating the external SAW filters for image rejection[1]. Image rejection mixers based on RC asymmetric polyphase filters (PPF), which are used in communication circuits for quadrature generation and image rejection, make transceivers without SAW filters possible[2, 3]. RF mixer designs based on PPFs for image rejection have been reported[4–8]. In this paper, the design of an image rejection mixer based on PPFs will be discussed in detail and implemented with a 0.18-μm CMOS technology.

2. Mixer architecture

The mixer structure is shown in Fig. 1; there are three sets of PPFs: the RF and LO PPFs for quadrature signal generation and the IF PPF for image rejection. The RF frequency, which is 1220 MHz, is down converted to the IF of 36.125 MHz with the LO frequency of 1183.875 MHz, while the image band centered on 1147.75 MHz, will be rejected. A passive FET double balanced mixer had been adopted as a double-quadrature converter due to its lower power consumption and better matching properties than Gilbert active mixer[4]; further amplification at the mixer output would compensate the loss in the signal path.

3. Design considerations

3.1. Properties of the PPF

Unlike the traditional RC-CR image rejection topology, which only provides a single pole at the rejected frequency, the desired rejection bandwidth and attenuation can be achieved by cascading PPF stages with different poles. With the PPF, the image rejection ratio (IRR) of the receiver is determined by the phase and amplitude mismatch caused by the RC spread within the PPF stages[3]. The absolute deviation of element values in the PPF shifts the pole frequencies, while the relative spread of the R and C values within the same stage degrades the IRR. For a typical super-heterodyne receiver with a single-quadrature conversion structure, the phase and the amplitude mismatch of less than 0.1% for the RF and the LO signals as well as the IF PPF are required for an image rejection of 60 dB; this requirement can be greatly relaxed by adopting the double-quadrature conversion structure[4, 8], which only requires a 3% amplitude and phase mismatch for I and Q signals from the RF and the LO, but still requires the same mismatch level of 0.1% for the IF PPF, as in the case of single-quadrature conversion. Thus, a lot of attention should be paid to reduce the mismatch in the IF PPF, while an acceptable signal loss and overall system noise performance should also be maintained.

3.2. Design of the RF and LO PPFs

In order to reject the image signal, differential I and Q

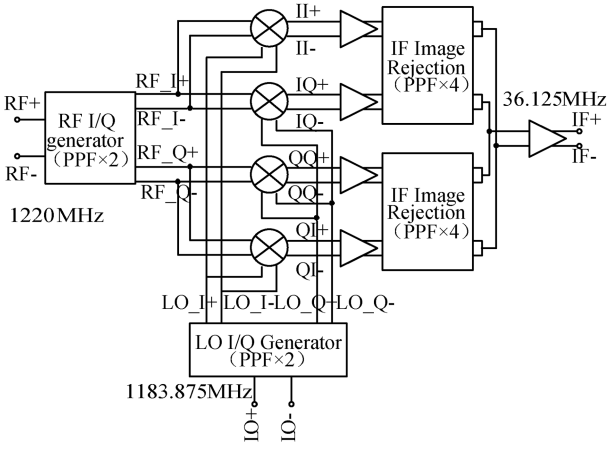

Fig. 1. Mixer block diagram.

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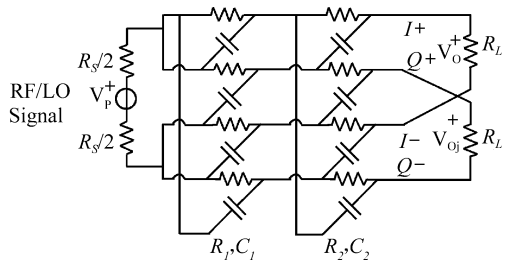

Fig. 2. Schematic of the two-stage PPF used for the quadrature generation.

signals for RF and LO signals are needed.

A two-stage PPF with the pole frequency centered on the image frequency is used for the RF or LO quadrature generation, as shown in Fig. 2. By solving the Kirchhoff equations for this circuit, the following relation is found for the output voltage across R_L:

$$V_O = \frac{1}{2}\frac{(1+j)RR_L L V_p}{R^2 - R_L R_S + j(R^2 + 2RR_S + RR_L + R_L R_S)}, \quad (1)$$

where R represents the average resistance of the resistors used in different stages of the PPF (e.g. $R \approx \sqrt{R_1 R_2}$); R_S and R_L are source and load resistance, respectively.

The maximum output voltage can be found when

$$R^2 = R_L R_S. \quad (2)$$

If we let $R = \sqrt{R_L R_S}$ and $R_L = kR_S$, the maximum output voltage V_{OMAX} is:

$$V_{OMAX} = V_P \frac{\sqrt{2}}{2}\frac{k}{2 + 2\sqrt{k} + k}. \quad (3)$$

Based on Eqs. (1) and (2), the maximum power gain of this PPF can be achieved when:

$$R_S = R_L/2. \quad (4)$$

LO quadrature signal generation can be achieved by using digital dividers; a large amplitude LO signal with strong driving capability can be generated by optimizing the parameters of the driving inverters. However, digital dividers will increase the power consumption and the divider input frequency must be at least two times of the LO input frequency; this will increase the VCO power consumption. Also, it is hard to achieve a good phase relationship for the quadrature LO signal using this divider. The PPF can generate a precisely matched differential quadrature signals without externally required power. Since the gate capacitance of the mixer transistor is small and the real part of the input impedance is large, a polyphase structure is sufficient for quadrature LO signal generation, even without a buffer to boost the driving capability. Here, considering the spread of the technology, a two-stage PPF is used to generate I and Q signals for LO and RF signals. Besides the different pole frequencies, there are other issues that one should consider when designing the PPFs for the RF and LO signal generation. For a PPF used to generate the RF quadrature signals, we need to consider the noise performance;

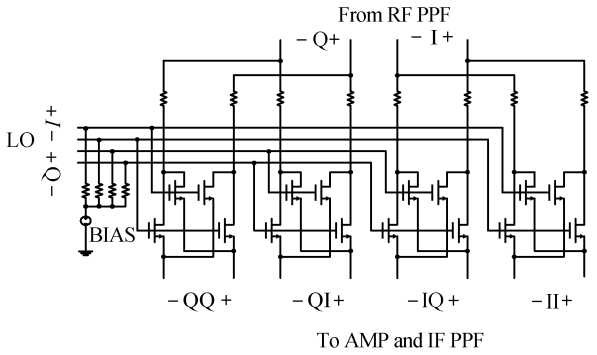

Fig. 3. Schematic of the passive double-quadrature mixer core.

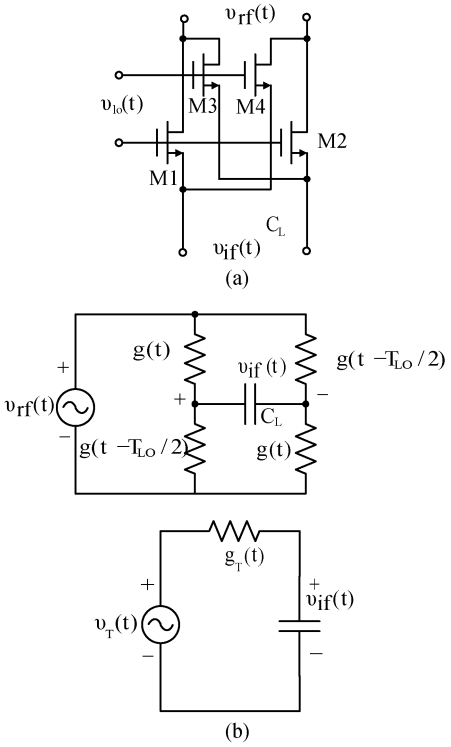

Fig. 4. (a) Passive double-balanced mixer cell; (b) The mixer can be modeled as Time varying conductances and its Thévenin equivalent circuit[9].

while for the LO PPF, it is desirable to drive the gates of the mixer transistors with high LO voltages, which is good for getting a higher LO voltage and, thus, a low on-resistance for the mixer transistors. Due to the limited chip size, matching is not possible for the LO signal and the maximum voltage gain can only be achieved by increasing the k in Eq. (3). The k for the LO PPF is about 30.

3.3. LO injection and mixer design

In this design, a passive double balanced mixer is adopted due to its low power consumption and simple structure, which gives the designer a better control of the mismatch elements. The schematic of the mixer core is shown in Fig. 3. The transistors in the mixer operate in the linear region and work as voltage switches.

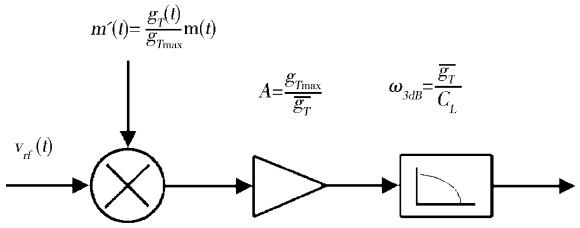

Fig. 5. The derived block diagram of the passive mixer[9].

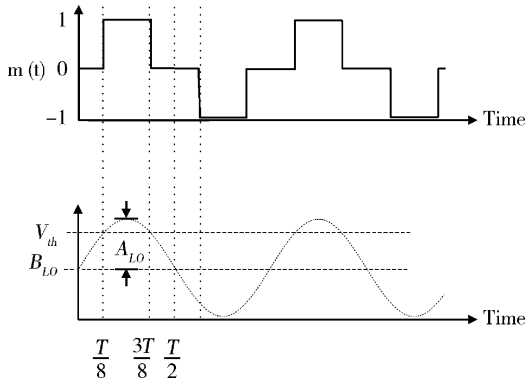

Fig. 6. The bias condition for the LO signal for maximum conversion gain.

As discussed in Ref. [9], the passive mixer cell (Fig. 4(a)) can be modeled as a Thévenin equivalent network, as shown in Fig. 4(b).

The output IF voltage can be expressed as

$$v_{\mathrm{T}}(t) = \frac{g(t) - g(t - T_{\mathrm{LO}}/2)}{g(t) + g(t - T_{\mathrm{LO}}/2)} v_{\mathrm{rf}}(t) = m(t) v_{\mathrm{rf}}(t). \quad (5)$$

And the Thévenin conductance is:

$$g_{\mathrm{T}}(t) = \frac{g(t) + g(t - T_{\mathrm{LO}}/2)}{2}. \quad (6)$$

In Ref. [9], the system block diagram of the mixer was also derived, as shown in Fig. 5. Here $g_{\mathrm{T}}(t)$ is the equivalent conductance shown in Fig. 4(b), $\overline{g_{\mathrm{T}}}$ is the DC level of $g_{\mathrm{T}}(t)$, g_{Tmax} is the maximum value of $g_{\mathrm{T}}(t)$, $m(t)$ is defined in Eq. (5), and C_{L} is the load capacitance at the mixer output. So, as stated in Ref. [9], assuming $\overline{g_{\mathrm{T}}}/(2\omega_{\mathrm{LO}}C_{\mathrm{L}}) \leqslant 1$, using sinusoidal signals as the LO signal leads to a better conversion gain, as compared with using square wave signals; also, the conversion gain is even better if the applied sinusoidal is a break-before-make case, which means the switching transistors have resulting conduction cycles less than 50%.

The LO signal can be expressed as $v_{\mathrm{LO}}(t) = A_{\mathrm{LO}} \cos(2\pi f_{\mathrm{LO}} t + \phi_{\mathrm{LO}}) + B_{\mathrm{LO}}$. If defining $r = |V_{\mathrm{th}} - B_{\mathrm{LO}}|/A_{\mathrm{LO}}$, the extreme case would be that $r = 1$, corresponding to an ideal conversion gain of unity[9].

However, in a real design, this will not happen since, when $\overline{g_{\mathrm{T}}}$ is too low, the assumption $\overline{g_{\mathrm{T}}}/(2\omega_{\mathrm{LO}}C_{\mathrm{L}}) \leqslant 1$ is not valid anymore. In this mixer circuit, since the IF is relatively high (i.e., 36.125 MHz), the lowpass filter formed by $\overline{g_{\mathrm{T}}}$ and C_{L}, as shown in Fig. 5, can not be neglected. Thus, conversion gain is approximating to unity when $r \approx 1$ if we neglect the lowpass filter in Fig. 5; but as r increases to a certain point

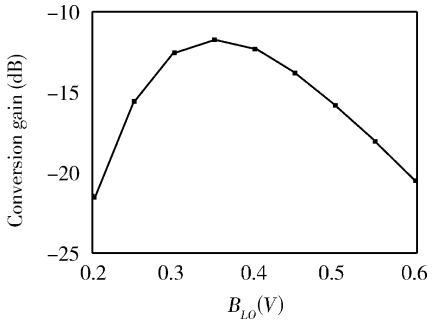

Fig. 7. Bias voltage at transistor gates versus simulated IF conversion gain.

when the resulting $\overline{g_{\mathrm{T}}}$ is small enough that $\omega_{3\mathrm{dB}}$ is comparable to the IF, the conversion gain will start to drop down.

In this design, in order to reduce the power consumption, a two-stage PPF is used instead of digital dividers to generate the LO quadrature signal. So, the injected LO signal are sinusoidal signals. At a fixed A_{LO}, the r for the highest conversion gain can be found by varying the DC biasing point B_{LO}. In this circuit, it is found by simulation that the maximum gain happens when the transistors operates at about 25% on-off-ratio. As shown in Fig. 6, the corresponding biasing voltage B_{LO} for the highest conversion gain of the mixer is:

$$B_{\mathrm{LO}} = V_{\mathrm{th}} - A_{\mathrm{LO}} \sin 45^{\circ}. \quad (7)$$

The threshold voltage of the MOS transistor used in the mixer core is about 0.5 V, and the LO power is 3 dBm after passing LO PPF. The peak LO voltage of the transistor is 212 mV. Based on Eq. (7), the optimum biasing is 0.35 V. The simulation result of the conversion gain versus B_{LO} is shown in Fig. 7. The peak of the conversion gain in the measurement plot deviates with the simulated B_{LO} by about 40 mV. This might be due to the process corner, as shown in Fig. 13.

The mixer core consists of four balanced passive mixers. The mismatch of the mixing transistors will leads to a worse IRR. To reduce the mismatch, the layout of them is highly symmetrical; the length and the width of the transistor gates are optimized based on the following consideration: longer channel length and width will lead to larger parasitic capacitance and a decrease of the frequency performance, which corresponds to a lower conversion gain, while for smaller W and L, the mismatch will be bigger and the IRR requirement may not be fulfilled. It is a great advantage to use the submicron CMOS process for the mismatch-critical mixer design since the matching can be ensured by high fabrication accuracy. So, fewer penalties are suffered to maintain the matching while keeping an acceptable conversion gain. To reduce the substrate noise, all transistors are surrounded by guard rings to reduce the noise interference.

3.4. Design of the IF PPF

The IF PPF is the critical part for the image rejection since the overall rejection ratio mainly depends on the matching property of it. In this design, an IRR of more than 55 dB within a rejection bandwidth of 8 MHz centered on 36 MHz

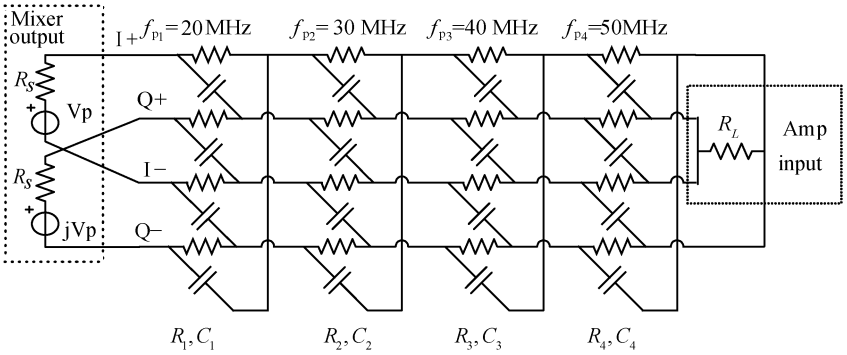

Fig. 8. Schematic of four-stage PPF used for IF selection.

is required. As shown in Fig. 8, a four-stage PPF with a combined differential output is used for the image rejection. To compensate the process spread, the designed rejection bandwidth is increased to 40 MHz, which can only be achieved by cascading four polyphase stages. Each stage has its own pole frequency, which is $f_{pN} = 1/2\pi R_N C_N$, where N is the stage number. Each stage will result in a notch at its pole frequency to reject the image IF signal. Component matching of 0.3% is required for a 55-dB rejection ratio[4], and the careful layout design of it will be discussed in section 3.5.

To achieve the maximum voltage gain, by solving the Kirchhoff equations for this circuit with some simplifications, the resistors in the polyphase stages should be chosen according to the formula for the lowest loss:

$$R = \sqrt{R_S R_L}, \tag{8}$$

where R represents the average resistance of the resistors in the four stages.

If $R = \sqrt{R_S R_L}$ and $R_L = kR_S$, the following relation is found for the voltage on R_L:

$$V_{RL} = \frac{k}{2k + 2\sqrt{k} + 1} \frac{1}{1 + j} V_P. \tag{9}$$

The voltage gain is proportional to k. Similar to the quadrature generation and based on Eq. (9), the maximum power gain is achieved when

$$R_S = 2R_L. \tag{10}$$

In practice, the choice of the resistances of the resistors in the PPF is a compromise between noise performance, gain, IRR, and available chip area. Components occupying a larger area will have less mismatch. A smaller resistor in the PPF requires a larger capacitor for the same pole frequency. This will consume a larger area, but will also reduce the noise. On the other hand, the larger the resistor is, the higher the noise voltage would be, although the required capacitor is small. Here, a capacitance of about 2 pF is a proper choice for the capacitors within each PPF stage.

As shown in Fig. 1, two identical IF PPFs are placed in the I and Q channel for less RF signal attenuation[4]. The simulation result shows that this structure improves the linearity rather than the signal loss. In a design where a lower linearity can be tolerated, only one IF PPF is recommended for a smaller chip area.

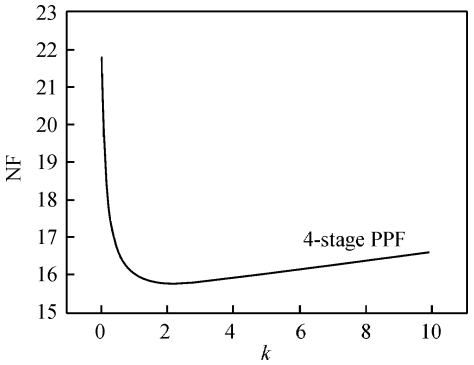

Fig. 9. Noise figure of the four-stage PPF versus k.

The resistors in this PPF are the main noise contributors for the entire mixer. The simulation shows that the noise voltage at the PPF output is proportional to the resistances of the PPF resistors and the load resistor. Since the IF frequency is feed into an amplifier having a high input impedance, we are more concerned with the signal voltage transfer than the signal power transfer. The voltage gain G, as well as the output noise, are proportional to the load resistance R_L.

$$G(R_L) \propto R_L, \tag{11}$$

$$N(R_L) \propto R_L. \tag{12}$$

The best output noise figure (NF) can be determined by simulation. We assume that $R_L = kR_S$, where k is the factor to be swept. To simplify the simulation, we also assume that all resistors in every stage of this PPF have the value $R = \sqrt{R_S R_L}$ for the max passband gain. Then, the simulated noise figure can be plotted, as shown in Fig. 9. It can be seen that the lowest noise figure is located at about $k = 2.2$, corresponding to an NF = 15.8 dB. The NF of the entire mixer can be reduced by increasing the gain of the amplifier between the mixer core and the IF PPF. The simulated NF of the entire mixer is 20 dB.

3.5. Mismatch reduction

To fulfill the high IRR requirement, a carefully designed layout has been applied to the entire mixer. The mixer core and the PPFs are placed in a symmetric topology, and the parasitic parameters of the wires are balanced by snake-line routing with the same corners and vias. Special attention has been

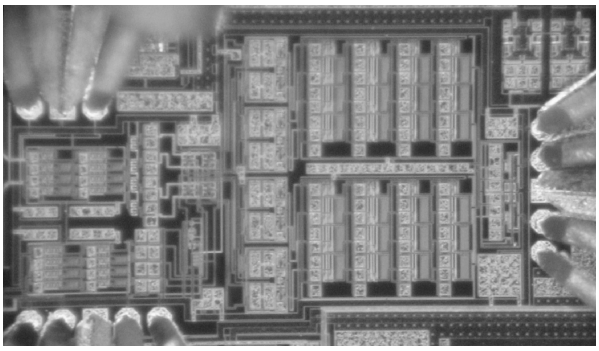

Fig. 10. Fabricated chip during the on-wafer test.

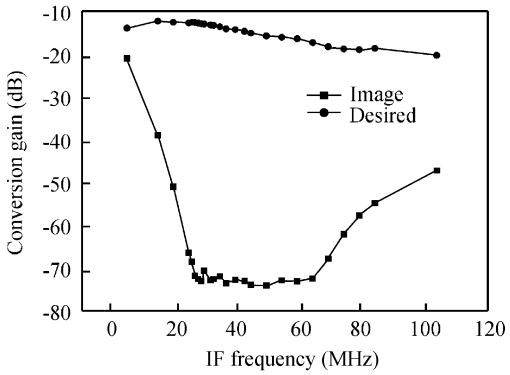

Fig. 11. Measured conversion gains for desired and image signals.

paid to arrange the IF PPF; the large sized capacitors, and the resistors have been chosen to bring the mismatch to a minimum.

4. Experimental results

The mixer is fabricated with a 0.18-μm 2p6m CMOS process. The chip micrograph is shown in Fig. 10. The total area of the chip is 1680×935 μm^2.

The measured conversion gain and IRR of the mixer is shown in Fig. 11 and Fig. 12. The attenuation of the image signal over the desired bandwidth is at least 58 dB, with a conversion gain over the desired bandwidth of about –13.5 dB. As discussed in section 3.3, the conversion gain versus the LO bias voltage are measured by applying an adjustable external bias voltage to the chip, shown in Fig. 13. The optimum LO bias voltage is around 0.39 V. The total current of the mixer is about 6 mA, and the amplifiers consume most of the power. The measurement results are summarized in Table 1.

5. Conclusion

The design and implementation of an image-rejection mixer based on PPFs have been presented. The PPF properties, the optimization, the mixer biasing, the mixer signal analysis, the noise performance, as well as the layout considerations have been discussed in detail. The mixer shows an IRR of 58 dB with a conversion gain of –13.5 dB. The high image-rejection ratio of the mixer is achieved by adopting the double-quadrature conversion structure and a proper layout design.

Table 1. Summary of measurement results.

Parameter	Value
Process	0.18-μm 2p6m CMOS
Supply voltage	1.8 V
Conversion gain (Pass band)	–13.5 dB
IRR	$\geqslant$ 58 dB
Power consumption	11 mW
RF frequency	1220 MHz
IF frequency and bandwidth	36.125 MHz ± 4 MHz
1-dB gain compression point (input)	–15 dBm
NF	20 dB

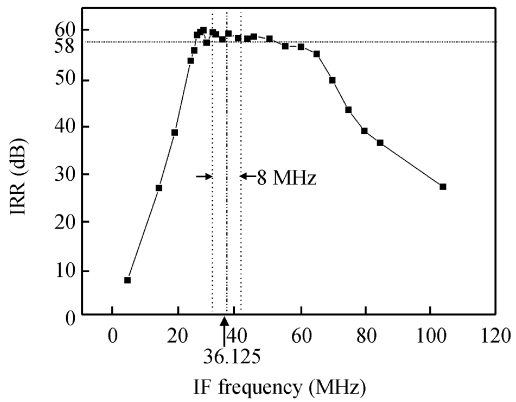

Fig. 12. Measured IRR over the designed bandwidth.

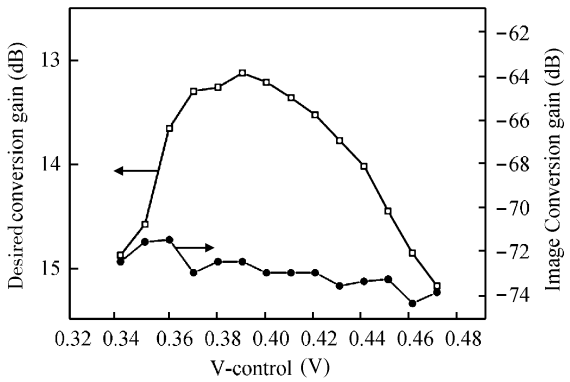

Fig. 13. Bias voltage at the transistor gates versus the measured desired and image conversion gain.

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