A fully integrated BPSK amplitude and spectrum tunable transmitter for IR-UWB system

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Abstract: A 3–5 GHz low power BPSK modulated impulse radio UWB transmitter is implemented in 0.13 μm CMOS technology. In this design the amplitude and spectrum of the output impulse are both tunable to solve the special problem in IR-UWB, where it is difficult to control the spectrum. Measurement results indicate that, by changing the control bits in the gain control circuit and differential circuit, the 3-step peak-to-peak voltage amplitudes are 240, 170 and 115 mV and the center frequency of the impulse can be tuned from 3.2 to 4.1 GHz. A power controlled output buffer is designed to drive the antenna. The total power consumption is only 4.44 mW when transmitting a baseband signal of 100 MHz. The chip area is 1.2×1.4 mm^2.

Key words: IR-UWB; pulse generator; BPSK
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1. Introduction

Ultra wideband (UWB) technology has received significant interest since the FCC released an unlicensed spectrum of 3.1–10.6 GHz for UWB applications. The maximum power spectral density of the UWB is −41.25 dBm/MHz, which is extremely low. This results in small interference with other radio signals while maintaining excellent immunity to interference from these signals. Hence, UWB can coexist with those wireless standards that have already been allocated within the 3.1–10.6 GHz frequency band. UWB techniques are promising, and they are capable of accurate position location and high-rate short-range ad hoc networking, as well as high resolution sensing[1].

There are three main proposals for UWB systems: multi-band OFDM (MB-OFDM), direct-sequence UWB (DS-UWB) and carrier-less impulse radio UWB (IR-UWB). The transceiver architecture of MB-OFDM[2,3] is similar to that of a conventional wireless OFDM system. It is viewed as the best suited technology for communication applications with very high data rate. The DS-UWB[1,4] and IR-UWB[5–7] are impulse based systems. They need no FFTs, no DACs and no fast hopping synthesizers, and since the signal of the impulse-based UWB is duty-cycled, the circuits can be shut down between impulses intervals. Therefore, the impulse-based system can lead to low complexity and a low power design well suited for low data rate communication applications[5]. In the case of IR-UWB, no carrier is used to up/down-convert the signal resulting in even simpler implementation. The main disadvantage of this system is the difficulty in controlling the exact shape of the impulse, and consequently the overall frequency response[8].

CMOS technology has gained a great deal of attention because of its high integrity and low cost. Nowadays, deep submicron CMOS devices have cutoff frequency in the 100 GHz range. The parasitic capacitances of the devices are very small such that it makes it possible to implement the UWB system in CMOS technology. In this paper, a 3–5 GHz fully integrated low power amplitude and spectrum tunable IR-UWB transmitter is designed in 0.13 μm CMOS technology. In section 2, the circuit implementation of this transmitter is introduced. Section 3 shows the measurement results. Lastly, a conclusion is given.

2. Circuit implementation

The transmitter consists of only three blocks, the pulse generator, the output buffer and a power control block, as shown in Fig.1.

2.1. Pulse generator (PG)

Basically, there are two categories of pulse generators: the analog pulse generator and the digital pulse generator. In Ref.[6], an analog pulse generator is designed employing the square and exponential functions of transistors biased in saturation and the weak inversion region, respectively. The main disadvantage of this method is that the amplitude of the output pulse is very small; a wideband amplifier is thus needed. The basic concept of the digital pulse generator is to combine the edges of a digital signal and its inverted signal to form a very short duration pulse, and then a differential circuit

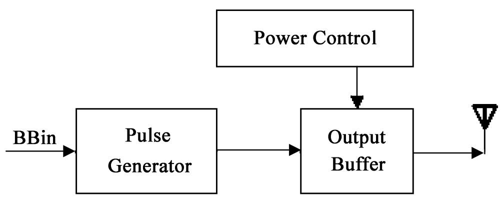

Fig.1. IR-UWB transmitter.

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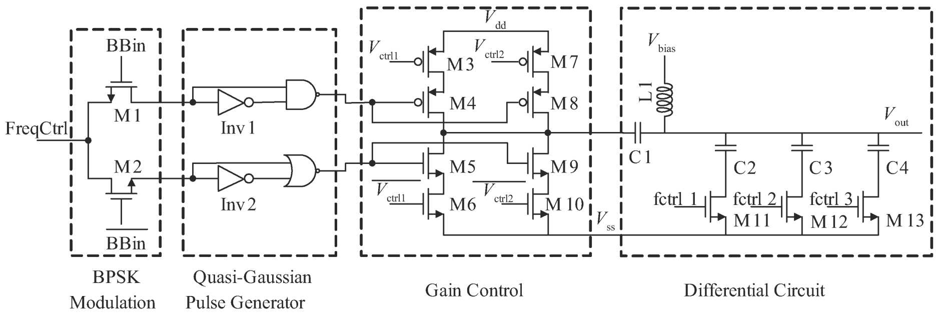

Fig.2. Pulse generator.

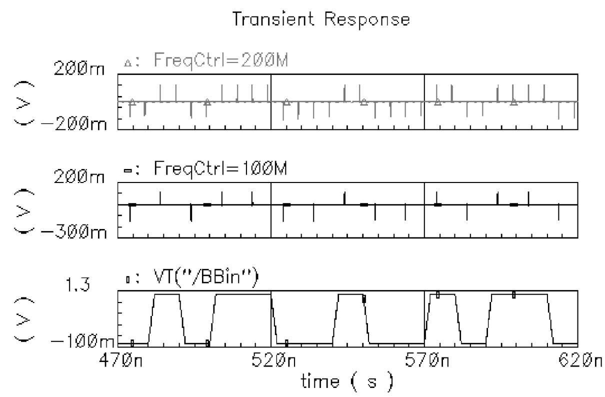

Fig.3. Number of impulses per bit can be controlled by FreqCtrl.

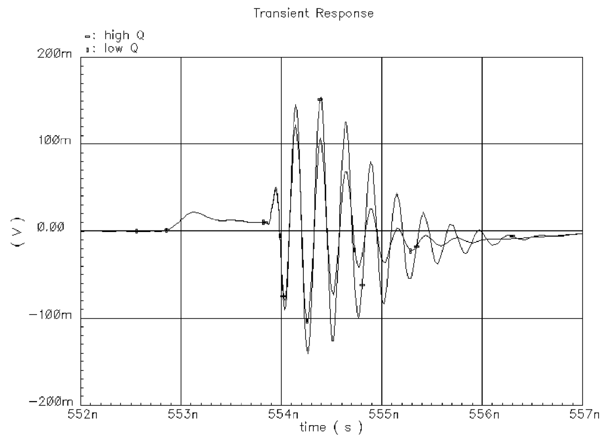

Fig.4. Resonance response with different Q value.

is used to up-convert the signal. Except that, Reference [7] presents a novel way to up-convert the signal. Four pulses are combined successively to form a fifth derivative Gaussian pulse. This method eliminates the inductor used in the differential circuit which consumes the majority portion of the chip area. However, this method suffers from a lot of process variation. For all these pulse generators it is difficult to control the exact pulse shape and its spectrum. In this paper, an amplitude and spectrum tunable pulse generator is designed to solve this problem. And since this pulse generator only consists of digital and passive circuits, the power consumption is very low.

2.1.1. BPSK modulation and quasi-Gaussian pulse generator

Many types of modulations can be used in impulse based UWB systems, such as OOK, PPM, BPSK, etc. BPSK has an advantage over the other types of modulations due to an inherent 3 dB increase in separation between constellation points[9].

In Fig.2, BBin is the baseband input signal. When BBin is high, the upper path is selected and a positive pulse is generated by NAND; otherwise, the lower path is selected and a negative pulse is generated by NXOR. FreqCtrl is a rectangle signal that determines how many pulses are to be formed in one bit of BBin. As shown in Fig.3, the baseband inputs a signal of 100 MHz, when the frequency of FreqCtrl signal is 100 MHz, the quasi-Gaussian pulse generator outputs one impulse per bit; when the frequency of FreqCtrl is 200 MHz, there are two impulses per bit. By transmitting several impulses for one bit of information, the SNR can be enhanced [10]; however, the power consumption will also increase.

2.1.2. Gain control

Transistors of M3–M10 are used to control the amplitude of the output impulse. The sizes of M3-M4 (M5-M6) are twice the sizes of M7-M8 (M9-M10), so a 3-step gain control is realized by applying “1” or “0” to V_{ctrl1} and V_{ctrl2}. The measurement results indicate that the peak-to-peak voltage swings of the impulses are 240, 170 and 115 mV on an output termination resistor of 50 Ω.

2.1.3. Differential circuit

Inductor L1 and the gate parasitic capacitance of transistor M14 of the output buffer compose an under-damped resonance network to up-convert the impulse signal. An under-damped response is characterized by an exponentially decaying sinusoidal waveform. The quality factor Q of the inductor needs to be designed carefully. A high Q indicates low damping and a long decaying time, as shown in Fig.4. A 4-step frequency tuning is realized by switching M11–M13 on/off to compensate for the process, voltage and temperature (PVT) variations. The center frequency tuning range is 3.2–4.1 GHz.

2.2. Output buffer

Since the transmitted power of the UWB is very low, the power amplifier is optional in the transmitter. In this paper, an output buffer is implemented to drive the antenna. As shown in Fig.5, the cascade structure is employed to improve the input-output isolation. R_2 is the input impedance of the

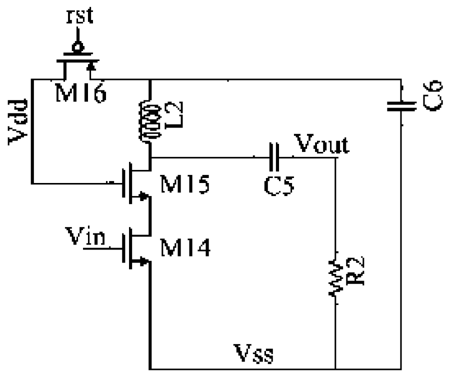

Fig.5. Output buffer.

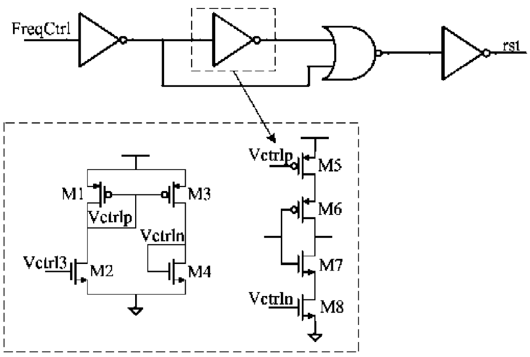

Fig.6. Power control circuit.

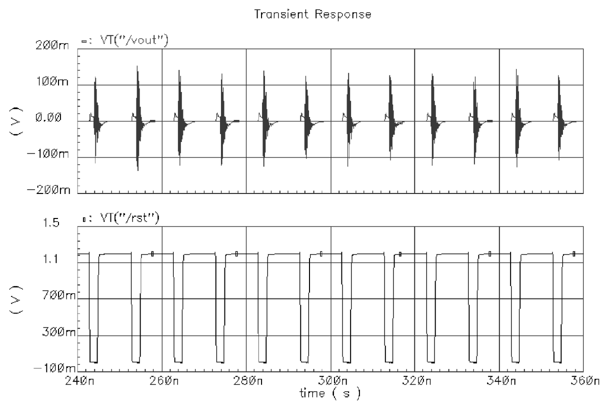

Fig.7. Transient simulation of rst.

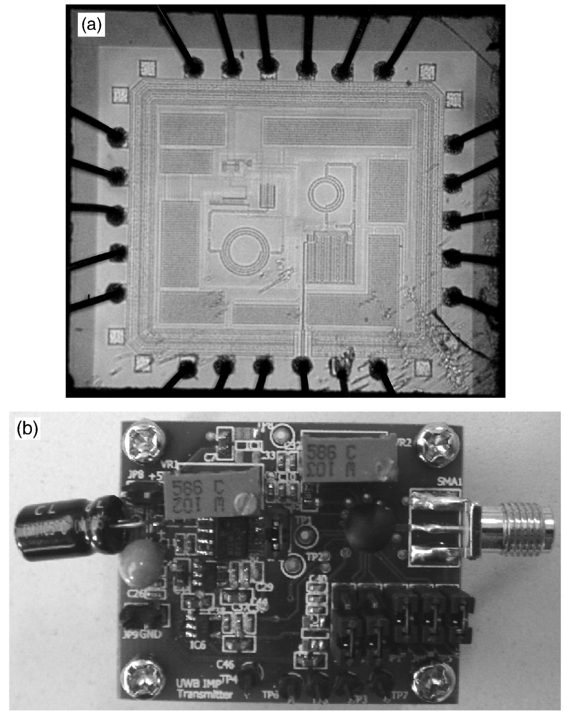

Fig.8. (a) Die photomicrograph and (b) PCB of transmitter.

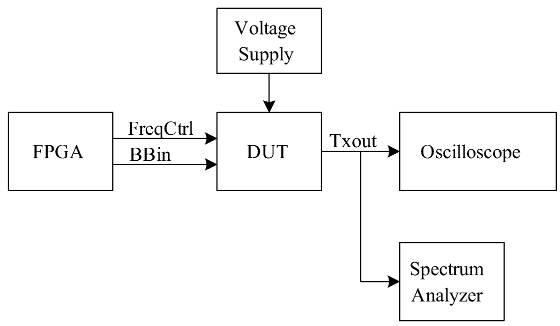

Fig.9. Transmitter test scheme.

antenna, which is 50 Ω in the UWB operating frequency range. Unlike in traditional narrowband systems, the Q of inductor L_2 should be low enough to have wide frequency band selectivity. Since the signal of IR-UWB is inherently duty-cycled, the output buffer can be disabled during the intervals between impulses. Transistor M16 is a large scale pMOS switch; the gate control signal rst is used to turn the switch on/off, hence low power design is realized. Capacitor C_6 is used to suppress the unnecessary pulse generated by switching on/off.

2.3. Power control

A power control block is used to generate the rst signal for the output buffer. The circuit of the power control block is shown in Fig.6. The structure of the inverter in the dashed block is shown below. M5 and M8 are used to control the charging or discharging current, thus controlling the delay time of the inverter. The biasing circuit is also shown in Fig.6. From the simulation result in Fig.7, we can see that when an impulse is generated, the voltage of rst is low, which makes M16 in Fig.5 switched on; when there is no signal during the impulses intervals, the voltage of rst is high, thus M16 is switched off.

3. Measurement results

The proposed IR-UWB transmitter is implemented in 0.13 μm 1P8M CMOS technology. The die photomicrograph and PCB test board of the transmitter are shown in Fig.8. The die area is 1.2×1.4 mm^2. The total power consumption of the transmitter is only 2.4 and 4.44 mW with a supply voltage of 1.2 V when transmitting 50 and 100 MHz baseband signals, respectively.

The test scheme is shown in Fig.9. XinlinxVC2VP30 that has a system clock of 100 MHz is used to generate the baseband and the FreqCtrl signals. The output of the transmitter is measured with Tektronic TDS 6604 and Agilent E4440A in time and frequency domain, respectively.

The measured time domain waveform is illustrated in

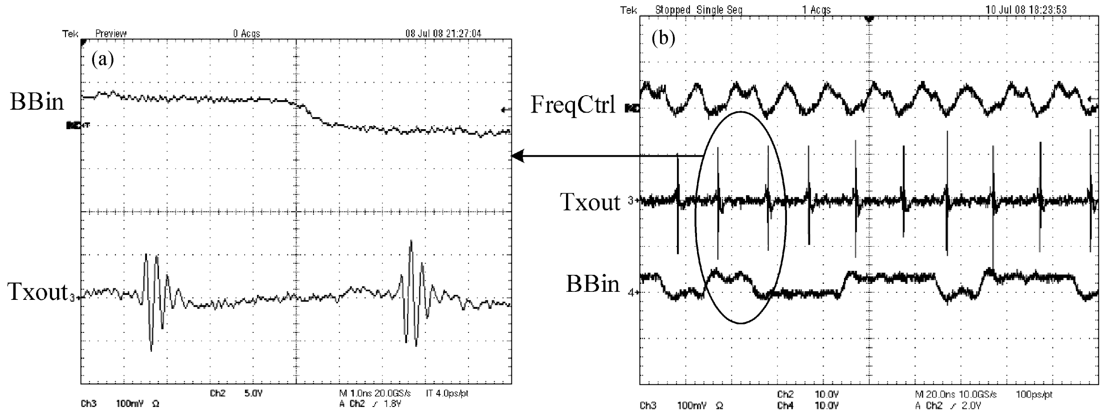

Fig.10. (a) Two enlarged BPSK modulated impulses; (b) Measured impulses with a data rate of 50 MHz.

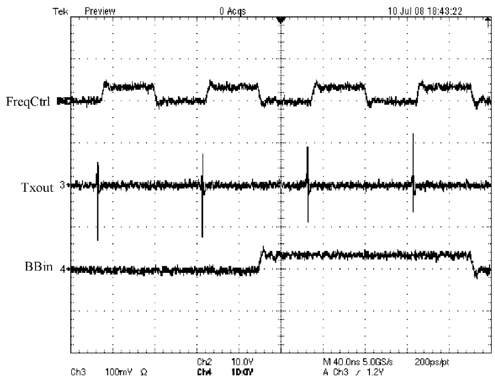

Fig.11. Two impulses per bit.

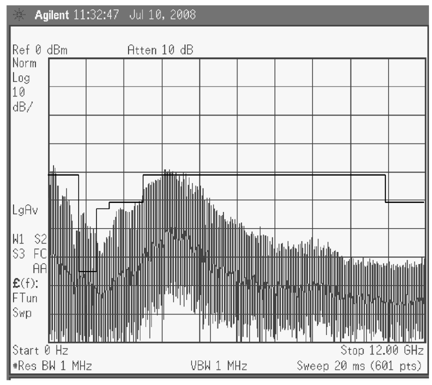

Fig.12. Power spectral density of transmitter.

Table 1. Summary of transmitter performance and comparison.

Reference	[7]	[11]	[12]	[13]	This work
Frequency band (GHz)	3–5	3–5	3–10	3–5	3–5
Modulation	PPM	PPM	BPSK+PPM	OOK	BPSK
Max data rate (MHz)	400	16.7	1800	100	100
Pulse width (ns)	2	/	0.3	1.4	1
Pulse amplitude (mVpp)	200	/	220	400	240
Power consumption (mW)	76	0.72	129	14	4.44
pJ/bit	190	43	126	140	44.4
Technology	CMOS 0.18 μm	CMOS 90 nm	CMOS 90 nm	CMOS 0.18 μm	CMOS 0.13 μm
Die area (mm^2)	2.6×1.7*	0.2×0.4	2.83	25×10**	1.2×1.4

* Die area of transceiver

** Package area of transceiver

Fig.10 (b), where the data rate (BBin) is 50 MHz. Figure 10 (a) shows two enlarged BPSK modulated impulses. The pulse width is 1 ns, and the peak-to-peak amplitude is 240 mV. Figure 11 shows the situation when the frequency of FreqCtrl is twice the data rate of BBin. As we can see each bit of the baseband signal generates two impulses, thus the SNR is enhanced by 6 dB.

The measured power spectral density (PSD) with FCC mask when transmitting 50 MHz baseband data is shown in Fig.12. The spectrum is centered at 4 GHz with maximum PSD of −40 dBm/MHz. The 3–5 GHz PSD is compliant with the FCC mask. The low frequency energy in the spectrum is contributed by the switch in the output buffer. It distributes out of the UWB band and can be easily removed using a high pass filter. By changing the control bits in a differential circuit, the center frequency can be tuned from 3.2 to 4.1 GHz.

A summary of the measured results and a comparison with previously published papers is shown in Table 1.

4. Conclusion

A low power, low complexity carrier-less IR-UWB transmitter has been introduced. The proposed transmitter is amplitude and spectrum tunable, thus the problem of spectrum control can be solved. The pulse generator only consists of digital and passive circuits, and the output buffer can be turned off during the intervals between impulses, thus low power design is realized.The power consumption is only 4.44 mW with the data rate of 100 MHz. However, the switch in the output buffer introduces low frequency energy in the spectrum, and thus a filter is needed.

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