A 3.1–4.8 GHz CMOS receiver for MB-OFDM UWB*

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Abstract: An integrated fully differential ultra-wideband CMOS receiver for 3.1–4.8 GHz MB-OFDM systems is presented. A gain controllable low noise amplifier and a merged quadrature mixer are integrated as the RF front-end. Five order Gm-C type low pass filters and VGAs are also integrated for both I and Q IF paths in the receiver. The ESD protected chip is fabricated in a Jazz 0.18 μm RF CMOS process and achieves a maximum total voltage gain of 65 dB, an AGC range of 45 dB with about 6 dB/step, an averaged total noise figure of 6.4 to 8.8 dB over 3 bands and an in-band IIP3 of –5.1 dBm. The receiver occupies 2.3 mm^2 and consumes 110 mA from a 1.8 V supply including test buffers and a digital module.

Key words: ultra-wideband; MB-OFDM; radio frequency; low noise amplifier; quadrature mixer
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1. Introduction

As an emerging technology for high speed wireless personal area network (WPAN) communications, the ultra-wideband (UWB) systems enable data rate up to 480 Mbps or even higher within 2–10 m distance by occupying a very wide frequency spectrum from about 3.1 to 10.7 GHz. Recently, the multiband orthogonal frequency division multiplexing (MB-OFDM) has been supported as the most competitive UWB solution ready for a wireless USB, a higher version of Bluetooth and so on. By dividing the UWB spectrum into several sub-bands each of 528 MHz while adopting frequency hopping among these bands in combination with OFDM modulation (see Fig.1), the multi-path effect and narrowband interferences are relaxed while achieving high data rate. The first 3 bands ("mode 1") from 3.168 to 4.752 GHz are now under research and development, in which the carrier frequencies are 3.432, 3.96 and 4.488 GHz, respectively[1].

Considering the experimental principle that RF circuits' working frequencies are limited no higher than $(1/5)f_{\rm T}$ – $(1/10)f_{\rm T}$[2], a 0.18 μm CMOS process with about 40 GHz cut-off frequency ($f_{\rm T}$) is required at least for the Mode-1 UWB design. Many advanced CMOS or SiGe technologies below 130 nm are expected for future full-band UWB since their $f_{\rm T}$ are well above 80 GHz or even higher. This paper describes the realization of an MB-OFDM UWB receiver covering 3.1–4.8 GHz bands in a low cost 0.18 μm CMOS process. Firstly, the receiver specification and architecture are analyzed. Then the RF front-end design including LNA, mixer and LO buffers is described. The intermediate frequency (IF) low pass filter and variable gain amplifier (VGA) are also introduced.

2. Receiver specification and architecture

As shown in Fig.2, the UWB wireless receiver employs direct-conversion architecture and locates behind the antenna and pre-filter. The received weak UWB signals are amplified and converted to IF baseband, and after further filtering and amplifying, the analog baseband signals should be large enough to drive the ADC for digital signal processing. This paper will mainly focus on the designs and implementations of the blocks between the dashed lines in Fig.2 and the quadrature local oscillator (LO) generator is not included.

The existing MB-OFDM standard[3] requires a receiver sensitivity of –70.4 dBm for 480 Mbps rate and the differential input peak-peak full scale voltage is 0.64 V (0 dBm in 50 Ω system) for the subsequent ADC. The voltage chosen here is reasonable for an ADC in the same silicon technology with 5-bit resolution and 528 MSps sampling rate or above, and it is convenient to realize a total SoC solution for UWB. Taking into account of the 6 dB peak–to-average ratio (PAR) for OFDM signals, the required total voltage gain is larger than 65 dB. Besides, the receiver should have an AGC range of more than 40 dB in case of maximum UWB signal apart from another UWB device within 0.2 m. The noise figure is required to be as good as possible to optimize the signal-to-noise ratio (SNR), and is set to be 7–8 dB for the 0.18 μm CMOS process. To survive in strong in-band signals and out-band interferences environment, the input referred 3rd intercept point (IIP3) and 1 dB gain compression point (1dBCP) should be better than –9 and –23 dBm, respectively[4]. The IF baseband frequency is from 4.125 to 264 MHz, and the spectrum fraction near DC is abandoned to avoid flicker noise and DC offset[1]. To effectively reject the out-band interferers, the filters should provide

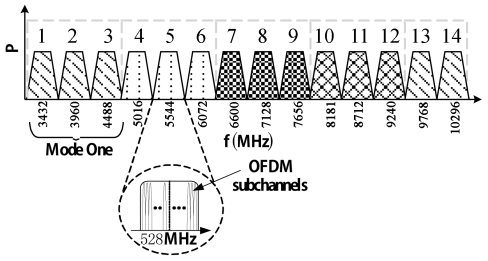

Fig.1. Spectrum planning for an MB-OFDM UWB.

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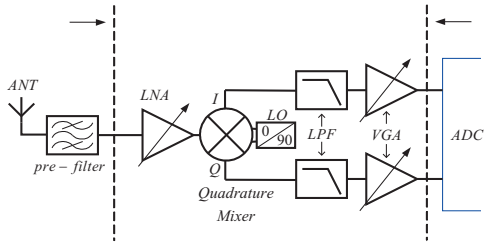

Fig.2. UWB receiver architecture.

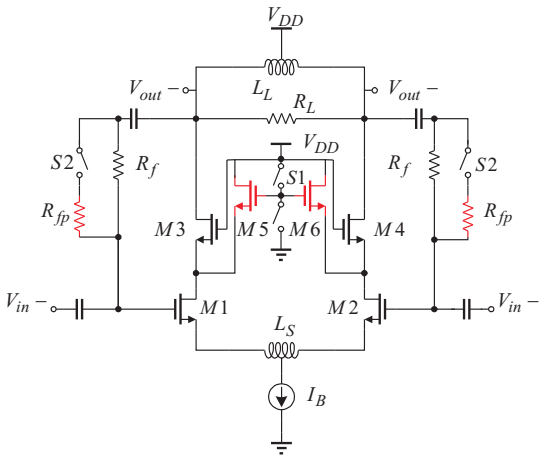

Fig.3. P roposed gain controllable LNA.

at least 40 dB attenuation at 600 MHz.

To meet the requirements proposed above, design emphases for modules are considered as below. The RF front-end provides changeable gain with low noise and moderate conversion gain. The filters and VGAs should have good linearity and frequency response.

3. RF front-end design

3.1. Low noise amplifier

The main target of the LNA design is to enable the gain controlling without affecting the noise figure and input matching. The adopted circuit is based on the resistive shunt feedback topology, which achieves a wideband matching with a good balance between area cost and performances, although there is a slight degradation of the noise figure comparing to other techniques like LC ladder[5] and transformer feedback matching[6], which always use quite a large number of inductor coils.

As shown in Fig.3, resistors (R_f,) are placed between the drain of the cascode transistors (M3,M4) and the gate of main amplifying transistors (M1,M2,) to provide an AC feedback path. The source degeneration inductor (L_S) is differential to save the area. These elements build up the input matching network together with the bond wires and parasitic capacitances. The controlling switch (S1) of current bypassing transistors (M5,M6) is set to be zero when high gain is needed and high in low gain mode. Compensating resistors (R_{fp},) controlled by switch S2 are connected in parallel with R_f to improve the input matching in low gain mode. The output of the LNA is loaded by a differential inductor (L_L,) and a shunt resistor (R_L,).

As illustrated in Fig.4, if the bondwire is ignored, the circuit can be represented by a feedback loop with a G_m

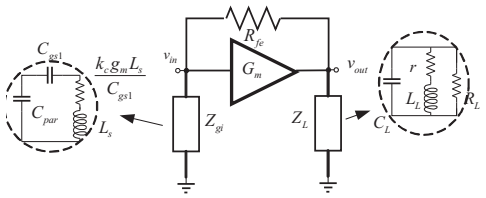

Fig.4. A simplified representation of the LNA.

amplifier, an effective feedback resistor (R_{fe}), an input network (Z_{gi}) and an output network (Z_L). The load capacitors including the subsequent mixers' gate-source capacitors are assumed to resonate with the load inductors at the same frequency as the input network. Thus, a simplified expression of the gain at the resonance frequency ω_0 can be solved by

$$A_v = -(1 + \frac{sQ_{in}}{\omega_0})\frac{k_c g_m}{1 + k_c g_m L_s s}(R_{fe} \parallel R_L \parallel rQ_L^2), \qquad (1)$$

where r is the series resistance of the inductor, Q_{in} is the quality factor of the input network, Q_L is the inductor's quality factor, g_m is the transconductance of M1 and M2, and $k_c = W_{3,4}/(W_{3,4} + W_{5,6})$ is named as the current bypassing factor and depends on the proportion between the width of M3,M4 and M5,M6. It is easy to find that the gain depends on k_c and Figure 5(a) shows the effect of different k_c on gain.

It should be noted that the input network is partly related to k_c (seen in Fig.4) and R_{fe}. If R_{fe} is a constant, the real part of input impedance will vary with k_c and no longer matching in the other gain mode. So, R_{fp} is introduced to the feedback loop to compensate for the input matching. If $k_R = R_{fp}/(R_{fp} + R_f)$ is represented as the feedback compensation factor, a simulation of different (k_c, k_R) pairs is shown in Fig.5(b). Comparing the curves of (1,1) and (0.46,0.6), it is obvious that the real impedance could be compensated for tremendously.

The output noise is mainly contributed by channel noise of M1 and M2, thermal noise of feedback resistors. Mathematical analyses indicate that increasing the transconductances of M1, M2 and the feedback resistors will reduce the noise figure, but care should be taken to balance the impedance matching. The k_c also influences the noise figure reversely but it is not important since the signals are big enough to provide good SNR when k_c drops (low gain in other words).

The LNA is simulated in 18 mA biasing current and achieves 14–16 dB gain and 3–4 dB noise figure in the 3.1–4.8 GHz UWB band in high gain mode, the high-to-low gain drop is about 10 dB. The input return loss is similarly better than –10 dB in both gain modes.

3.2. Quadrature mixer

The purpose of exploring merged architecture for the quadrature mixer is to minimize the capacitive loading to the LNA. The load inductance (L_L) has to be decreased to keep the resonance frequency around 4 GHz if the capacitive load is too large, subsequently the load resistor (R_L) has to be smaller to maintain the gain flatness, resulting in degraded gain and noise figure.

The merged quadrature mixer adopted in the design is shown in Fig.6. Two identical switching units (MI3–MI6, MQ3–MQ6) share the same RF transconductance stage (MT1,MT2), the LO signals are quadrature, generating

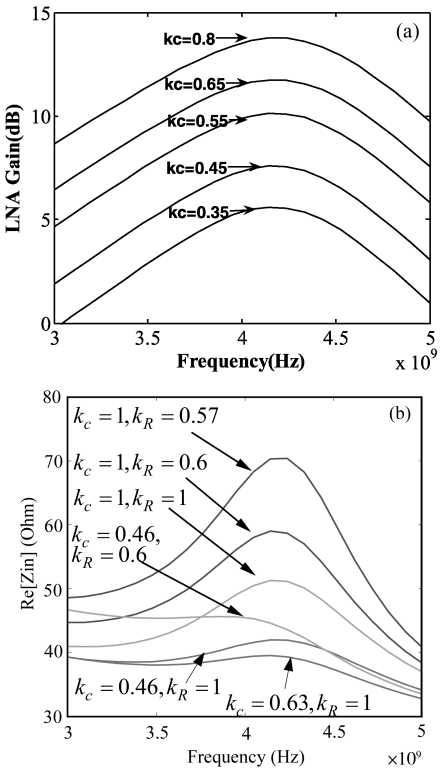

Fig.5. (a) Simulation of the LNA gain with k_c from 0.35 to 0.8, while the k_R is 1; (b) Simulated input real impedance with different (k_c, k_R) pairs. Note that $k_R = 1$ corresponds to no feedback resistance compensation and $k_c = 1$ corresponds to no current bypassing.

differential IF signals in I and Q. The same static currents (I_F) are injected in every common-source nodes of the switching stages. As a result, the load resistors can be big enough to improve the conversion gain and noise figure while keeping all the transistors in saturation region. Another benefit is that the flicker noise of switching transistors could be suppressed in IF outputs[7]. Since the constant current injection shows high impedance for small signals, the conversion gain will not vary with injections. An expression of the voltage conversion gain is given by

$$A_{\mathrm{v,Quadrature}} = \frac{1}{\pi} g_{\mathrm{m,RF}} R_{\mathrm{L}}, \tag{2}$$

where $g_{\mathrm{m,RF}}$ is the transconductance of MT1,MT2, and R_{L} is the IF load resistor. Compared to the conventional Gilbert mixer, the quadrature mixer provides a half of the gain of Gilbert mixer. But under a doubled biasing current, the merged configuration can provide the same gain while using smaller transistors, the load of the LNA is reduced consequently.

The mixer is optimized to provide enough gain using smaller transconductance transistors with a noise figure and linearity no worse than the Gilbert topology. The mixer is biased in 8.3 mA current.

The LO signals for the mixer are applied externally and two common-source unit-gain amplifiers are designed to buffer the LO signals. The buffers consume approximately 9 mA current in total.

Combining the LNA and quadrature mixer, the RF front-end achieves 23–25.5 dB gain and 4.5–5.5 dB noise figure over three bands of interest in the high gain mode. Simulated IIP3 is better than −4.3 dBm in the low gain mode.

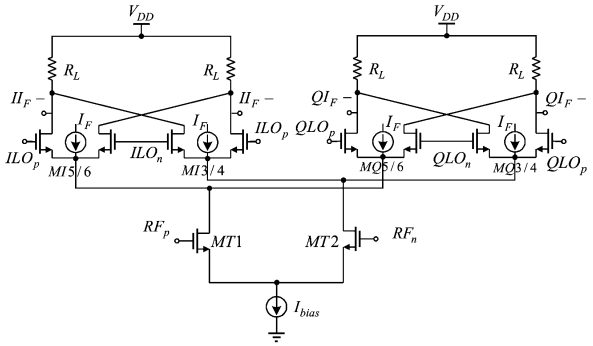

Fig.6. Simplified schematic of the quadrature mixer.

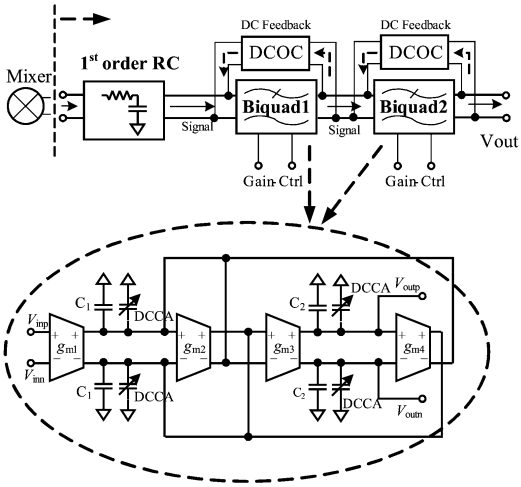

Fig.7. LPF and biquad structure.

4. Low pass filter and VGA

4.1. Gm-C type low pass filter

The filter adopts 5th order Chebyshev approximation and Gm-C biquad architecture as shown in Fig.7. Note that the down-conversion mixer's load resistors are utilized to form the first passive RC filter stage. As a result, simulations covering both mixer and filters should be taken to make sure that the overall frequency response and gain are optimized. The following active filter stages are Gm-C type biquads. Since the operational transconductance amplifiers (OTAs) in Gm-C biquads are operating in open loop mode, much higher frequency response can be achieved but the linearity may be degenerated. Therefore, a pseudo differential topology which gets rid of the harmonics due to the non-ideal tail current source[8] is utilized in the OTAs to improve the linearity. To suppress the common mode gain and stabilize the output common mode voltage, common mode feed-forward (CMFF) and feed-back (CMFB) circuits are used in the pseudo differential OTAs. As shown in Fig.8, M1–M4 the are input stage, M9–M12 form the basic pseudo differential OTA, M5–M8 extract the common mode component of the input signal (i_{com}) and feedforward to the OTA, M13–M18 provide CMFB, and node V_{x} connects to previous stage's CMFB output.

Since the filter capacitors are of pFs in value to be insensitive to parasitic capacitances, the transconductance of the OTA is about 2 mS consequently. The lengths of the input and output transistors of the OTA are chosen to be 350 nm to make a tradeoff of the parasitics and OTA GBW. The override voltage of the input transistors is 300 mV to balance the linearity

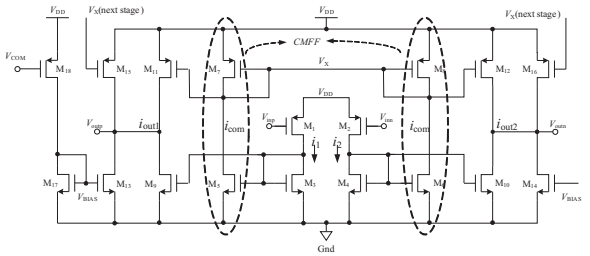

Fig.8. Pseudo differential OTA used in the LPF.

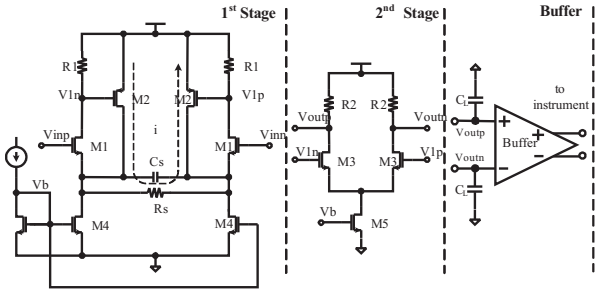

Fig.9. VGA circuits and buffer configuration.

and power consumption.

Because the filter requires 264 MHz cutoff frequency and 40 dB attenuation at 600 MHz with less than 1 dB in-band ripple, the filter approximation is chosen to be 5th order Chebyshev. In detail, a 1st order passive low pass filter with 118 MHz 3 dB-corner and two low pass biquards with 198 and 283 MHz 3 dB-corners combine together (see Fig.7). The latter two biquads' Q factors are 1.036 and 3.876, respectively. The frequency corners of the filter can be adjusted by the digitally controlled capacitor arrays (DCCA). The biquads' gain can also be digitally controlled by changing the g_{m} stage in the biquads. DC offset calibration (DCOC) circuits are introduced to the filter to reject the DC offset due to device mismatch. During calibration, static voltages on both positive and negative output nodes of the biquad are sampled and compared, the results are feedback to the previous stage's current source in current. As a consequence, the filter's attenuation from DC to 4.125 MHz is achieved simultaneously since the DCOC is equivalently a high pass filter with 4 MHz corner frequency.

The filter's corner frequency can be coarsely tuned from 185 to 370 MHz and finely tuned near 264 MHz by DCCA. Each biquad's gain is initially fixed to 0 dB and increases up to 12 dB by 6 dB per step. Therefore, the total gain of the filter is from 0 to 24 dB.

4.2. VGA design

The VGA in this design is realized by a two-stage amplifier, which is demonstrated in Fig.9. The first stage adopts transconductance-enhanced source degeneration architecture to reach higher linearity. The second stage is a common-source amplifier to promise enough gain. DCOC circuits which are identical to those in filters are also used here (not shown in Fig.9). The VGA is followed by a test buffer which drives the low impedance instrument.

As the input and output signals of the VGA is relatively large, a good linearity is required for the amplifiers. The feedback PMOS transistors M2s in the first stage keep the gate-source voltage of M1s more constant, therefore, the small signal current only flows through resistor R_{S}. As a result,

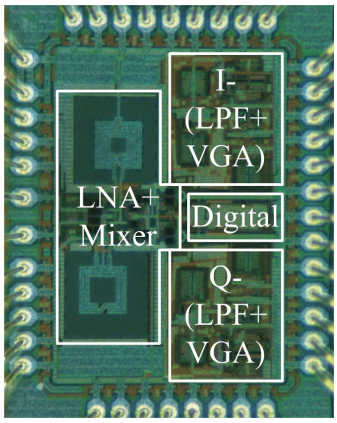

Fig.10. Chip photograph.

the effective transconductance of the first stage is roughly $1/R_{\mathrm{S}}$ which dose not depend on the input. A capacitor (C_{S}) in parallel with the resistor adds a zero to compensate for the high frequency response, expanding the bandwidth of the amplifier[9]. The override voltage of M3s in the second stage is set larger to optimize the linearity. The amplifier gain varies through adjusting the source feedback resistor (R_{S}) in the first stage, C_{S} should be changed synchronously to keep the gain flatness since the zero-pole position may vary with gain.

The lengths of main amplifying transistors in the first stage are chosen to be twice the minimum transistor length to reduce device mismatch and those in the second stage are even longer to enlarge output impedance. The VGA's fixed gain is 6 dB and increases by 18 dB for one step.

The bias current is 16.5 mA for each single LPF and 8.5 mA for a VGA. IF test buffers consume 10 mA current in total.

5. Implementation and measurements

The proposed UWB receiver is fabricated in the Jazz 0.18 μm 1P6M RF CMOS process. All pads are ESD protected with HBM ESD tolerance of 1.36 kV. The chip die covers an area of 1.3×1.7 mm^2 including pads, and its photograph is shown in Fig.10. To reduce the logical signal pads, a serial register is embedded in the receiver to translate serial data into parallel to set all controlling bits in LPFs and VGAs. The register is controlled by PC through an MCU out of the chip. As a result, the total number of pads for digital controlling shrinks to only three and the receiver layout is greatly simplified. The chip is directly bonded on a PCB test board.

Figure 11 shows the experimental results of the RF port input return loss (S_{11}) at both LNA high gain and low gain modes. There are two reasons to result in the S_{11} curves being unexpectedly above –10 dB in lower UWB bands. One is the inaccurate modeling of bond wires. The other may be the unmatched characteristic impedance of the signal trace on the PCB board, which cause the measured real impedance much lower than 50 Ω below 4 GHz. But the similarity of the curves at two modes implies that the input matching compensation design of the LNA works well. The overall noise figure is measured using a Agilent$^{\mathrm{TM}}$ E4440A Spectrum Analyzer and 346C Noise Source. The noise figure versus IF frequency offset in 3 bands is shown in Fig.12. It achieves lower than 6 dB

Table 1. Results summary and comparison with previously published designs.

	Ref.[4]	Ref.[10]	Ref.[11]	Ref.[12]	This work
Technology	0.13 μm CMOS	0.25 μm SiGe	0.13 μm CMOS	90 nm CMOS	0.18 μm CMOS
Freq. range (GHz)	3.1–4.8	3.1–4.8	3.1–4.8	3.1–9.5	3.1–4.8
Max. gain (dB)	69–73	59	37	58.7–64	62–65
Noise figure (dB)	6.5–8.4	4.7–5.7	4.1	6.3–7.8	6.4–8.8
IIP3 (dBm)	n/a	−6**	2	-17	-5.1/7^{+}
Power (mW)	1.5×70/105	2.5×78/195	237	1.1×203/224	1.8×90/162^{++}
Total area (mm^2)	1.0*	4	6.6	3.5	2.3

Notes: * without pads; ** out-band results; $^{+}$ in-band and out-band results respectively; $^{++}$ without LO generation.

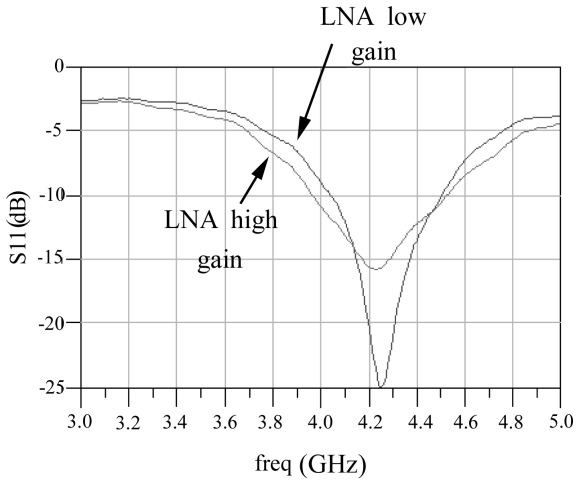

Fig.11. S_{11} of LNA RF input port .

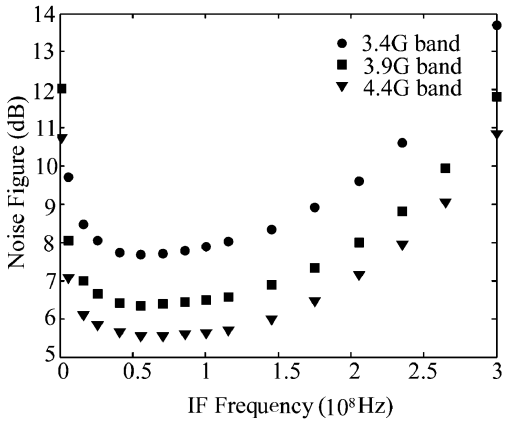

Fig.12. Noise figure at 3 bands.

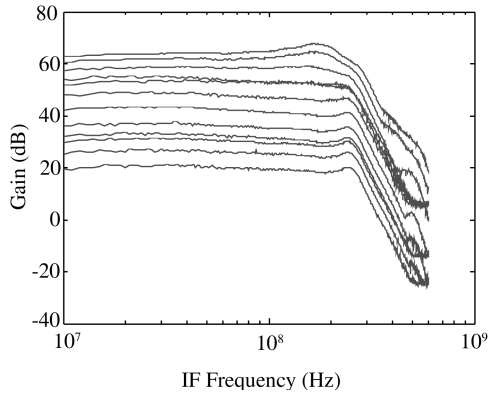

Fig.13. Total receiver gain at 3.96 G-band.

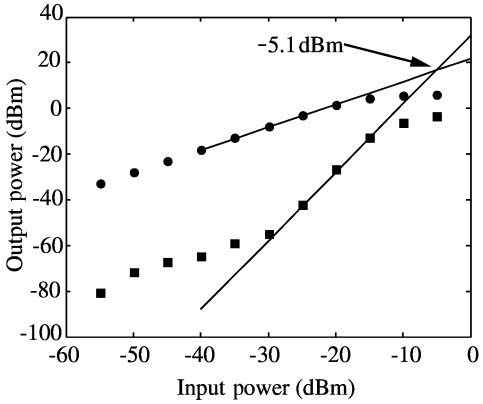

Fig.14. In-band IIP3 test result.

in 3.96 G-band and rises to higher than 8 dB in 3.432 G-band due to the imperfect LNA input matching. The degradation at higher IF offset is due to the poor noise suppression of the first biquad stage in filters. Therefore, averaged noise figures are computed to be 6.4, 7.3, and 8.8 dB for 4.488 GHz-band, 3.96 GHz-band, and 3.432 GHz-band, respectively.

The receiver gain is measured using the Agilent^{TM} E4440A and E4438C Vector Signal Generator by sweeping the input RF signal power. The measured total voltage gain in 3.96 G-band versus IF offset from 10 to 600 MHz is given in Fig.13 and the lower 4 MHz corner is not shown in this figure due to the limitations of the instrument. Some very close curves just correspond to different control bits for the same gain. It can be seen that the cutoff frequency is exactly 264 MHz and attenuation at 600 MHz is better than 45 dB. The gain varies from 20 to 64 dB, and the steps are 6 ±1 dB at lower gain modes and shrink to 4 dB at the highest three curves due to the signal saturation in output buffers. The maximum gains at three bands are 62, 64, and 65 dB, respectively which are smaller than those of the simulations, because the loading effect of DCCA in the first filter stage deteriorates the mixer gain. Keeping the 3rd harmonic (HD3) well below –50 dBc, the output differential amplitude can be larger than 600 mV, which enables driving the subsequent ADC.

The in-band IIP3 and 1 dB compression point at minimum gain are tested by applying a 2-tone or one-tone signal to the receiver input and the results are depicted in Fig.14. The out-band IIP3 test is done with 2-tone input at 5.2 GHz ISM band and 5.8 GHz UNII band when the receiver gain is about 50 dB, and the result is 7 dBm. The measured out-band IIP2 is 33.7 dBm with two tones of 5.8 and 2.4 GHz ISM bands at 50 dB receiver gain. The superior IIP3 and IIP2 performances guarantee that the receiver can survive in a strong interference environment. Under a 1.8 V supply voltage, the total current of the receiver changes from 105 to 115 mA (averaged to 110

mA) with the gain. If the LO and IF test buffers are not considered, the core consumes 90 mA only. The measurement results are summarized in Table 1 and some recently published works are also listed. Comparison shows that our receiver performances are competitive in a lower cost process.

6. Conclusion

An integrated fully differential RF receiver chip for 3.1–4.8 GHz MB-OFDM UWB applications has been presented. The chip meets most of the performance requirements for 480 Mbps data rate in a low cost 0.18 μm CMOS technology.

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