A 13-bit, 8 MSample/s pipeline A/D converter

Guo Dandan(郭丹丹), Li Fule(李福乐)†, Zhang Chun(张春), and Wang Zhihua(王志华)

(Institute of Microelectronics, Tsinghua University, Beijing 100084, China)

Abstract: A 13-bit 8 MSample/s high-accuracy CMOS pipeline ADC is proposed. At the input, the sample-and-hold amplifier (SHA) is removed for low power and low noise; meanwhile, an improved sampling circuit is adopted to alleviate the clock skew effect. On-chip bias current is programmable to achieve low power dissipation at different sampling rates. Particularly, drain-to-source voltages in the operational amplifiers (opamps) are fixed to ensure high DC gain within the variant range of the bias current. Both on-chip and off-chip decoupling capacitors are used in the voltage reference circuit in consideration of low power and stability. The proposed ADC was implemented in 0.18-μm 1P6M CMOS technology. With a 2.4-MHz input, the measured peak SNDR and SFDR are 74.4 and 91.6 dB at 2.5 MSample/s, 74.3 and 85.4 dB at 8.0 MSample/s. It consumes 8.1, 21.6, 29.7, and 56.7 mW (including I/O drivers) when operating at 1.5, 2.5, 5.0, and 8.0 MSample/s with 2.7 V power supply, respectively. The chip occupies 3.2 mm^2, including I/O pads.

Key words: analog-to-digital converter; pipeline; high-accuracy; sampling circuit; power programmable
DOI: 10.1088/1674-4926/30/2/025006 **EEACC:** 1265H

1. Introduction

With the rapid development of digital VLSI technology, wide applications of digital signal processing in wireless communication, asynchronous digital subscriber loop (ADSL) and high-speed imaging all require high-linearity, high-speed and low-power ADCs. Particularly, due to the rapid development of digital consumer electronics, low power design of ADCs becomes a concerned issue, considering the portability. In order to meet these increasing demands, ADCs with pipeline architecture become more attractive, because they can provide a good trade-off among the resolution, speed and power consumption[1].

In a typical pipeline ADC, the front-end sample-and-hold amplifier is often removed for low power[2, 3]. But in this case, the first pipeline stage has to sample the input signal directly, and the clock skew between the sampling circuit and the comparator circuit will inevitably induce a new frequency limitation of the input signal. Particularly, when the input signal exhibits a large slew rate, it can be the bottleneck to increase the input frequency. In this work, the SHA is removed for low power; meanwhile, the front-end sampling circuit is modified for wider input bandwidth.

In practice, ADCs are not always running at full speed. The ability to program the power consumption for a good power/speed ratio is also essential for a power efficient design. In this work, the ADC power is controlled by on-chip programmable current reference. And in order to achieve high accuracy, amplifiers are optimized to maintain high DC gain when the bias currents change. Both on-chip and off-chip decoupling capacitors are also used in voltage reference circuit for low power and stability issue.

2. Proposed ADC architecture

The proposed pipeline ADC architecture is shown in Fig.1. It consists of band gap, on-chip current/voltage references, clock generator, the first 6 passive capacitor error-averaging (PCEA) stages[2, 4, 5], the following 7-bit back end ADC, and some extra supporting circuit blocks.

PCEA is a kind of analog calibration techniques, with which the first-order gain error can be removed and a high accuracy can be obtained. The resolution of the 6 PCEA stages is 1.5 bit, which allows large correction range for comparator offsets. No calibration is applied to the backend 7-bit ADC, because the accuracy requirement of the later stages in pipeline architecture is much relaxed.

3. Circuit design

3.1. Improved front-end sampling circuit in the first pipeline stage

For low power and low noise, the conventional dedicated SHA is removed in this work. As a result, the input signal directly feeds into the two sampling paths in the first pipeline stage, which is shown in Fig.2. The passive SC path consists of sampling capacitors and switches, and the sub-ADC path consists of comparators and logic circuits. There is a crosstalk path between the two paths. Since the comparators in the sub-ADC are not so sensitive to the sampling disturbance, the sub-ADC path always samples slightly after the passive SC path. This means the input voltages processed by the two paths are not the same. Suppose the interval between $\Phi 1$ and $\Phi 2$ is Δt, and the resulting dynamic voltage offset between the two sampling paths is ΔV, as shown in Fig.2. When the input frequency

† Corresponding author. Email: lifule@tsinghua.edu.cn
Received 30 July 2008, revised manuscript received 9 October 2008

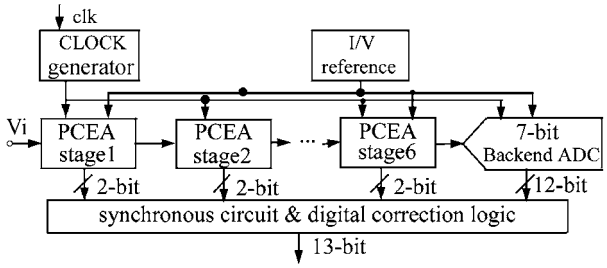

Fig.1. Proposed ADC architecture.

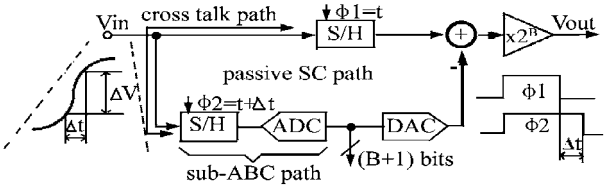

Fig.2. First pipeline stage without SHA.

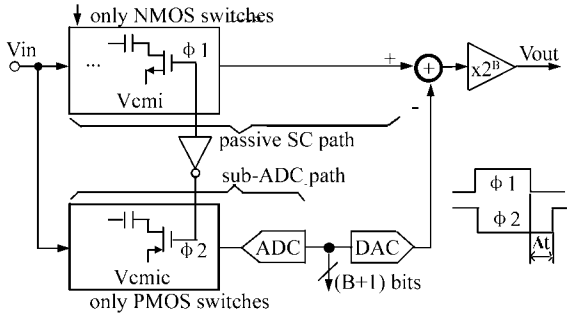

Fig.3. Improved front-end sampling strategy in the prototype ADC.

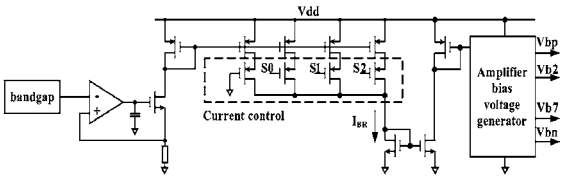

Fig.4. On-chip current reference.

increases, ΔV becomes larger and can ultimately result in a serious mistake in the first pipeline stage when it exceeds the digital error-correction range of the subsequent stages. To sum up, the interval Δt is necessary but should be as small as possible. Due to this Δt, a new frequency limitation is imposed on the input signal, which can be given by[3]

$$f_{\text{in}} \approx \frac{V_{\text{correction}} - \sum V_{\text{offset}}}{A2\pi\Delta t}, \tag{1}$$

where f_{in} is the input frequency, $V_{\text{correction}}$ is the digital correction range, ΣV_{offset} is the sum of comparator and interstage amplifier offset voltages, and A is the amplitude of the sinusoidal input. It is obvious that when other circuit parameters remain constant, the input frequency f_{in} is inversely proportional to Δt. Thus, decreasing Δt can effectively reduce the input frequency limitation.

Conventionally, Δt is achieved by the propagation delay of several inverters in cascade, typically 2 or 4 inverter delays. The improved sampling circuit in this work is shown in Fig.3. NMOS switches and PMOS switches are used respectively in the two different sampling paths, and as a result, Δt can be only one inverter delay. The frequency limitation is effectively reduced.

Furthermore, as indicated in Fig.3, the common voltage V_{cmi}, which is connected to NMOS switches in the passive SC path, is designed to be close to the ground, and the common voltage V_{cmic}, which is connected to PMOS switches in the sub-ADC path, is designed to be close to the power supply. This leads to smaller switch on-resistances, and the input bandwidth of each sampling path becomes wider, which is also helpful for the input bandwidth of the ADC.

3.2. On-chip current reference

The bias current of the proposed ADC is programmable for low power dissipation at different sampling frequencies. The programmable current reference is shown in Fig.4. The reference current I_{BR} is controlled by PMOS switches S_0, S_1 and S_2, which have different W/L ratios. Obviously, the bias currents of amplifiers change with I_{BR}. And finally, the ADC power consumption can be controlled.

3.3. Improved amplifier for variant bias current

In this work, a good power/speed ratio can be realized by adjusting the power consumption, which is controlled by programmable bias current. But the problem is that the DC gain and maximum output swing of the amplifiers will change with the bias currents. Thus, amplifiers need to be improved to treat this problem. As shown in Fig.5, folded-cascode with gain-boosting architecture is selected because of its high DC gain and large output swing. To adapt to variant bias currents, some new bias circuits are added to the gain-boosting stages. In gain-boosting 1, sources of transistors M1, M2 and M3 are all connected to node V_{mn}. And a new voltage equation rises, which can be given by

$$V_{\text{gs1}} \approx V_{\text{gs2}} \approx V_{\text{gs3}}, \tag{2}$$

where V_{gs1}, V_{gs2}, and V_{gs3} are the gate-to-source voltages of transistors M1, M2, and M3, respectively. The bias voltage V_{dcn} is designed to be constant when reference current I_{BR} changes, so the bias voltages at nodes n1 and n2 are also constant and equal to V_{dcn}. In the same way, the bias voltages at nodes p1 and p2 are constant and equal to V_{dcp} in gain-boosting 2. Thus, the drain-to-source voltages of transistors MN1, MN2, MP1, and MP2 in the cascode stage are almost constant and these transistors can operate in the saturation region within a large variation range of bias currents. In this way, the amplifier maintains high DC gain and constant output swing.

3.4. On-chip voltage reference

In the proposed ADC, which uses switch-capacitor technique, due to repeated charging and discharging operations, the reference voltages always include transient glitches and high frequency switching noise. To reduce these non-ideal factors, both on-chip and off-chip decoupling capacitors are used.

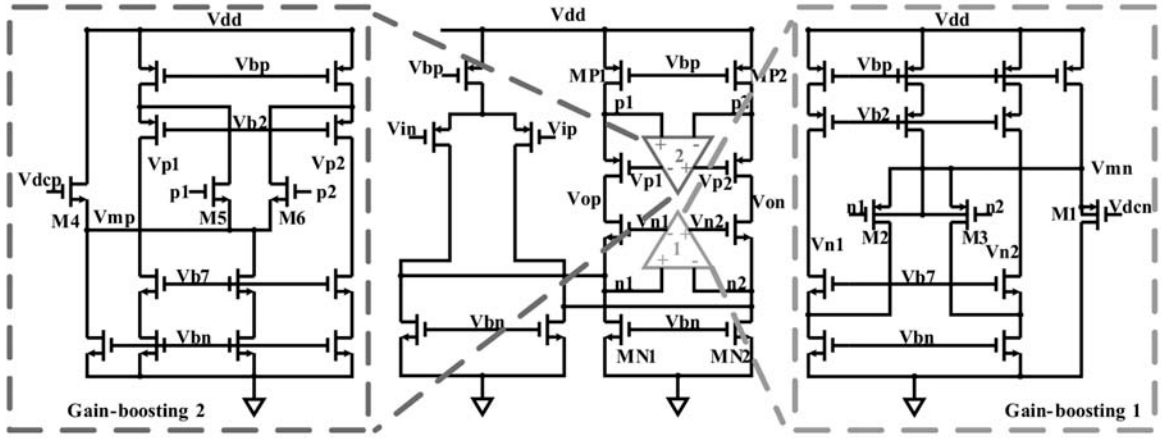

Fig.5. Improved folded-cascode amplifier with gain-boosting.

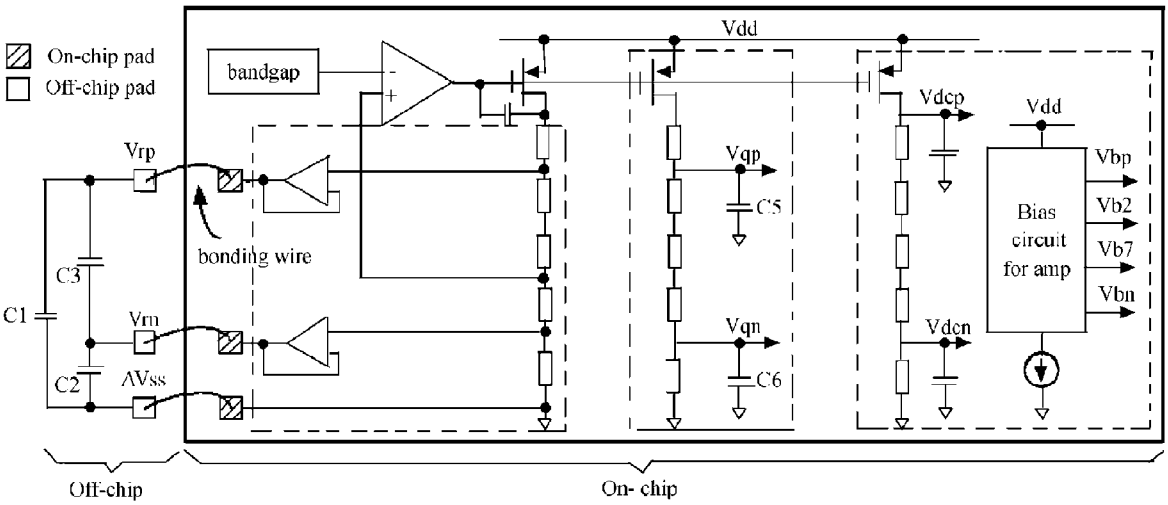

Fig.6. On-chip voltage reference.

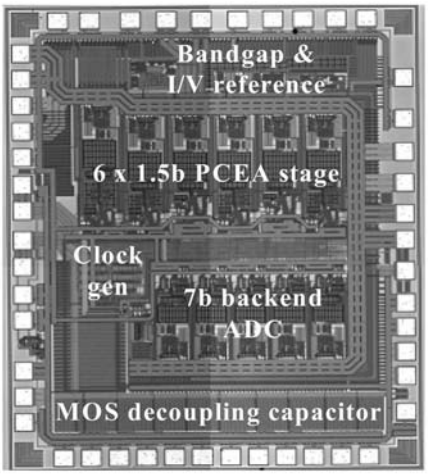

Fig.7. Die photo of the proposed ADC.

As shown in Fig.6, strings of resistors generate the reference voltages, which depend on the resistor ratio not the resistor absolute values. These reference voltages have the same stability as the bandgap reference, which are independent of the supply and temperature variations.

V_{rp} and V_{rn} are the reference voltages used in MDACs in pipeline stages, the accuracy and stability of which are significant for the ADC performance. Considering the potential LC resonant tank circuit, which is formed by the parasitic inductance related to bonding wires and the decoupling capacitors applied to V_{rp} and V_{rn}, the decoupling capacitors should be either very small or very large to set the resonant frequency at GHz-level or Hz-level to minimize the negative effect on the stability of V_{rp} and V_{rn}. In terms of power, noise, and chip area, large off-chip decoupling capacitors C_1, C_2 and C_3 at 0.5-μF level are used among V_{rp}, V_{rn} and the analog ground AVss to provide fast AC driving, while only small voltage buffers are used to supply DC driving current.

V_{dcp} and V_{dcn} are the bias voltages for the amplifiers. When the reference current I_{BR} changes, V_{dcp} and V_{dcn} are still constant, fixing the amplifier DC operational points within a reasonable range. V_{qp} and V_{qn} are the reference voltages applied to the comparators. Since the accuracy requirements of V_{qp} and V_{qn} are much relaxed in 1.5-bit stages, only on-chip decoupling capacitors are used to save pad.

4. Experimental results

The proposed ADC was implemented in the 0.18-μm 1P6M CMOS technology. The chip area, including I/O pads, is 3.2 mm^2, as shown in Fig.7. All the measurements were

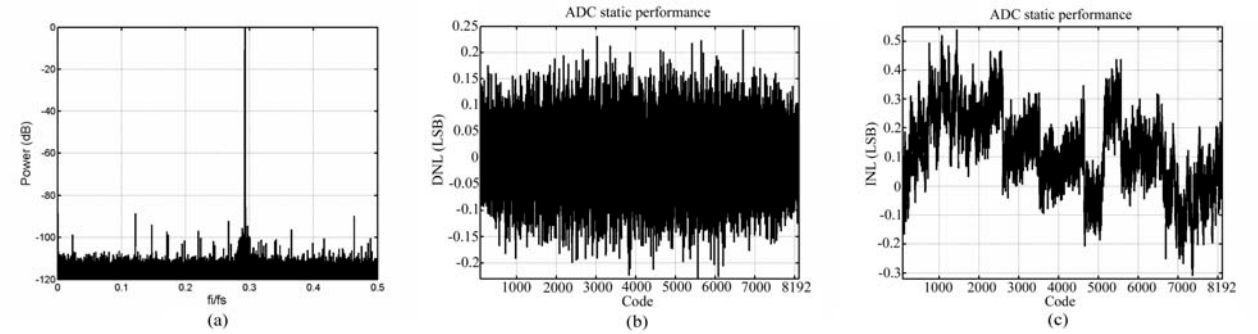

Fig.8. (a) Measured FFT spectrum @ f_{in} = 2.4 MHz, f_s = 8.0 MHz; (b) Measured DNL @ f_{in} = 2.4 MHz, f_s = 8.0 MHz; (c) Measured INL @ f_{in} = 2.4 MHz, f_s = 8.0 MHz.

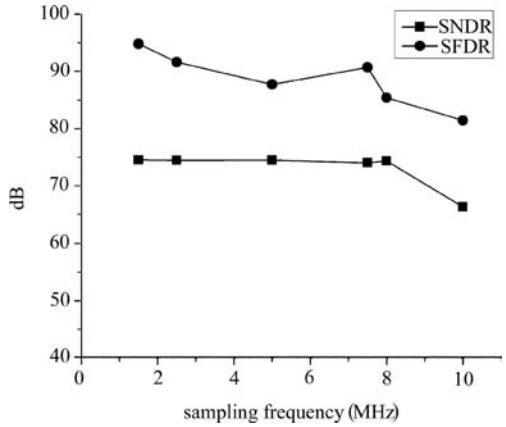

Fig.9. Measured SNDR and SFDR versus sampling frequency.

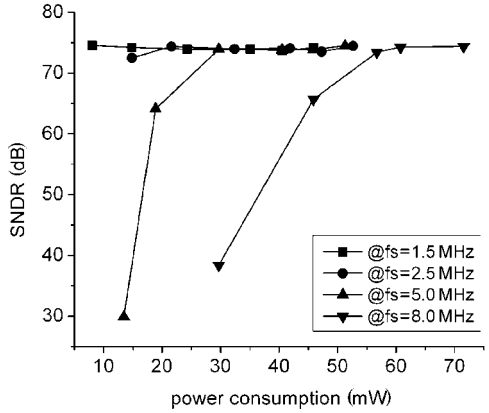

Fig.10. Measured SNDR versus power consumption at different sampling frequencies.

Table 1. Summary of the ADC performance @ f_{in}= 2.4 MHz.

Technology	0.18-μm 1P6M CMOS mixed signal technology	
Resolution (bit)	13	
Power supply (V)	2.7	
Sampling frequency (MHz)	2.5	8.0
Measured DNL (LSB)	–0.23 to +0.25	–0.30 to +0.25
Measured INL (LSB)	–0.32 to +0.55	–0.33 to +0.56
Peak SNDR (dB)	74.4	74.3
Peak SFDR (dB)	91.6	85.4
Lowest power consumption[a] (mW)	21.6	56.7

[a] The lowest power consumption of the SNDR above 73.4 dB

Table 2. Comparison with some previous works.

Reference	Resolution (bit)	Sampling frequency (MHz)	Input frequency (MHz)	SNDR (dB)	Power (mW)	Area (mm^2)	FOM (pJ)
Ref. [2]	14	12	1	75.5	98	10	1.7
Ref. [6]	14	10	4.8	77	220	12.54	3.8
Ref.[7]	13	40	1	67	268	3.6	3.7
This work	13	2.5	2.4	74.4	21.6	3.2	2.0
		8.0	2.4	74.3	56.7		1.8

performed at room temperature. Figures 8 (a) to 8 (c) indicate the measured FFT spectrum, DNL and INL. Figure 9 indicates the measured SNDR and SFDR with a 2.4 MHz input and 2.7 V power supply at different sampling frequencies up to 10 MHz.

The measured DNL and INL at 8.0 MSample/s are –0.30/+0.25 LSB and –0.33/+0.56 LSB, respectively. When the sampling frequency is 2.5 MHz with a –0.153 dBFS 2.4 MHz input, the measured peak SNDR and SFDR are 74.4 and 91.6 dB. When operating at 8.0 MSample/s, it achieves peak SNDR and SFDR of 74.3 and 85.4 dB. When the ADC is not running at full speed (8 MHz), lower power consumption can always be found while the ADC still maintains high accuracy. All the measured results are summarized in Table 1. As

shown in Fig.10, when the ADC operates at 1.5, 2.5, 5.0, and 8.0 MHz, the measured lowest power consumption for SNDR above 73.4 dB is 8.1, 21.6, 29.7, and 56.7 mW. According to Eq.(3), the FOM values are 1.25, 2.0, 1.5, and 1.8 pJ, respectively. Table 2 shows the comparison of this work and several previously reported high-resolution pipeline ADCs with 13-bit or 14-bit resolution. With emphasis on conversion accuracy and FOM value, the comparison shows that the prototype ADC achieves comparable conversion accuracy and FOM values.

$$\text{FOM} = \frac{\text{Power}}{2^{\text{ENOB}} f_{\text{s}}}. \tag{3}$$

5. Conclusion

This paper presents a high-accuracy low-power 13-bit 8 MSamples/s CMOS pipeline ADC. By using SHA-less architecture with improved front-end sampling circuit, on-chip programmable bias current, fixed drain-to-source voltage bias for the amplifiers in the pipeline stages, and low power on-chip reference circuit, the proposed ADC can get the highest ENOB of 12 bits and achieve different power dissipations at different sampling frequencies. The corresponding FOM values are 1.25, 2.0, 1.5, and 1.8 pJ at 1.5, 2.5, 5.0 and 8.0 MHz sampling rates, respectively, which is good in comparison with Refs.[2, 6, 7].

References

[1] Lu C C, Lee T S. A 10-bit 60-MS/s low-power CMOS pipelined analog-to-digital converter. IEEE Trans Circuits Syst Ⅱ, 2007, 54(8): 658

[2] Chiu Y, Gray P R, Nikolic B. A 14-b, 12-MS/s CMOS pipeline ADC with over 100-dB SFDR. IEEE J Solid-State Circuits, 2004, 39(12): 2139

[3] Cho T. Low-power low-voltage analog-to-digital conversion techniques using pipelined architectures. PhD Dissertation, University of California Berkeley, 1995

[4] Chiu Y. Inherently linear capacitor error-averaging techniques for pipelined A/D conversion. IEEE Trans Circuits Syst II, 2000, 47(3): 229

[5] Li Fule, Wang Hongmei, Li Dongmei, et al. A capacitor mismatch calibration technique for pipelined A/D conversion. Chinese Journal of Semiconductors, 2005, 26(9): 1838 (in Chinese)

[6] Chuang S Y, Sculley T L. A digitally self-calibrating 14-bit 10-MHz CMOS pipelined A/D converter. IEEE J Solid-State Circuits, 2002, 37(6): 674

[7] Ray S, Song B S. A 13-b linear, 40-MS/s pipelined ADC with self-configured capacitor matching. IEEE J Solid-State Circuits, 2007, 42(3): 463