Ternary logic circuit design based on single electron transistors

Wu Gang(吴刚)†, Cai Li(蔡理), and Li Qin(李芹)

(Institute of Science, Air Force Engineering University, Xi'an 710051, China)

Abstract: Based on the *I–V* characteristics and the function of adjustable threshold voltage of a single electron transistor (SET), we design the basic ternary logic circuits, which have been simulated by SPICE and their power and transient characteristics have been extensively analyzed. The simulation results indicate that the proposed circuits exhibit a simpler structure, smaller signal delay and lower power.

Key words: single electron transistor; adjustable threshold voltage; ternary logic

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1. Introduction

The multi-value logic (MVL) circuit is an important part of modern digital electronics. MVL circuits allow more than two levels of logic, so we may have ternary, quaternary or more levels of logic styles. Compared with the conventional binary logic, the information density in MVL is much higher. MVL can reduce the number of operations that is necessary to implement a particular mathematical function; thus it has an advantage in terms of reduced area, which in turn reduces parasitics associated with routing and provides a higher speed of operation. In the design of a digital system, an e level system costs less. Because 3 is the nearest integer to e, the ternary logic circuit has attracted more attention[1−4].

Over the past 40 years, researchers have advanced the performance of circuits and reduced their power dissipation by reducing characteristic size. But the reduction of characteristic size leads to some problems such as metal inter-linkage and current tunnelling which can hamper the development of integrated circuit. The single electron transistor (SET) needs only one or several electrons to work, so it can work with ultimately low power dissipation. On the other hand, the much smaller size of the SET can advance the integration density. So the low power dissipation and high density make the SET a key element for further development of integrated circuits[5].

In this paper, we introduce the basic ternary logic circuits and analyze the characteristic of adjustable threshold voltage of SET. Also, we design the basic ternary gates and extensively analyze the power and the transient characteristics of the designed circuits.

2. Basic ternary logic circuits

A kind of multi-value algebra system is necessary for the design of a multi-value logic circuit. In several actual multi-value algebra systems, the Disjoint algebra[6] is prevalent in engineering. The min (minimum) operator, max (maximum) operator and the literal operator are the basic operations in the Disjoint algebra.

Consider $L = \{0, 1, \cdots, R-1\}$ is the set of the multi-value variable in the R value system.

The max operator is defined as

$$\max(X, Y) = \begin{cases} X, & X \geqslant Y \\ Y, & X \leqslant Y \end{cases}, \tag{1}$$

where X, Y belong to the set R.

The min operator is defined as

$$\min(X, Y) = \begin{cases} X, & X \leqslant Y \\ Y, & X \geqslant Y \end{cases}, \tag{2}$$

where X, Y belong to the set R.

The literal operator is defined as

$${}^{a}X^{a} = \begin{cases} R-1, & X = a \\ 0, & X \neq a \end{cases}, \tag{3}$$

where X belongs to the set R.

If there are two thresholds, the literal operator is defined as

$${}^{a}X^{b} = \begin{cases} R-1, & a \leqslant X \leqslant b \\ 0, & X \leqslant a\,,\ X \geqslant b \end{cases}, \tag{4}$$

where X belongs to the set R.

3. Characteristics of adjustable threshold voltage of SET

The basic characteristics of SET are Coulomb oscillation and Coulomb block. Furthermore, SET can have multiple gates that give it an adjustable threshold voltage. The two-gate SET is shown in Fig.1, where C_{g1} and C_{g2} are the gate capacitances, and C_D and C_S are the tunnel junction capacitances. For the two gates, one gate is used as a voltage input port V_{in} and the other gate as a threshold voltage adjusting port V_{con}. The current through the two tunnel junctions in series is controlled by the voltage on the island. On the basis of Ref.[7], the formula to calculate the island voltage is

$$V_{island} = \frac{1}{C_\Sigma}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con} - ne), \tag{5}$$

† Corresponding author. Email: wugang1927@163.com

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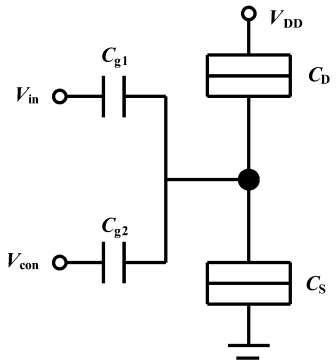


Fig.1. Sketch of two-gates SET.

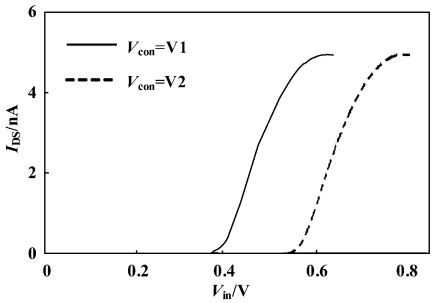


Fig.2. SET's characteristic of controlled threshold.

where $C_\Sigma = C_{g1} + C_{g2} + C_D + C_S$, and n is the number of the background charge that can be ignored.

We consider the inherent threshold voltage from the quanta island to be V_{th}, which is related to the parameter C_Σ[8]. The SET will turn on when $V_{island} > V_{th}$. Here V_{island} is

$$V_{island} = \frac{1}{C_\Sigma}(C_D V_{DS} + C_{g1} V_{in} + C_{g2} V_{con}) > V_{th}. \quad (6)$$

Then the apparent threshold voltage of the transistor from gate V_{in} is given as

$$V_{in} > \frac{C_\Sigma V_{th} - C_{g2} V_{con} - C_D V_{DS}}{C_{g1}}. \quad (7)$$

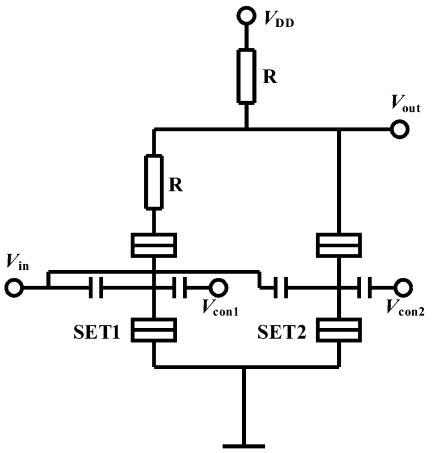
So the threshold voltage for the gate V_{in} is

$$V_{th}^1 = \frac{C_\Sigma V_{th} - C_{g2} V_{con} - C_D V_{DS}}{C_{g1}}. \quad (8)$$

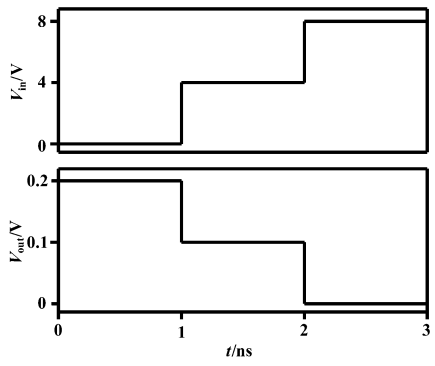
From Eq.(8), we can see that the threshold voltage for V_{in} is controlled by V_{con}. The characteristic of controlled threshold is shown in Fig.2.

4. Design of a ternary logic circuit based on an SET

In this study, the Mahapatra-Ionescu-Banerjee (MIB) model[9] of SET is used. The MIB model is based on the "Orthodox theory of single electron tunneling"[6], and it is a physically based compact model that can be used for single or multiple gates and symmetric or asymmetric devices. The model also accounts for the background charge and is valid in a wide range of drain to source voltages $|V_{DS}| \leqslant 3e/C_\Sigma$ and temperature $T \leqslant e^2/10\, k_B C_\Sigma$.



(a) Schematic of the complement gate



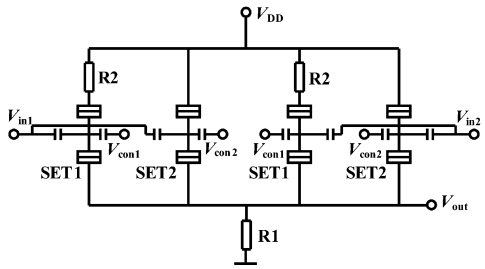
(b) Transfer characteristic

Fig.3. Ternary complement gate.

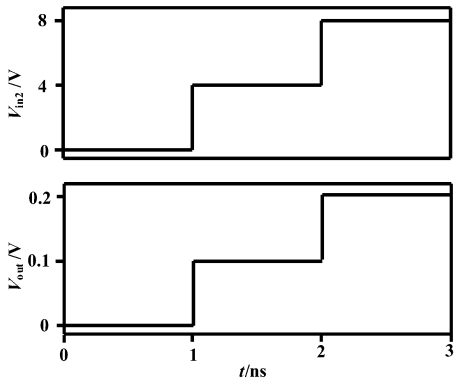
In the ternary logic circuit based on SET, we will use two kinds of SET, i.e. SET1 and SET2. The parameters of SET1 and SET2 are: $C_{g1} = C_{g2} = 0.01$ aF, $C_D = C_S = 1$ aF, $R_D = R_S = 1$ MΩ, $V_{con1} = 8$ V and $V_{con2} = 4$ V, where V_{con1} and V_{con2} are used to adjust the threshold voltages of SET1 and SET2 respectively. Based on these parameters, the threshold voltages of SET1 and SET2 are respectively 2.5 and 6.5 V. In order to reduce the leak current of the SET, V_{in} should be much larger than V_{DD}. So the voltage of the ternary logic level in input and output should be defined respectively. On the input, we define the logic "0" as a voltage less than V_{th1}, the logic "1" as a voltage between V_{th1} and V_{th2}, and the logic "2" as a voltage greater than V_{th2}. Because the supply voltage is 0.2 V, on the output, logic "0" would correspond to a voltage less than V_1 (≈ 0.1 V), logic "1" to a voltage between V_1 and V_2 (≈ 0.2 V), and logic "2" to a voltage greater than V_2.

4.1. Ternary complement gate

The ternary complement gate based on an SET is shown in Fig.3 (a). The circuit is composed of two resistances R and two SETs, i.e. SET1 and SET2. In order to realize the correct logic function, R should be much greater than the tunnel junction resistance, so we consider $R = 400$ MΩ. When V_{in} is less than V_{th1}, both SETs are off. Hence, the output voltage is held at V_{DD}. When V_{in} reaches a value between V_{th1} and V_{th2},



(a) Schematic of the max gate



(b) Transfer characteristic

Fig.4. Ternary max gate.

SET1 is on and SET2 is off. Hence, the output voltage is held approximately at $V_{DD}/2$. When V_{in} exceeds V_{th2}, SET2 turns on and SET1 turns off, so the output voltage is pulled down to almost 0. The output voltage can be expressed as

$$V_{out} = \begin{cases} V_{DD}, & V_{in} < V_{th1} \\ V_{DD}/2, & V_{th1} \leqslant V_{in} \leqslant V_{th2} \\ 0, & V_{in} > V_{th2} \end{cases}.$$

Figure 3 (b) shows the DC transfer characteristic of the complement gate.

4.2. Max gate

The max gate based on an SET is shown in Fig.4 (a). In the circuit, V_{in1} and V_{in2} are the inputs of the max gate, and V_{out} is the output of the max gate. When either V_{in1} or V_{in2} is logic "2", either of two SETs turns on, so the output voltage V_{out} is V_{DD}, that is logic "2".

When (V_{in1}, V_{in2}) = (0, 1) or (V_{in1}, V_{in2}) = (1, 0), the output voltage V_{out} should be logic "1". Hence,

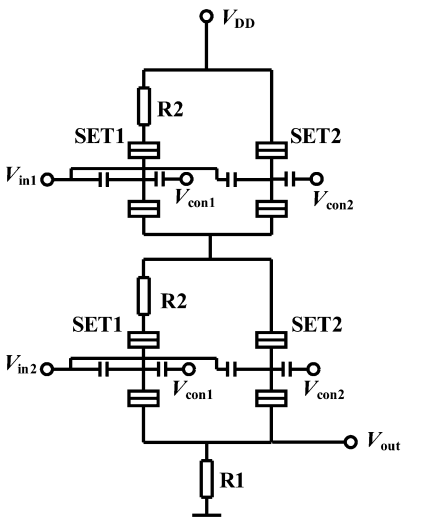
$$V_1 < V_{DD}\frac{R_1}{R_1 + R_2} < V_2. \tag{9}$$

When (V_{in1}, V_{in2}) = (1, 1), the output voltage V_{out} should be logic "0". Hence,

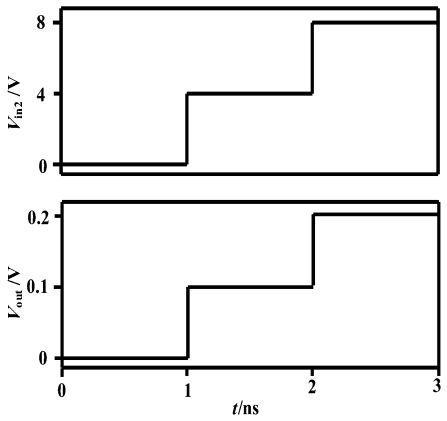
$$V_1 < V_{DD}\frac{R_1}{\frac{R_2}{2} + R_1} < V_2. \tag{10}$$

Considering $V_1 = \frac{1}{3}V_{DD}$ and $V_2 = \frac{2}{3}V_{DD}$, Equation (10) can be simplified as

$$\frac{1}{2}R_1 < R_2 < 2R_1,\ R_1 < R_2 < 4R_1. \tag{11}$$



(a) Schematic of the min gate



(b) Transfer characteristic

Fig.5. Ternary min gate.

Hence, the relation of R_1 and R_2 is $R_1 < R_2 < 2R_1$. In our simulation, $R_2 = \frac{3}{2}R_1$ has been chosen (R_1 = 400 MΩ, R_2 = 600 MΩ). Figure 4 (b) shows the DC transfer characteristics of the proposed max gate with V_{in1} at logic "0" and V_{in2} being swept from logic "0" to logic "2".

4.3. Min gate

The min gate based on an SET is shown in Fig.5 (a). In the circuit, V_{in1} and V_{in2} are the inputs of the min gate, and V_{out} is the output of the min gate. When either V_{in1} or V_{in2} is logic "0", there is no access between V_{DD} and the ground, so the output voltage V_{out} is 0, that is logic "0".

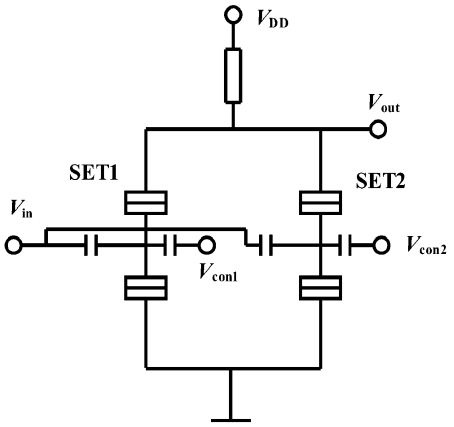
When (V_{in1}, V_{in2}) = (2, 1) or (V_{in1}, V_{in2}) = (1, 2), the output voltage V_{out} should be logic "1". Hence,

$$V_1 < V_{DD}\frac{R_1}{R_1 + R_2} < V_2. \tag{12}$$

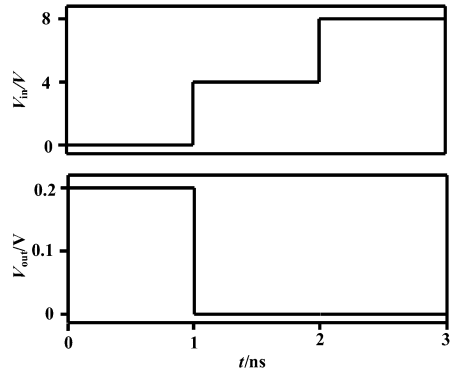
When (V_{in1}, V_{in2}) = (1, 1), the output voltage V_{out} should be logic "2". Hence,

$$V_1 < V_{DD}\frac{R_1}{2R_2 + R_1} < V_2. \tag{13}$$

Considering $V_1 = \frac{1}{3}V_{DD}$ and $V_2 = \frac{2}{3}V_{DD}$, the above formulas can be simplified as



(a) Schematic of the $^0X^0$ gate



(b) Transfer characteristic

Fig.6. Ternary $^0X^0$ gate.

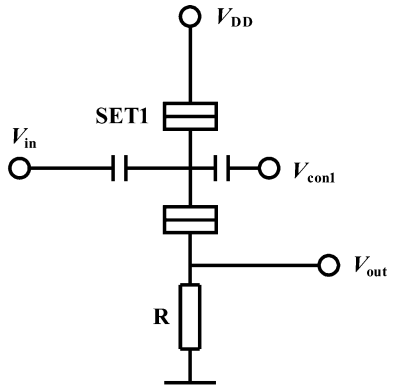
$$\frac{1}{2}R_1 < R_2 < 2R_1,\ \frac{1}{4}R_1 < R_2 < R_1. \tag{14}$$

Hence, the relation of R_1 and R_2 is $\frac{1}{2}R_1 < R_2 < R_1$. In our simulation, $R_2 = \frac{3}{4}R_1$ has been chosen (R_1 = 400 MΩ, R_2 = 300 MΩ). Figure 5 (b) shows the DC transfer characteristics of the proposed max gate with V_{in1} at logic "2" and V_{in2} being swept from logic "0" to logic "2".

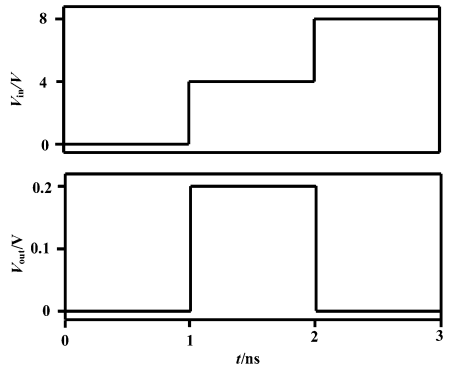
4.4. Literal gate

The $^0X^0$ gate based on SET is shown in Fig.6 (a). The circuit is composed of two SETs with a pull-up resistance. When the input V_{in} is logic "0", both SETs are off, so output voltage V_{out} is V_{DD}, that is logic "2". When the input V_{in} is logic "1", SET1 is on and SET2 is off, then there is an access between V_{DD} and the ground, so the output voltage V_{out} is 0, that is logic "0". When the input V_{in} is logic "2", SET1 is off and SET2 is on, then there is an access between V_{DD} and the ground, so the output voltage V_{out} is 0, that is logic "0". Figure 6 (b) shows the DC transfer characteristics of the $^0X^0$ gate.

The $^1X^1$ gate based on SET is shown in Fig.7 (a). The circuit is composed of on SET with a pull-down resistance. When the input V_{in} is logic "0" or "2", SET1 is off, so output voltage V_{out} is 0, that is logic "0". When the input V_{in} is logic "1", SET1 is on. There is an access between V_{DD} and the ground, so output voltage V_{out} is V_{DD}, that is logic "2". Figure 7 (b) shows the DC transfer characteristics of the $^1X^1$ gate.



(a) Schematic of the $^1X^1$ gate



(b) Transfer characteristic

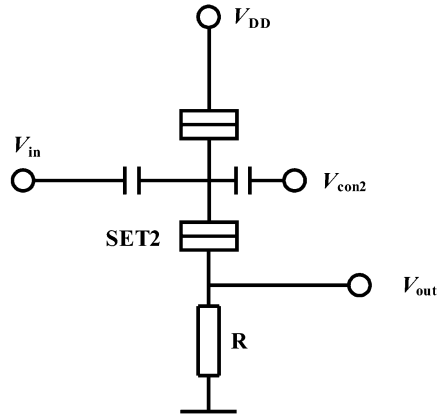
Fig.7. Ternary $^1X^1$ gate.

The $^2X^2$ gate based on SET is shown in Fig.8 (a). The circuit is composed of a SET with a pull-down resistance. When the input V_{in} is logic "0" or "1", SET2 is off, so output voltage V_{out} is 0, that is logic "0". When the input V_{in} is logic "2", SET2 is on. There is an access between V_{DD} and the ground, so output voltage V_{out} is V_{DD}, that is logic "2". Figure 8 (b) shows the DC transfer characteristics of the $^2X^2$ gate.

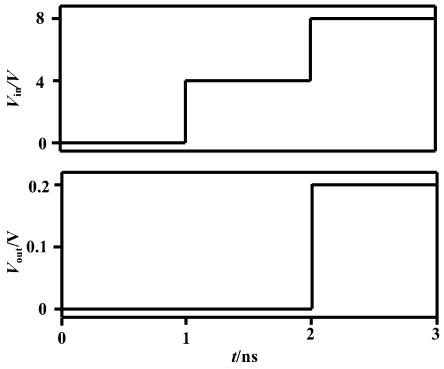
Based on the literal gates $^0X^0$, $^1X^1$ and $^2X^2$, we can design other kinds of literal gates[6].

5. Analysis of a ternary logic circuit based on an SET

The above ternary circuits have been simulated by SPICE. We can get the average delay time, average power and delay-power product. The performance parameters above are shown in Table 1. From Table 1, we can see that the average delay time of ternary logic circuits reaches the 10^{-11} s level, and the power reaches the nW level. The ternary circuits based on SET have much better transient performance and much lower power. In the design of the ternary logic circuits based on SET, the pull-up resistance and pull-down resistance have a more important effect on the performance of circuit. When the pull-up resistance or pull-down resistance increases, the delay time will increase but the power will decrease. So, when designing these circuits, we can adjust the pull-up resistance or pull-down resistance so as to make the delay-power product reach the minimum.



(a) Schematic of the $^2X^2$ gate



(b) Transfer characteristic

Fig.8. Ternary $^2X^2$ gate.

The SET has particular characteristics different from the conventional MOS transistor, so there are problems to be discussed.

(1) In order to avoid the leak current through SET, the voltage on gate V_{in} must be larger than the supply voltage V_{DD}. Then the voltage level of the input is larger than the voltage level of the output, leading to poor driven ability. For this problem, we can use a CMOS amplifier to magnify the output voltage so as to drive the next circuit.

(2) For the SET, in order to realize the characteristic of Coulomb block, the supply voltage V_{DD} must be smaller, so the noise margin of the proposed circuits is smaller. In order to advance the noise margin, we must advance the supply voltage V_{DD} and decrease the gate capacitance at the same time , but this will increase the power dissipation. So in the design of the circuit, we must select an appropriate value of V_{DD} to find a balance between noise margin and power dissipation.

Table 1. Average delay, average power and delay-power product of the designed circuits.

	Average delay (ns)	Average power (nW)	Delay-power product (10^{-18}J)
$\overline{x}$	0.08	0.92	0.074
$^0X^0$	0.08	0.48	0.04
$^1X^1$	0.04	0.44	0.018
$^2X^2$	0.04	0.40	0.016
min	0.07	0.41	0.028
max	0.1	0.44	0.044

6. Conclusion

The SET has an adjustable threshold voltage. We can get SETs with different threshold voltages by different controlling voltages on the gate, which is advantageous for the SET in designing a multi-value logic circuit. The basic ternary logic circuits have been designed. The simulation results indicate that the ternary logic circuits have a simpler structure, much better transient and much lower power dissipation.

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