Formation of a silicon micropore array of a two-dimension electron multiplier by photo electrochemical etching

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Abstract: A semiconductor PEC etching method is applied to fabricate the n-type silicon deep micropore channel array. In this method, it is important to arrange the direction of the micropore array along the crystal orientation of the Si substrate. Otherwise, serious lateral erosion will happen. The etching process is also relative to the light intensity and HF concentration. 5% HF concentration and 10–15 cm distance between the light source and the silicon wafer are demonstrated to be the best in our experiments. The n-type silicon deep micropore channel array with aperture of 3 μm and aspect ratio of 40–60, whose inner walls are smooth, is finally obtained.

Key words: photo-electrochemical etching; MCP; electron multiplier; micropore deep-channel n-type silicon
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1. Introduction

The microchannel plate (MCP) is a two-dimension channel electron multiplier (CEM) that is a honeycomb-shape thin slice composed of hundreds and thousands of passageways. The two-dimension CEM is used as the detector and the electronic image-amplifying device, which has many profits, such as high gain, low noise, high resolution, low power, wide band, long life and self-saturation effect. Since its invention in the 1960s, the MCP has been applied in the fields of military science, spectroscopy, medical X-ray image formation, material testing and instrument analyzing etc., especially in the fields of military night vision in the low-level light and space science[1,2].

The traditional MCP material and techniques have some inherent limitation factors. It is very difficult to improve the performance of a traditional MCP and extend its application area. The advanced technology of microchannel plates (AT-MCP) proposed by Galileo Co., early in the 1990s, has many merits compared with the traditional MCP process, and has been taken as a revolution in the MCP process. Key process technologies of AT-MCP include the etching processing technology of micropore channel arrays and the manufacturing technology of continuous dynode. The silicon micropore channel array is prepared by the dry-etching technology or the photo electrochemical (PEC) etching technology. The two-dimension silicon periodic channel array is processed by dry-etching technology such as electron-beam direct writing technology, deep reactive ion etching (DRIE) technology or induction coupled plasma (ICP) technology. The requirements of these technologies for equipments and process costs are very high. The PEC etching is cheaper than these dry-etching technologies, and the semiconductor PEC etching can remove the inherent limitation of the traditional MCP process. In this paper, n-type silicon micropore deep-channel arrays are prepared by utilizing silicon PEC anisotropic etching in an HF solution. Because holes of n-type silicon are minority carriers, the iodin-tungsten lamp is used to irradiate on the back of a silicon wafer to generate photo-generated holes in the anode etching process. Photo-generated current can be controlled by regulating light intensity and by being completely concentrated at channel tips. Thus the anisotropic etching process is sustained. A micropore channel array of high aspect ratio was fabricated finally. We also research the processing technology of the microchannel array of an MCP[3–9]. The continuous dynode will be fabricated in a subsequent process.

2. Fundamental theory of fabricating the silicon micropore array of an MCP

The mechanism of n-type silicon anisotropic etching is briefly described as follows: in the PEC process, on the one hand, the holes centralize at tips of the micropores array because the space charge region is bent around the micropore tips, as shown in Fig.1, which causes rapid dissolution of deep micropore tips. On the other hand, because Si$\{111\}$ dangling bonds are rather less than Si$\{100\}$ dangling bonds, the Si$\{111\}$ passivation speed is rather quick and effective. Then current impacted on Si$\{100\}$ was prior to Si$\{111\}$. The effective macropore growth is induced on Si $\{100\}$ in most possible cases and Si$\{111\}$ is firstly passivated to the channels wall. Because holes of n-type silicon are minority carriers, irradiations are employed to generate holes at the same time. So, after a while, the deep micropore channels are prepared by the PEC process at the tips of the square patterns.

The PEC reaction rate is closely related to the current

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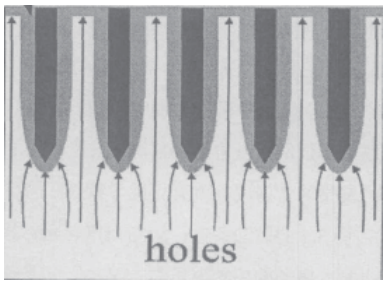

Fig.1. Hole distributing and infusing direction in n-type silicon.

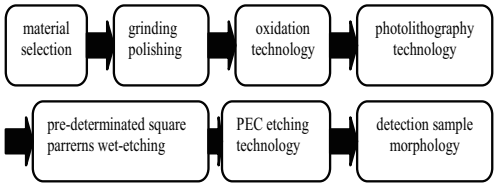

Fig.2. Manufacturing technological process schematic diagram of the n-silicon deep microchannel array.

density[3–6]. In the PEC procession, when the current flows through both electrodes and solution, charges are transferred with a certain rate. The process is the electrode reaction. The Faraday law shows the relation between the current flowing through electrode and the substance amount of the electrode reaction.

The PEC reaction rate v is the variable of the electrode reaction process per unit time and per unit area that is

$$v = \mathrm{d}\xi/A\mathrm{d}t, \tag{1}$$

where A is the region area with unit of m^2, the unit of the electrode reaction process ξ is mol, and the unit of the PEC reaction rate v is mol/(m^2·s). However, current is easily measured in the PEC experiments. So the PEC reactivity rate v is denoted by current density j. The relation between the current density j and the reactivity rate v is

$$j = ZFv. \tag{2}$$

Many subsequent PEC experiment phenomena and results were closely related to the reaction rate.

3. Experiments of fabricating the two-dimension silicon deep channel array

3.1. Manufacturing technological flow

On an n-type single crystal silicon substrate, the deep micropore array of the two-dimension electron multiplier MCP was prepared by applying oxidation, standard photolithography, KOH etching and PEC etching technology. The schematic diagram of the manufacturing technology process of n-silicon deep microchannel array is shown in Fig.2.

3.2. Experimental conditions

<100>-oriented n-type silicon substrates are adopted in the PEC etching experiments. The diameter of the silicon wafers is 1 inch. The resistivity of the n-type silicon wafers is 2–5 Ω·cm. The back side of the n-type silicon is coated with a layer of aluminum to provide an Ohm contact.

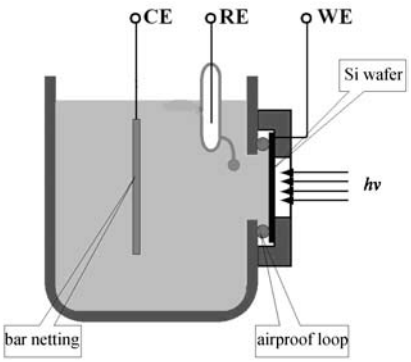

Fig.3. Cross-section of the electrochemical cell.

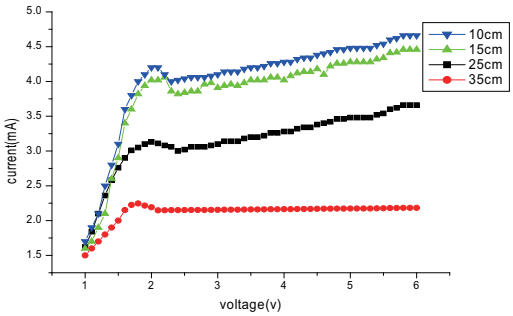

Fig.4. *I*–*V* characteristic curves in the different distance between light source and silicon wafer.

N-type silicon is anodized in hydrofluoric acid with concentrations of 1%–15%. At the same time, micropore arrays are formed at a constant potential and the electrolyte solution is stirred mechanically. The electrochemical three-electrode setup is used in the PEC experiments. The counter electrode (CE) is a platinum grid and the reference electrode (RE) is a saturated calomel electrode (SCE). The work electrode (WE) potential is controlled with a potentiostat. The current is plotted with an *X*–*Y* recorder. And all repetition experiments are conducted at room temperature at about 20 °C. The experimental process stability is very good. The cross-region of the electrochemical cell and its electrical connections is shown in Fig.3.

4. Results and discussion

4.1. Effect of light intensity on the n-silicon micropore array formation of the MCP

An iodin-tungsten lamp is used as a light source in the PEC experiments. The light intensity can be adjusted by changing the distance between the light source and silicon wafer. *I*–*V* characteristic curves are measured at different distances between the light source and silicon wafers, as shown in Fig.4.

In the Lehmann space charge region model[4–8], it is pointed out that holes generated by light at the back of wafers in the PEC process diffuse to boundaries of the space charge region at first, then they participate in the Si electrochemical etching reaction because of the electric-field effect between

Fig.5. Cross-section of the deep micropore array observed by a metallography microscopy.

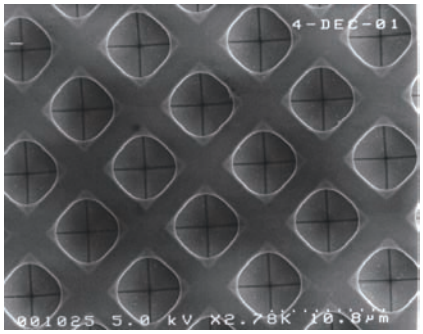

Fig.6. Plan alignment view of the micropore array direction and the Si substrate crystal orientation.

Si and the HF electrolyte. Thus, the space charge region is extended and the current intensity is increased before the voltage reaches a special value. The drifting rate and the amount of holes injecting into the space charge region in unit time is linearly increased with the rising of the current intensity, so the intensity of etching current is linearly raised with the increasing of the voltage (Eq.(2)). After the voltage reaches the special value, the increasing rate of the etching current becomes slow. In the space charge region, the drifting rate of carriers is saturated because of the lattice scattering, so the etching current reaches saturation too. According to Eq.(2), the PEC etching rate can be improved by changing the etching current which is proportional to the light intensity. The PEC etching rate remarkably varies with light intensity in the experiments. By analyzing lots of PEC experiments, the optimal process parameters are obtained. When the distance between the light source and the silicon wafer is 10 – 15 cm and the light source voltage is 12 V, the best etching result is obtained. Figure 5 shows a cross-section of the deep micropore array obtained in 5 wt% HF solution in the above conditions. The aspect ratio of the channels of the MCP with an aperture of 3 μm is 40–60. The deep micropore channel is not significantly laterally etched, and the inner walls of the micropore channel are very smooth.

4.2. Effect of crystal orientation on the n-silicon micropore array formation of the MCP

According to the difference of the etching rates of <100>-Si and <111>-Si, pre-determinate square patterns can be formed by the standard photolithography technology. The micropore array arranged along the same direction as the

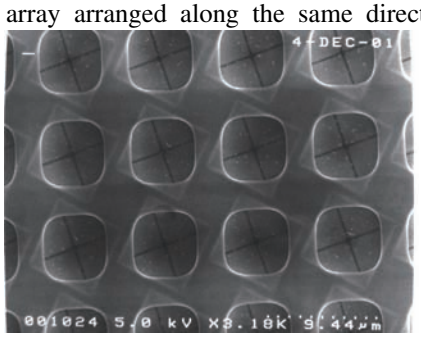

Fig.7. Plan discrepancy view of the micropore array direction and the Si substrate crystal orientation.

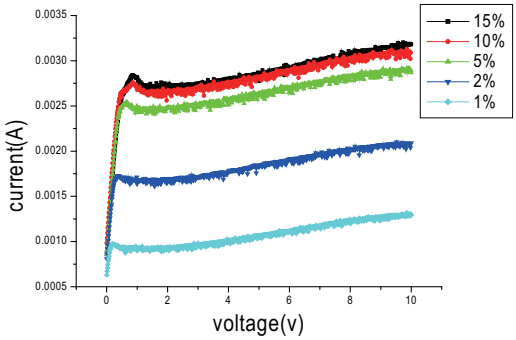

Fig.8. Effect of HF concentration on *I*–*V* curves of n-silicon.

crystal orientation of the Si substrate is shown in Fig.6. But Figure 7 shows the discrepancy between the micropore array direction and the Si substrate crystal orientation, which is because the micropore array arrangement direction is not adjusted to the silicon wafer crystal orientation in the standard photolithography process. Even so, the micropore channel array can also be formed by the subsequent PEC etching process. However, the square orientation is changed, and the geometry dimension of pre-determinate square patterns will be enlarged. If the distance between two adjacent square patterns is too short, then the two channels will be combined by the transverses etching. Therefore, the direction of the micropore array should be adjusted to the crystal orientation of the Si substrate before the PEC etching process. Otherwise, the distance between two adjacent micropores should be large enough.

4.3. Effect of HF concentration on the n-silicon micropore array formation of the MCP

Figure 8 shows the typical *I*–*V* curves of n-silicon etched in HF solutions with different concentrations, and the dependence of the PEC etching reaction on HF concentrations is revealed too. When the potential increases, the current exhibits a peak and then remains at a correspondingly slow change. According to Eq.(2), the PEC etching rate varies with the current density. As for n-type silicon with the same sizes, the higher the current is, the faster the etching rate is, and vice versa. At the constant potential, the PEC etching rate also increases when HF concentration increases.

Furthermore, the formation rate of the micropore channel arrays is the fastest when the HF concentration was about 5% according to previous experimental results. The main reasons include that the series impedance of Si/HF interface is large, and the current intensity at the tips of the micropore channel is rather large, and meanwhile the Schottky barrier is very low in about 5% HF concentration. If the HF concentration is less than 1%, the formation rate of the micropore channels is very slow, because F^- is low at the tips of the micropore channel, and the oxidation products of the deep micropore bottom cannot be promptly dissolved in the HF solution. Moreover, the area of the deep micropore tip that the current flowed through is rather large, thus the series impedance of the Si/HF interface is rather large. So the curvature radius of the deep micropore bottom is increased and the current intensity is decreased, and the growth of the deep micropore is further hindered. But if the HF concentration surpasses 15%, the lateral erosion of the inner walls of the silicon deep micropore channel becomes rather serious. The homogeneity of the inner surface morphology of the deep micropore channel array is destructed. Therefore, the optimal HF concentration is about 5%, which can ensure not only the suitable growth rate of the micropore channel but also the uniform inner surface morphology of the deep micropore channel array.

5. Conclusion

The n-silicon deep micropore array of the two-dimension MCP with an aspect ratio of 40−60 is manufactured in this paper. It is a key step to adjust the direction of the micropore array to the crystal orientation of the Si substrate during the process of forming pre-determinate square patterns before the PEC etching process. If the adjustment is incorrect, the serious lateral erosion will occur even though the deep micropore array can still be formed. The electrochemical reaction strongly depends on the light intensity and HF concentration. The best HF concentration is 5%, and the optimal distance between the light source and silicon wafers is 10−15 cm at 12 V light source voltage. Under these optimized conditions, the n-silicon deep micropore array with smooth inner walls is obtained at a fast etching rate. It is demonstrated that the PEC etching method used in this paper is an economic and practical solution to fabricate the deep micropore channel array of AT-MCP.

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