A widely tunable continuous-time LPF for a direct conversion DBS tuner

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Abstract: A continuous-time 7th-order Butterworth Gm–C low pass filter (LPF) with on-chip automatic tuning circuit has been implemented for a direct conversion DBS tuner in 0.35 μm SiGe BiCMOS technology. The filter's −3 dB cutoff frequency f_0 can be tuned from 4 to 40 MHz. A novel on-chip automatic tuning scheme has been successfully realized to tune and lock the filter's cutoff frequency. Measurement results show that the filter has −0.5 dB passband gain, +/– 5% bandwidth accuracy, 30 nV/Hz$^{1/2}$ input referred noise, −3 dBVrms passband IIP3, and 27 dBVrms stopband IIP3. The I/Q LPFs with the tuning circuit draw 13 mA (with f_0 = 20 MHz) from 5 V supply, and occupy 0.5 mm^2.

Key words: active filters; Butterworth filters; continuous-time filters; direct broadcast satellite tuner; Gm-C filters; SiGe BiCMOS

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1. Introduction

Most modern direct broadcast satellite (DBS) tuners use direct conversion architecture to achieve lower cost and power consumption. In a direct conversion DBS tuner , the broadband I/Q downconverting mixers directly convert a cluster of channels from the L-band (950–2150 MHz) to baseband. The baseband I/Q low pass filters (LPFs) select the desired channel signal, which is then converted to digital bits through ADCs in the digital demodulator chip for further processing.

The baseband LPF has to meet strict specification from system requirements.

(1) As the DBS channel date rate can vary from 1 to 45 Msps, the cutoff frequency of the channel selection LPF should be tunable from 4 to 40 MHz to cut off the closely spaced unwanted neighbor channel interferences. The DBS standards (e.g., DVB_S/DVB_S2) adapt QPSK or 8PSK modulation scheme, so the filter should have good linear phase response, i.e. it should have lower group delay distortion. As for all analog continuous-time filters, an automatic tuning system is needed to maintain the precise filtering characteristics against process variation, temperature drift and aging.

(2) Since there is no filtering until the baseband LPF, the LPF itself should be very linear. Here, the linearity of the LPF is increased on a circuit-level by introducing a high linear transconductor circuit (Gm cell), and on a system level by proper gain and pole distribution.

(3) System simulations indicate that a baseband VGA should be placed in front of the LPF to optimal noise and linearity line-up. So the noise specification of the LPF is not so challenge and can be compromised for lower power consumption.

2. System design considerations

2.1. About the main filter topology

For the main filter, a 7th-order Butterworth leapfrog Gm-C filter topology is selected based on the following observations:

(1) A leapfrog realization of a low pass filter has lower sensitivities of the passband frequency response to individual element values than a cascaded biquads realization[1].

(2) The Gm–C topology is usually preferred at high frequency for its lower power consumption relative to active-RC or MOSFET-C structures.

(3) If implemented in bipolar or BiCMOS technology, the Gm cells can be easily tuned through bias current variation as they can be designed to follow a linear g_m–I_c relationship, which is the fundamental translinear behavior of the bipolar junction transistor. As a result, Gm–C filter's cutoff frequency, which is proportional to Gm/C, can have a wide tuning range.

Here, we use the bipolar junction transistor in our 0.35 μm SiGe BiCMOS technology to design a novel translinear Gm cell which has a large enough signal–handling capacity and moderate low noise. By properly bias circuits design, the cutoff frequency of the implemented Gm–C main filter can also be directly proportional to a control current. In other words, we have a linear tunable ICF (current controlled filter.)

2.2. About corner frequency programmability and on chip automatic tuning

System specifications requires that the –3dB cutoff frequency f_0 of the LPF can be digitally programmed from 4 to 40 MHz, and the switching step should be as fine as possible to cut off the closely spaced unwanted neighbor channel interferences. Already having a linear tunable current controlled main

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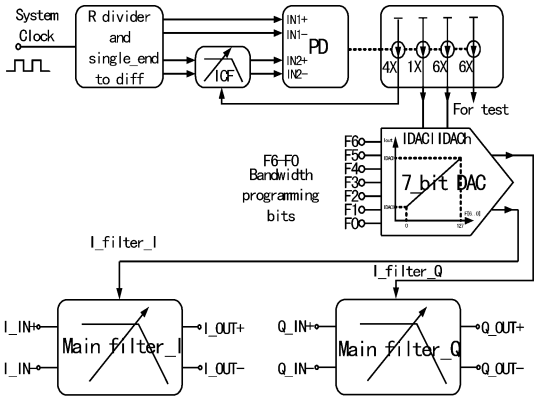

Fig.1. Filter system block diagram.

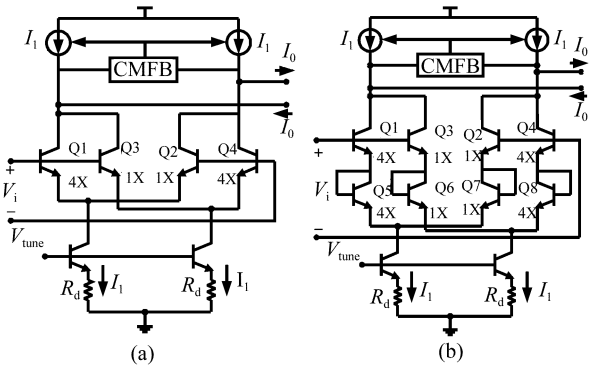

Fig.2. (a) Standard multitanh dublet Gm cell; (b) "Emitter-degenerated" multitanh dublet Gm cell.

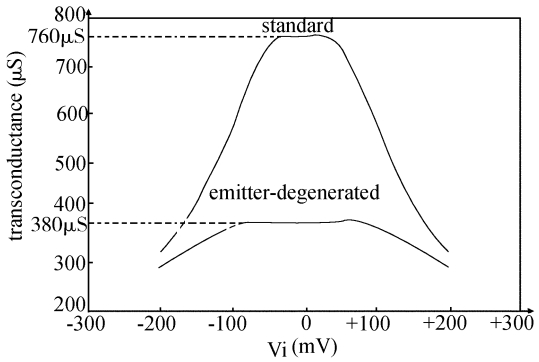

Fig.3. Simulated plots of G_m versus input signal for the standard and the emitter-degenerated multitanh doublet Gm cells with the same bias currents.

filter, we can use a linear current DAC to achieve digital programmability with a fine step. The output current of the DAC responding to the input digital bits is then used to control the main filter; thus the cutoff frequency of the main filter can be programmed within the DAC's resolution. Here a 7-bit linear current DAC is implemented.

To guarantee accurate and stable filtering characteristic, on-chip automatic frequency tuning is needed. In the proposed design, a master-slave tuning system locks the main filter's frequency response to a reference clock signal. The PLL-based on chip automatic tuning system is shown in Fig.1.

The 5-bit R counter divides the tuner system crystal frequency by R. The frequency-divided clock signal feeds a second-order linear tunable ICF, which is a fully differential Gm–C low pass biquad (see Fig.6). The phase detector compares the phase difference between the input and output of the ICF and changes the pole frequency of the ICF through a control current until the output is in quadrature with the input. Then the pole frequency of the ICF is equal to the reference frequency, which means that controlled by this current, the biquad ICF now exhibits an accurate and stable frequency response. Since the Gm–C biquad ICF use the same Gm cell topology as the main filter, and the capacitors used in the ICF and those in the main filter can be matched very well, the control current of the biquad ICF can also be used to derive that of the main filter to maintain a stable main filter frequency response. Here we "properly" scale it (see Fig.1) and use its two scaled versions as the two reference currents for the 7-bit linear current DAC. The DAC is designed to have the property that when its digital input is all "0"s, its output is its lower reference current, and when its digital input is all "1"s, its output is its higher reference current. In this way, we can fine tune the main filter's cutoff frequency through the 7-bit DAC without relocking the PLL, which means a very small tuning time. A relatively longer tuning time is needed when we have to change R to achieve a coarse tuning by relocking the PLL to a new reference frequency.

3. Circuit design

3.1. Gm cell

The Gm cell is the most critical building block of the whole filter and tuning system. The Gm cells designed should have large enough linear input range, reasonable low noise and wide bandwidth. They should be easily tunable and low power consumption. The Gm cell used in the main filter and the biquad ICF is a modified multitanh doublet[2]. Figure 2 (a) shows a standard multitanh doublet Gm cell, which has a small-signal transconductance of $Gm = 8I_1/25V_T$ (where V_T is the thermal voltage) 36% smaller than that of a simple bipolar differential pair biased with the same total tail current. As a result of this linearization technique, this Gm cell has a much wider input range (96 mV peak-to-peak differential ppd) than that of a simple differential pair (32 mVppd) beyond which the total harmonic distortion (THD) of the output current becomes greater than 1% (–40 dB). In order to further extend the linear input range, an "emitter-degenerated" multitanh doublet can be used as the filter's Gm cells (Fig.2 (b)). Diode connected bipolar transistors instead of normal resistors are used as the degeneration resistors in order to maintain the linear g_m–I_C relationship of the standard multitanh doublet. This Gm cell supports an input signal of about 200 mVppd for better than –40dB THD. Figure 3 shows the simulated plot of Gm versus input signal for the standard and the emitter-degenerated multitanh doublet Gm cells, which are biased with the same total tail currents. As in the standard multitanh doublet and a simple differential pair case, here the value of transconductance is again traded for larger linear input range. The load current sources are implemented as PMOS transistors. Since the LPF

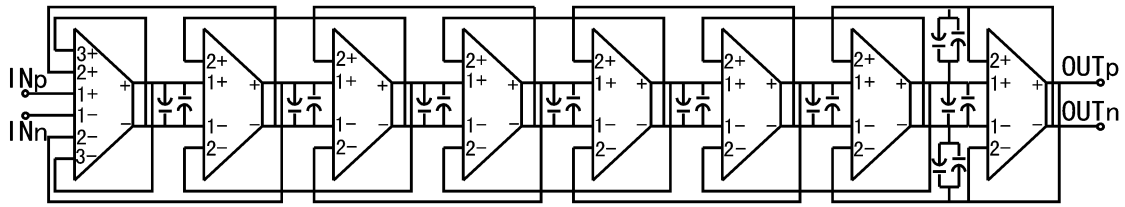

Fig.4. Main filter topology.

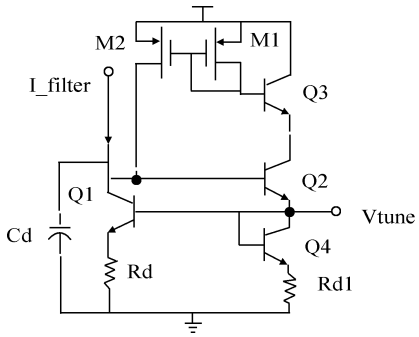

Fig.5. Main filter bias cell.

should have a wide tuning range, the bias current of the various Gm cells I1 will also be widely tuned. In order to keep the Gm cell's output impedance high even when the bias current I1 is at the high end of the tuning range, long channel PMOS transistors should be used. Longer and wider PMOS active loads contribute less flick noise to the Gm cells and the whole LPF. But the disadvantage of the large PMOS active load is the larger parasitic capacitances contribution, which should be considered when synthesizing the top topology of the LPF.

3.2. Main filter

The structure and the component values of leapfrog Gm–C filter are derived from the double terminated LC ladder LPF prototype by signal flow graph transformation. The LCR ladder prototype is a standard 7th-order Butterworth LPF added by a 1st-order delay equalizer to flatten the passband group delay. In cases where the output currents of several Gm cells are combined, we need only one set of load and common mode feedback (CMFB) circuit. So in practice we need half as many load and CMFB circuits as the Gm cell input stages[3]. The resulting topology is drawn in Fig.4. Node scaling technique is applied to the prototype active leapfrog filter to improve the dynamic range on the topology level. The passband gain of the original doubly terminated filter is −6 dB. Scaling is carried out by varying the transconductance and capacitor values appropriately so that the voltage gain from the input to the internal and output node is no larger than unity. This node scaling technique makes maximum use of the limited linear input range of the Gm cells. The integrating capacitors are split as anti-parallel ones to keep the back-plate parasitic capacitances balance to the n/p signal lines. Values of the actual capacitors are modified by deducing that of CMFB compensating capacitors and the parasitic capacitances contributed by the Gm cells. The main filter's bias cell is shown in Fig.5[4]. The control current is mirrored to the tail currents of the Gm cells with

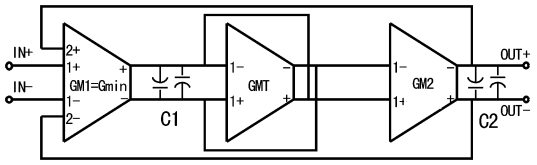

Fig.6. ICF topology.

different scaling ratios based on their individual Gm values. Voltage routing techniques is used to improve the matching between the Gm cells and to save power consumption, which requires a careful layout floor planning to properly route the base voltage bias line V_{tune}. In Fig.5, the base current of Q1 is compensated using a conventional beta helper transistor Q2. To further improve the accuracy, the base current of Q2 is again properly compensated. This is achieved by first sensing the amount of the base current of Q2 indirectly using the NPN transistor Q3 and then injecting it into the control current I_filter using PMOS current mirror M1 and M2. The capacitor C_{d} is included to reduce the circuit noise coupling, and the transistor Q4 and resistor R_{bl} is included to ensure that transistor Q2 is always biased in the active region. To improve matching, the current mirror transistor Q1 and the current source transistors in the Gm cells are designed to be multiplies of unit transistors. Accordingly, the degeneration resistors $R_{\text{d}s}$ are designed as parallel connected unit resistors to increase the output impedance of the current sources and to improve matching.

3.3. Biquad ICF

The ICF in the tuning circuit is a classic fully differential biquad with low-pass output (Fig.6)[5]. The low-pass transfer functions are

$$H_{\text{LP}}(S) = \frac{G_{\text{min}}G_{\text{m2}}}{S^2C_1C_2 + SC_2G_{\text{mT}} + G_{\text{m1}}G_{\text{m2}}}. \tag{1}$$

The pole frequency, the filter quality factor Q and the gain at the pole frequency of the biquad are

$$\omega_0 = \sqrt{\frac{G_{\text{m1}}G_{\text{m2}}}{C_1C_2}}, \quad Q = \frac{1}{G_{\text{mT}}}\sqrt{G_{\text{m1}}G_{\text{m2}}\frac{C_1}{C_2}},$$

$$H_{\text{LP}}(0) = \frac{G_{\text{min}}}{G_{\text{m1}}}, \quad H_{\text{LP}}(\text{j}\omega_0) = \frac{Q}{\text{j}}\frac{G_{\text{min}}}{G_{\text{m1}}}. \tag{2}$$

In the actual implementation, we choose $G_{\text{m1}} = G_{\text{min}} = \frac{1}{2}G_{\text{m2}} = 6G_{\text{mT}}$, $C_1 = C_2$ which leads to

$$\omega_0 = \frac{\sqrt{2}G_{\text{m1}}}{C_1}, Q = 6\sqrt{2}, H_{\text{LP}}(0) = 1, H_{\text{LP}}(\text{j}\omega_0) = \frac{Q}{\text{j}}. \tag{3}$$

At the pole frequency, the output of the ICF is in quadrature to its input. The proper function of the loop is independent of

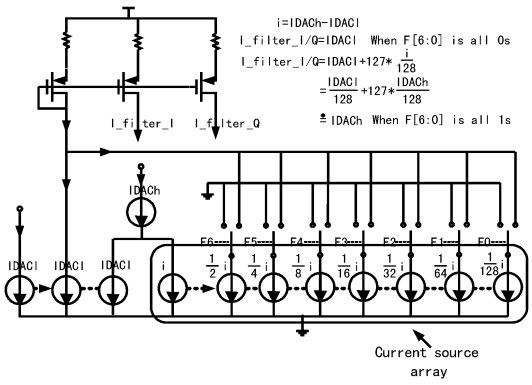

Fig.7. 7-bit DAC concept schematic.

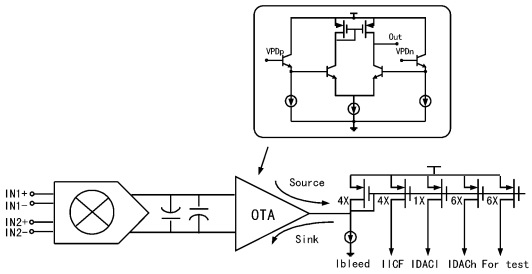

Fig.8. Phase detector and *V*–*I* conversion circuit.

the exact value of Q as long as it is in the range of 8 to 10 to provide sufficient tuning sensitivity. The ICF's bias cell is identical to that of the main filter in topology to improve the matching between the main filter and the biquad ICF.

3.4. DAC

The 7-bit DAC is a current-steering type linear DAC. Its concept schematic is shown in Fig.7. IDACh and IDACl are the DAC's high and low reference current, respectively. When the DAC's input is swept from all 0 s to all 1 s, its output current will vary linearly from IDACl to IDACh. Since the DAC is out of the PLL loop, it should be carefully designed to make its transfer characteristic independent of process variation and temperature drift, which is possible because the characteristic of the DAC depends only on elements matching. So a careful layout is also important here. The various current mirrors and current sources are designed using bipolar transistors with emitter degeneration. The transistors in the current source array are multiplies of unit bipolar transistors. And the ratioed degeneration resistors of the ratioed transistors in the current source array are implemented using conventional *R*–2*R* network. The matched transistors and resistors employ common centroid layout techniques to alleviate the effect of thermal gradients and stress gradients to which bipolar transistors are extremely sensitive.

3.5. Phase-detector

A current-output Gilbert multiplier is used as the phase detector, followed by two on-chip anti-parallel integrating capacitors to form an integrator (Fig.8). An OTA converts the differential output voltage of the integrator into a single end current signal, which combines with a constant bleeding current to derive the biquad ICF's control current and the DAC's reference currents. When the two inputs of the phase detector are in quadrature, its DC output current is zero. Then the DC output voltage of the integrator reaches a stable value and the PLL is settled. In order to suppress the second order harmonic signal of the phase detector output, the unit gain frequency of the integrator should be as low as possible. If implemented as an RC integrator, resistors or capacitors with large values are needed, which are very area consumption or even have to be off-chip. Here we bias the Gilbert multiplier with a small current to make the transconductance of the phase detector small enough. So capacitors small enough to be easily integrated on chip will meet the demand. The capture range of the PLL is set by the OTA's bias current and the bleeding current. When the OTA sinks all its bias current, the control current of the biquad ICF, IICF, is the sum of the bleeding current and the OTA's bias current, which makes the pole frequency of the ICF maximum. Contrarily, when the OTA sources all its bias current, IICF is the difference between the two currents, which makes the pole frequency of the ICF minimum. In the actual implement, the capture range of the PLL is from about 0.5 to 5 MHz.

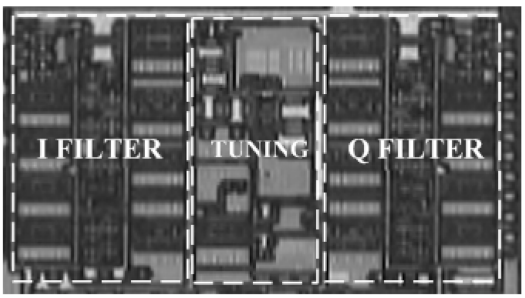

Fig.9. Die photo of the filter system.

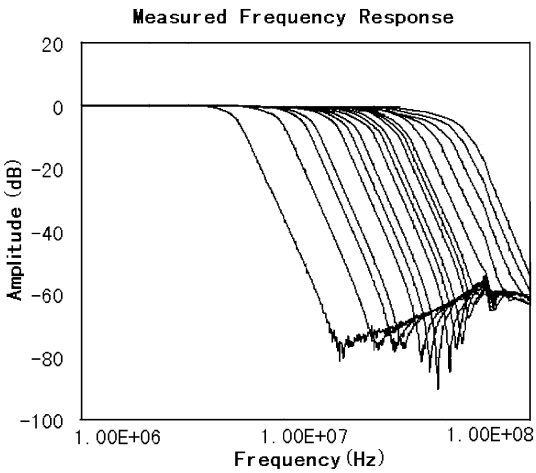

Fig.10. Measured filter frequency response.

4. Measurement result

The I/Q filters and the automatic tuning system have been implemented using a 0.35 μm SiGe BiCMOS technology. The die photo is shown in Fig.9. The I/Q channel filters with the tuning system occupy 0.5 mm^2.

Figure 10 shows the measured filter frequency response.

Table 1. Measurement results.

Technology	0.35 μm SiGe BiCMOS	
Supply voltage	5 V	
Filter type	7th-order Butterworth LPF	
Filter's cut off frequency f_0	4–40 MHz	
Filter's bandwidth accuracy (10 samples)	f_0 = 4 MHz	+/– 3%
	f_0 = 40 MHz	+/– 5%
Filter's stopband attenuation (f_0 = 20 MHz)	−25 dB @ 30 MHz −43 dB @ 40 MHz	
Filter's input referred noise (f_0 = 20 MHz)	30 nV/ $\sqrt{\text{Hz}}$	
Filter's passband IIP3 (f_0 = 20 MHz, f_{signal} = 10 MHz,11 MHz)	−3 dBVrms	
Filter's stopband IIP3 (f_0 = 20 MHz, f_{signal} = 40 MHz,41 MHz)	27 dBVrms	
Current consumption (I/Q filters + tuning circuits f_0 = 20 MHz)	13 mA	
Die size (I/Q filters + tuning circuits)	0.5 mm^2	

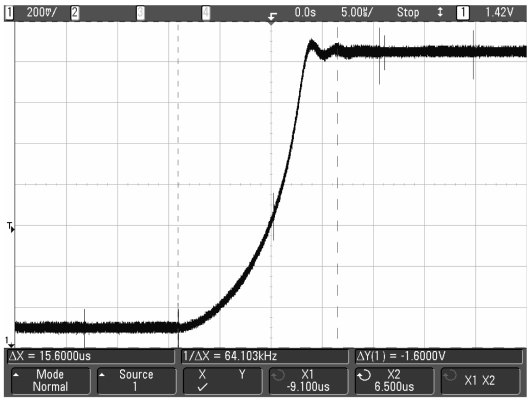

Fig.11. Measured PLL transit response.

Combined the coarse and fine tuning bits, the filter's cut off frequency can be tuned from about 3.98 to 39.6 MHz.

Figure 11 shows the PLL's transient response when the reference frequency is switched from 1 to 2 MHz. In this measurement, the test current (see Fig.8) flows through a 20 kΩ resistor to the PCB ground. In this case, the PLL's settling time is only 15 μs, which satisfy the system requirements.

Measured results are summarized in Table 1.

5. Conclusion

A high frequency and widely tunable continuous-time low pass filter has been implemented in the 0.35 μm SiGe BiCMOS technology. A novel on chip automatic tuning scheme has been successfully realized. The measurement results show that the filter system is well suited for a direct conversion DBS tuner.

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