A novel SOI-DTMOS structure from circuit performance considerations

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Abstract: The performance of a partially depleted silicon-on-insulator (PDSOI) dynamic threshold MOSFET (DTMOS) is degraded by the large body capacitance and body resistance. Increasing silicon film thickness can reduce the body resistance greatly, but the body capacitance also increases significantly at the same time. To solve this problem, a novel SOI DTMOSFET structure (drain/source-on-local-insulator structure) is proposed. From ISE simulation, the improvement in delay, obtained by optimizing p-n junction depth and silicon film thickness, is very significant. At the same time, we find that the drive current increases significantly as the thickness of the silicon film increases. Furthermore, only one additional mask is needed to form the local SIMOX, and other fabrication processes are fully compatible with conventional CMOS/SOI technology.

Key words: partially depleted silicon-on-insulator; dynamic threshold MOSFET; body capacitance; body resistance; silicon film thickness; circuit delay

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1. Introduction

The dynamic threshold MOSFET[1] (DTMOS), as shown in Fig.1, offers a good choice to the field of low voltage and low power devices because it provides low V_t, when the device is turned-on for high current drive, and high V_t, when the device is turned-off for low subthreshold leakage with these body-tied-to-gate structures. Although the same idea can be used in bulk devices, SOI technology is attractive for dynamic threshold MOS operation, due to the absence of substrate loading and substrate coupling problems that are encountered in the bulk DTMOS devices[1,2]. However, the large body capacitance and the delay in charging the body[3] are serious problems in implementing SOI-DTMOS. To solve this question, a novel SOI DTMOSFET structure (drain/source-on-local-insulator) is proposed as shown in Fig.2. In the novel structure, the improvement in delay is very significant, compared with conventional SOI-DTMOS, because the value of C_b is reduced by a shallow source/drain junction structure and the value of R_b is reduced by increasing silicon film thickness.

2. Analysis of optimized elements for the novel structures

A DTMOS delay is affected by two parameters dependent on T_{si} (silicon film thickness), namely R_bC_b and load capacitance C_l. C_l is proportional essentially to $C_g + C_b$ in a DTMOS circuit and C_g is the gate capacitance of the device. C_b is the body capacitance in a SOI DTMOSFET as shown in Fig.3. R_b is the body contact series resistance as shown in Fig.4.

Figure 5 shows the variation of C_b with silicon film thickness T_{si}. C_b for the novel structure remains constant and C_b for the conventional structure increases significantly for the same conditions. The reason is as follows.

In both the novel structure and the conventional structure, C_b depends strongly on A_S (source/drain-to-body-pn-junction area). In the conventional structure, source/drain-to-body junctions reach the Si-BOX layer interface, meaning that X_j (source/drain-to-body-pn-junction depth) is equal to T_{si}. And thus A_S, which is proportional to X_j, increases simultaneously as T_{si} increases, resulting in a rapid increase in C_b. In the novel structure, because of the drain/source-on-local-insulator structure, A_S is decided by the depth of the local insulator layer, not by T_{si}, and thus A_S becomes a constant when the depth of the local insulator is defined.

Figure 6 shows the variation of R_bC_b with silicon film thickness T_{si}. In the conventional structure, the product R_bC_b reduces significantly with T_{si} for small values of T_{si} because almost the entire body is depleted and thus the increase in C_b becomes slower than the decrease in R_b. And for larger values of T_{si}, the decrease in R_bC_b is compensated by a rapid increase in C_b and thus the value of R_bC_b nearly saturates. In the novel structure, the product R_bC_b reduces with increasing T_{si} for all values of T_{si}. Due to the shallow X_j from the drain/source-on-local-insulator structure, C_b is very small and hardly changes as T_{si} increases because A_S is constant as discussed above. At the same time R_b decreases significantly as T_{si} increases, reducing the R_bC_b delay of a DTMOS circuit as shown in Fig.6.

3. Simulation results and discussion

We used ISE[4] device simulations for conventional and novel structure PDSOI DT nMOSFETs of 100 nm drawn gate length in this study. The technology parameters used for these nodes are as per the International Technology Roadmap for Semiconductors (ITRS), with drive currents meeting the roadmap targeted values. The supply voltage V_{dd} used for these studies is 0.6 V, in order to prevent the source/drain-to-body

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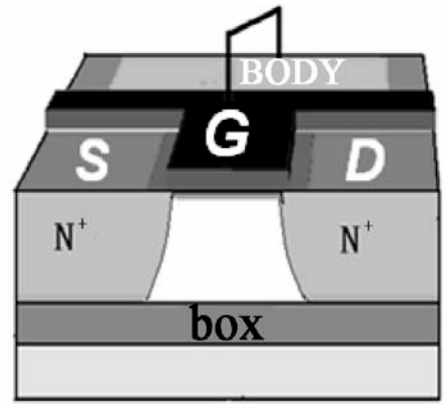

Fig.1. Conventional PDSOI-DTMOSFET.

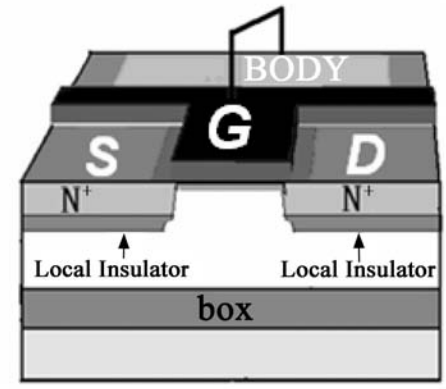

Fig.2. Novel PDSOI-DTMOSFET.

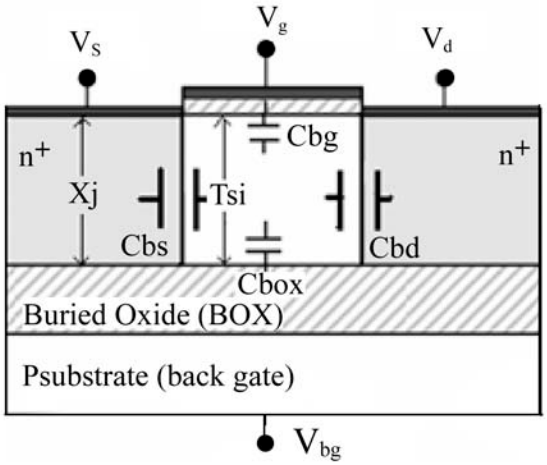

Fig.3. Body capacitance in an SOI DTMOSFET.

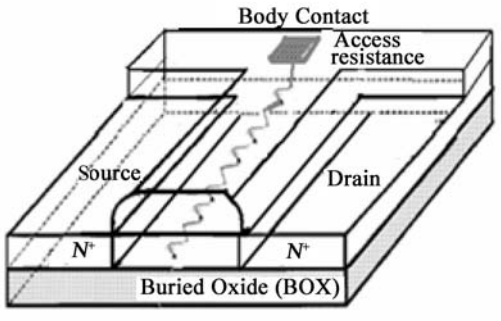

Fig.4. Body access resistance in an SOI DTMOSFET.

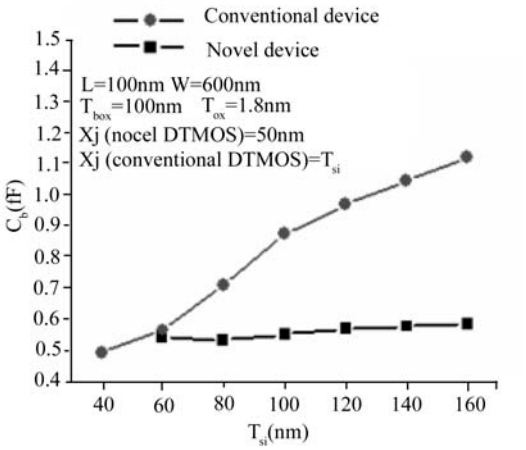

Fig.5. Variation of C_b with silicon film thickness Tsi.

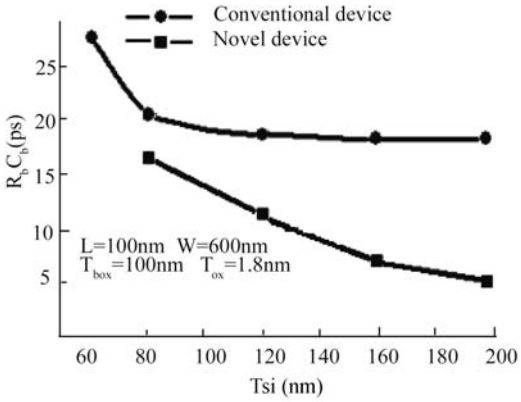

Fig.6. Variation of R_bC_b with silicon film thickness T_{si}.

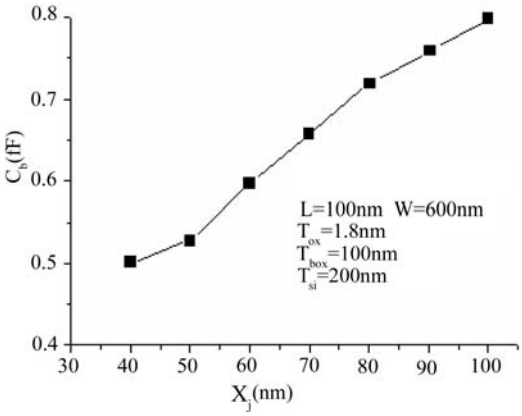

Fig.7. Variation of C_b with X_j for the novel device.

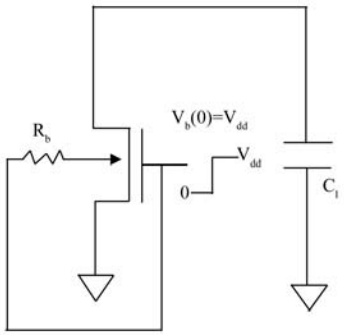

Fig.8. Measure structure used to measure DTMOS circuit delay.

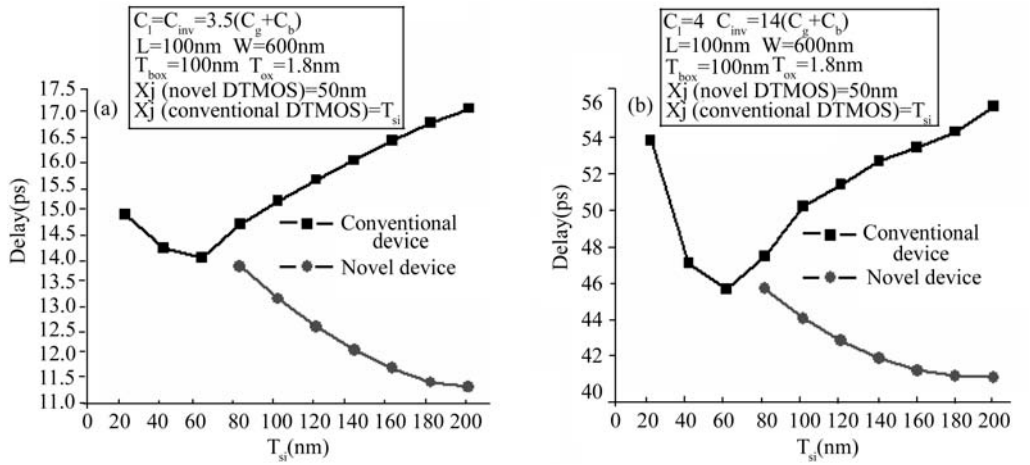

Fig.9. Device speed comparison between conventional and novel device PDSOI-DTMOS. (a) For $c_l = c_{inv} = 3.5(c_g + c_b)$; (b) For $c_l = 4c_{inv} = 14(c_g + c_b)$.

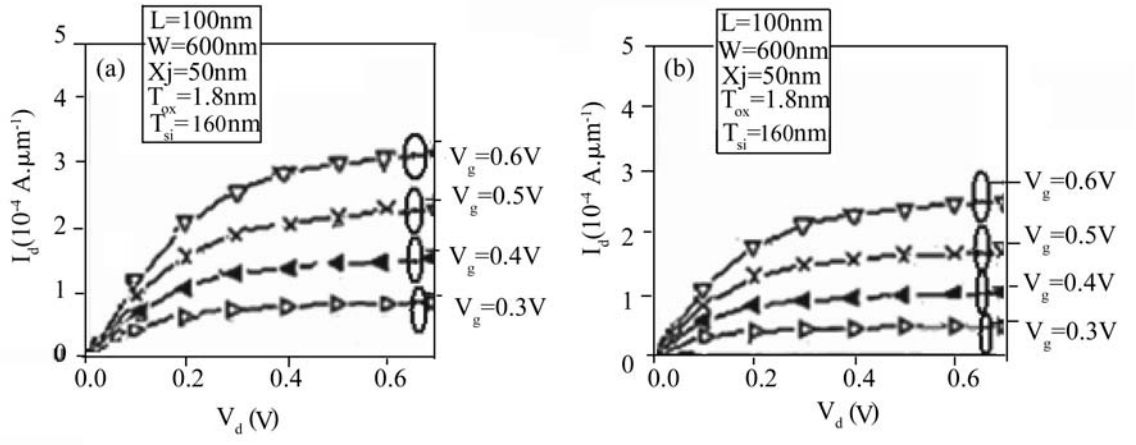

Fig.10. Comparison of simulated I_d–V_d characteristics. (a) Novel SOI-DTMOS device; (b) Conventional device.

junction from turning on.

We define the optimum value of X_j as that which gives the minimum value of C_b for the novel structure. As shown in Fig.7, C_b reduces significantly with X_j for larger values of X_j because A_S reduces greatly as X_j decreases. For small values of X_j (X_j < 50 nm), the decrease in C_b becomes slow because almost the entire source/drain-to-body junction is depleted and the charge share phenomenon in the depleted layer slows down the decrease of C_b. At the same time, considering the process condition and the dependence of R_{ds} (source/drain series resistance) on X_j, we hope the X_j is not too small. From general considerations, we define that the optimum value of X_j for the novel device, namely the distance between the Si surface and the local-insulator-layer surface, is approximately equal to 50 nm. We define the optimum value of T_{si} as that which gives the minimum DTMOS circuit delay for a particular value of OFF state leakage current. A good measure of this is the delay of the circuit shown in Fig.8[5]. In the measurement method, the source bias is 0 V, the drain is connected to load capacitances, and the gate is connected to the body through R_b, which is defined in the simulation above. And then the delay is calculated when the load discharges through the measured novel device.

The device speed comparison between conventional and novel PDSOI-DTMOS as T_{si} increases is shown in Fig.9. In the conventional structure, the delay decreases and then increases as T_{si} increases, because the product R_bC_b reduces significantly with T_{si} for small values of T_{si} and the value of R_bC_b nearly saturates for larger values of T_{si} as discussed in section 2; then the delay increases significantly as T_{si} increases because of an increase in $C_g + C_b$, which is proportional essentially to C_l in the DTMOS circuit. The smallest value of delay appears when T_{si} is about 60 nm.

In the novel structure, the delay decreases significantly as T_{si} increases because the product R_bC_b reduces significantly with T_{si} for all values of T_{si} as discussed in section 2, and after T_{si} is beyond about 180 nm the decrease in delay becomes slow because the R_bC_b delay is so small that the load delay of typical logic gates becomes dominant. So we define the optimum value of T_{si} as 180 nm.

As shown in Fig.9, the decrease in delay is about 15% for load $C_l = C_{inv}$, and about 10% for load $C_l = 4C_{inv}$ when T_{si} is increased from 20 to 200 nm, compared with conventional PDSOI-DTMOS. The improvement in delay, obtained by a shallow source/drain junctions depth and by optimizing T_{si}, is very significant, considering the reported speed improvement with DTMOS[6, 7] for the novel SOI-DTMOS structure device.

Finally, we analyze using two-dimensional (2D) simulations, the I_d–V_d characteristics of the novel and conventional

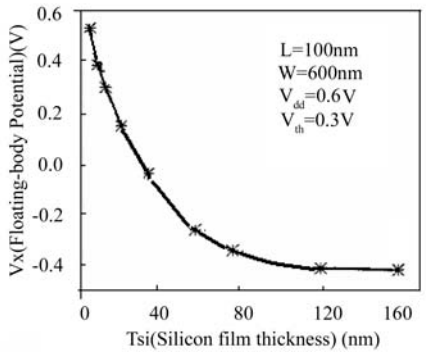

Fig.11. Floating-body potential at the silicon-BOX layer interface.

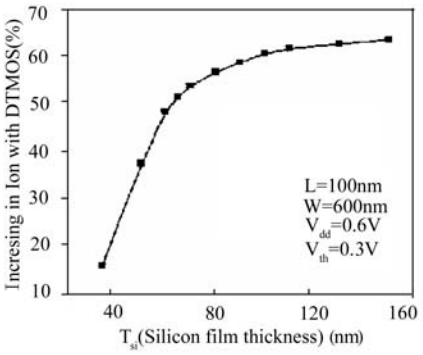

Fig.12. Increasing drive current as a function of T_{si} for the SOI-DTMOS.

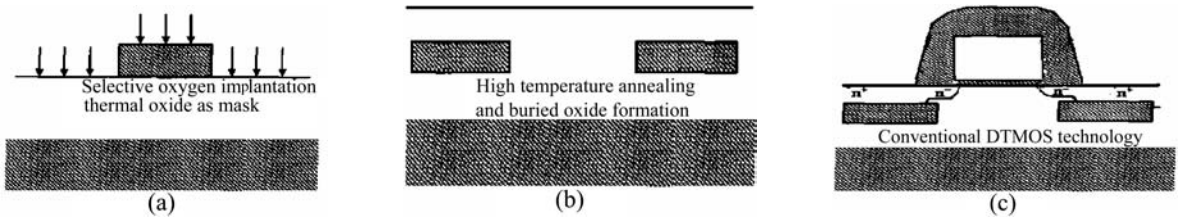

Fig.13. The novel device and its fabrication process.

devices whose delays are smallest as discussed above. As shown in Fig.10, the increase in drive current in novel SOI-DTMOS operation over conventional SOI-DTMOS operation is very large. We find that the increase in drive current is very sensitive to T_{si}. Significantly enhanced drive currents are observed only when the film thickness is sufficiently large.

We explain this observation as follows. We define V_x as the floating body potential (at the silicon-BOX layer interface) in the PD SOI device when the body is not connected to a gate. For a significant increase in current drive, the applied body bias should be much larger than V_x because only then would the depletion charge under the gate decrease appreciably, increasing the inversion charge correspondingly. This is the principle of operation of DTMOS. V_x is dependent on the thickness of the silicon film as well as the substrate doping and decreases when either is increased. As shown in Fig.11, V_x decreases when the thickness of the silicon film increases.

Now，let us consider a PDSOI-NMOS device with a film thickness of 160 nm. In DTMOS operation, when $V_b(= V_g) = V_{dd}$, the potential at the body contact becomes about 0.2 V, which is much larger than V_x (about −0.4 V in this case as shown in Fig.11). Thus, the drive current increases significantly. Then, let us consider a device with a silicon film thickness of 40 nm. In this case V_x is at −0.05 V as shown in Fig.11. When the gate is tied to the body and is at V_{dd}, the potential in the body near the contact becomes about 0.2 V, which is only slightly more than V_x. Thus the drive current does not increase significantly. The increasing drive current for the SOI-DTMOS with increasing T_{si} is shown in Fig.12.

4. Novel device fabrication process

The low dose and low energy local separation by implantation of oxygen (SIMOX) technology combined with the conventional CMOS/SOI technology is used to fabricate this kind of device. As SIMOX has been developed, low dose and low energy implantation has been widely used. This makes it possible to realize the novel structure by local SIMOX technology. Figures 13 (a), 13 (b) and 13 (c) illustrate the fabrication procedure. First, a thermal SiO_2 layer of thickness 500 nm was grown on the wafer as a mask for selective implantation. Then the windows for implantation were formed. Oxygen was implanted with an energy of about 100 keV for implantation and the dose of oxygen was about 6×10 cm^{-2} for a 100 mm diameter wafer. The temperature of the substrate was set to about 500 °C during the implantation. After the implantation，the wafers were annealed at about 1300 °C for 6 h in Ar + 0.5% O_2 gas. The thin oxide formed during this anneal was removed. As reported by He and Jiang[8], routine inspections of the samples with a microscope show that the product wafers are flat and perfectly crystalline. Only one additional mask is needed to form the local SIMOX, and other fabrication processes are fully compatible with conventional CMOS/SOI technology.

5. Conclusion

The performance of PDSOI-DTMOS devices is degraded by large body resistance R_b and body capacitance C_b. These parameters depend strongly on T_{si} and X_j. We propose a novel device structure of PDSOI-DTMOS, in which C_b is reduced by small X_j, obtained from the shallow drain/source-on-local-insulator structure, and R_b is reduced by increasing silicon film thickness. From ISE simulation, the improvement in delay, obtained by optimizing T_{si} and X_j, is very significant for the novel SOI-DTMOS structure device. At the same time, we find that the drive current increases significantly as the silicon film thickness increases for the novel structure. Furthermore, only one additional mask is needed to form the local SIMOX, and

other fabrication processes are fully compatible with conventional CMOS/SOI technology. The technology offers options for developing DTMOSFET technology.

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