# Accurate and fast table look-up models for leakage current analysis in 65 nm CMOS technology*

Xue Jiying(薛冀颖)†, Li Tao(李涛), and Yu Zhiping(余志平)

*(Institute of Microelectronics, Tsinghua University, Beijing 100084, China)*

**Abstract:** Novel physical models for leakage current analysis in 65 nm technology are proposed. Taking into consideration the process variations and emerging effects in nano-scaled technology, the presented models are capable of accurately estimating the subthreshold leakage current and junction tunneling leakage current in 65 nm technology. Based on the physical models, new table look-up models are developed and first applied to leakage current analysis in pursuit of higher simulation speed. Simulation results show that the novel physical models are in excellent agreement with the data measured from the foundry in the 65 nm process, and the proposed table look-up models can provide great computational efficiency by using suitable interpolation techniques. Compared with the traditional physical-based models, the table look-up models can achieve 2.5X speedup on average on a variety of industry circuits.

**Key words:** leakage current; 65 nm technology; table look-up model; interpolation
**DOI:** 10.1088/1674-4926/30/2/024004 **EEACC:** 1130B

## 1. Introduction

CMOS devices have been scaled down aggressively in each technology generation to achieve higher integration and performance. However, the leakage current has increased steadily with down-scaling and has become a major contributor to the total IC power. Different leakage mechanisms contribute to the total leakage current in a device. Among them, the three major ones can be identified as: subthreshold leakage current, gate oxide leakage current, and junction tunneling leakage (JTL) current[1]. For sub-65 nm technologies, emerging techniques to moderate the gate-oxide tunneling effect by using high-*k* dielectrics to better insulate the gate from the channel now bring gate oxide leakage current under control[2]. Hence, the main effort of this paper will focus on the analysis of subthreshold leakage current and JTL current.

Many works have been conducted to do leakage current analysis based on the physics-based models which have, for many years, been the most attractive approach for semiconductor device modeling and circuit simulation. However, previous works did not pay enough attention to variations in process parameters including lithographic and non-lithographic variation[3,4], such as dopant variation and layout dependent stress variation in strained silicon technology, making the traditional models inapplicable to the leakage current analysis in 65 nm technology. In this work, we develop new and more accurate compact physical models for leakage current analysis in the nano-scaled process. In addition, since many process parameters have to be introduced to the physical models in 65 nm technology, the new models would be more complicated, leading to longer simulation time. To improve the simulation speed, the table look-up model[5−10] is first introduced in this paper to conduct the leakage current analysis. The principle of using the table look-up model for leakage current simulation is to express the physical models in the form of tables. Then the calculation of leakage current would be translated to the search of the established tables, saving a considerable amount of time.

In this work, novel table look-up models for the subthreshold leakage current and JTL current analysis in 65 nm technology are proposed. This work also discusses, in detail, the generation of the leakage current characteristic tables from the established models and the use of appropriate numerical interpolation techniques to obtain more point values from the tables during the simulation process. The proposed table look-up models have been tested and verified with actual measured data in 65 nm CMOS technology.

## 2. New table look-up model

This section describes the generation of the table look-up models. First, the new physical models for subthreshold and JTL current are developed including scaling effects (e.g. short channel effect, narrow width effect), and layout parameters are added in the models to account for the effects induced by novel stress techniques. And then, based on the established compact models, the device leakage current characteristic tables for subthreshold and junction tunneling leakage current are generated, respectively. At the end of this section, the appropriate interpolation methods for our table look-up models are discussed.

### 2.1. Table look-up model for JTL current

#### 2.1.1. Novel compact physical model for JTL current

A high electric field across a reverse biased p-n junction causes JTL current due to the tunneling of electrons through

* Project supported by the State Key Development Program for Basic Research of China (No. 2006CB302700).

† Corresponding author. Email: xuejy06@mails.tsinghua.edu.cn

Received 11 August 2008, revised manuscript received 22 September 2008 


(a) (b)

Fig.1. Change of $J_{\text{junc}}$ under the influence of the "halo" profile: (a) Non-rectangular junction after lithography; (b) Impact of non-rectangular junction and "halo" on JTL.

the bandgap. The electron-hole pair generation/recombination comes not only through band-to-band tunneling (BBT), but also through trap-assistant tunneling (TAT). The total generation rate is composed of a BBT contribution term $R_{\text{BBT}}$ and a TAT term $R_{\text{TAT}}$. Then the JTL current can be expressed as

$$I_{\text{junc}} = q \iint (R_{\text{BBT}} + R_{\text{TAT}}) \mathrm{d}x\mathrm{d}y. \tag{1}$$

For a symmetrical MOSFET, Equation (1) can be applied to both the drain and the source junction. Previous works obtained the models for JTL current through the calculation of the integral in Eq.(1) by using the average JTL current density ($J_{\text{junc}}$) which is determined by the average electric field across the junction[1]. These models are not accurate because they are developed based on the assumption that the junction edge in an MOSFET is rectangular. However, this assumption works only when $J_{\text{junc}}$ is almost the same everywhere along the pn junction. In a real-life MOSFET, the peak of current density would actually changes significantly when the "halo" profile is applied to reduce the depletion region width of the source-substrate and drain-substrate junctions in nano-scaled technology. The current density peak occurs where the high doping region is implanted, and there is very nearly no current leaking through the bottom side of the junction. This can be seen in Fig.1 which is obtained using TCAD simulator Sentaurus.

Moreover, in the previous works, $J_{\text{junc}}$ is modeled as a function of $N_{\text{aside}}$ and $N_{\text{dside}}$, where $N_{\text{aside}}$ and $N_{\text{dside}}$ represent the acceptor doping concentration and donor doping concentration, respectively. These two non-lithographic variation sources not only exhibit large fluctuations in nano-scaled technology but also are very hard to be characterized, as the actual dopant profile cannot be measured directly. Therefore, new parameters should be introduced to replace them.

In this paper, we use two new parameters, $V_{\text{thlin}}$ and $V_{\text{thsat}}$ to express JTL current and its variations. $V_{\text{thlin}}$ is the subthreshold voltage measured when $V_{\text{ds}} = 0.1$V, representing the channel doping effect, and $V_{\text{thsat}}$ is the subthreshold voltage measured when $V_{\text{ds}} = V_{\text{DD}}$, representing the doping effects in drain.

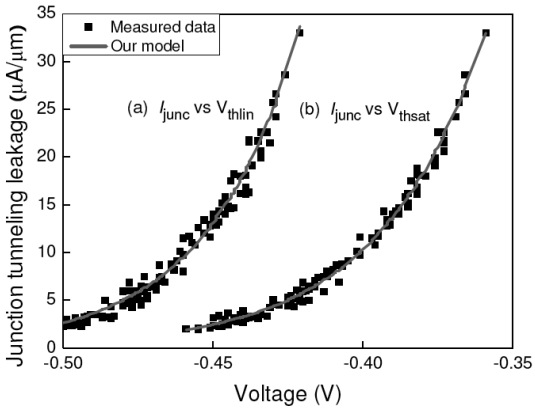


Fig.2. Comparison of our junction tunneling leakage current model with measured data in the 65 nm process: (a) $V_{\text{thsat}}$ is kept constant, $J_{\text{junc}}$ mostly depends on $V_{\text{thlin}}$; (b) $V_{\text{thlin}}$ is kept constant, $J_{\text{junc}}$ mostly depends on $V_{\text{thsat}}$.

The measurement of $V_{\text{thlin}}$ and $V_{\text{thsat}}$ complies with the standards of industry measurement. These two parameters not only have clear physical meanings, but are also easily measured.

Our junction tunneling leakage current model is shown as

$$I_{\text{junc}} = W\alpha_{\text{halo}}(R_{\text{BBT}}+R_{\text{TAT}})\frac{V_{\text{ds}}^{3/2}}{E_{\text{g}}^{1/2}} \exp\left(\frac{E_{\text{g}}^{3/2}}{\sqrt{V_{\text{ds}}}} + \frac{V_{\text{thlin}}}{\alpha_{\text{thlin}}} + \frac{V_{\text{thsat}}}{\alpha_{\text{thsat}}}\right), \tag{2}$$

where $E_{\text{g}}$ is the bandgap, $\alpha_{\text{halo}}$ denotes the tunneling length induced by "halo", and $\alpha_{\text{thlin}}$, $\alpha_{\text{thsat}}$, $R_{\text{BBT}}$ and $R_{\text{TAT}}$ are empirical parameters which can be extracted from measurement, respectively.

The comparison of the model prediction with measured data in the 65 nm process from the foundry is shown in Fig.2, where the horizontal axis represents $V_{\text{ds}}$. Because the curve in Fig.2 is obtained from the foundry for the PMOS device, the value of $V_{\text{ds}}$ is negative. We can see from Fig.2 that most of the JTL variations can be included by characterizing the fluctuations of $V_{\text{thlin}}$ and $V_{\text{thsat}}$.

### 2.1.2. Fast table look-up model for JTL simulation

Based on the proposed accurate physical model, we can

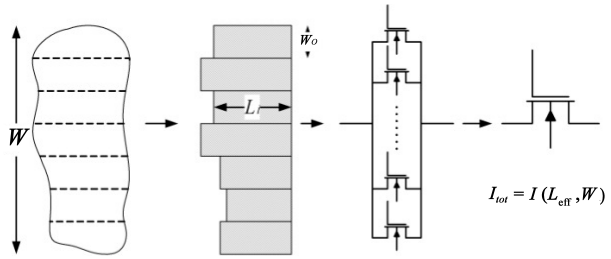


Fig.3. Procedure to derive the effective gate length model.

now establish the table for JTL current according to Eq.(2). Because $I_{\rm junc}$ depends solely on $V_{\rm ds}$, the established table that represents the variation of $I_{\rm junc}$ with $V_{\rm ds}$ is actually a one-dimension data array which stores the values of $I_{\rm junc}$ under different $V_{\rm ds}$. After such a table is established, $I_{\rm junc}$ can be obtained by searching the table according to the value of $V_{\rm ds}$ known from the circuit netlist.

Since the established table would include only limited data points, more data points which are not given in the table have to be obtained through interpolation methods. $I_{\rm junc}$ is only related to $V_{\rm ds}$, so one-dimensional interpolation is necessary. Commonly, the linear interpolation can be used to achieve good results. However, Figure 2 shows that $I_{\rm junc}$ grows severely with an increase of $V_{\rm ds}$, so the direct use of linear interpolation would generate large errors. As a consequence, we first get the logarithm of the $I_{\rm junc}$ so that for the majority of the values of given $V_{\rm ds}$, the linearity of the resultant logarithm curve is quite good for the use of piecewise linear interpolation to obtain satisfactory results. Nevertheless, when $V_{\rm ds}$ is relatively large, the linearity of the resultant logarithm becomes poor. Then the piecewise quadratic interpolation can be used to obtain accurate results.

### 2.2. Table look-up model for subthreshold leakage current

#### 2.2.1. Effective gate length model

In 65 nm technology, the minimum feature size is much smaller than the optical wavelength, causing a severe distortion of the rectangular-shaped gate, which has a significant impact on the subthreshold leakage current ($I_{\rm sub}$)[4,11]. Figure 3 shows a typical non-rectilinear gate profile. To obtain an accurate model for $I_{\rm sub}$, we have to first derive an effective gate length $L_{\rm eff}$ of this irregular gate.

For a given spatial period of irregularity, $W_0$, it can be disintegrated into several slices of different lengths and the same characteristic width $W_0$ along the width direction. Then the total subthreshold leakage ($I_{\rm tot}$) for this given shape of gate can be approximately expressed as the integration of $I_{\rm sub}$ of all the slices along the width direction, as shown in Eq.(3).

$$I_{\rm tot} = \sum_{i=1}^{N} I_i(L_i, W_0) = I(L_{\rm eff}, W), \tag{3}$$

where $L_{\rm eff}$ is given by

$$L_{\rm eff} = L_{\rm min} + \alpha \ln \frac{\sigma W}{W_0}, \tag{4}$$

where $\sigma$ is a fitting parameter, and

$$\sigma = \frac{\sqrt{\sum_{i=1}^{N} (L_i - \frac{\sum_{i=1}^{N} L_i}{N})^2}}{N}, \tag{5}$$

where $N$ is the total number of slices along the width direction. The value of $N$ depends on the actual process. $N$ can be made smaller for sophisticated technology and larger for less sophisticated technology. $L_i$ is determined by using scanning electron microscopy (SEM). Typically, the gate length shows random variation along the device width, which can be fitted by the Gaussian function.

#### 2.2.2. Compact physical model for subthreshold leakage current

Based on the effective gate length model, we can express $I_{\rm sub}$ as a function of $L_{\rm eff}$. We have fabricated [100] NMOSFETs with several different drawn gate lengths in 65 nm technology on the wafer of (100) substrate, and a tensile stress lager was deposited to examine the stress effects of $I_{\rm sub}$. Figure 4 shows the variation of $I_{\rm sub}$ with $V_{\rm ds}$ under different channel gate lengths when the gate voltage is zero. It is shown that the traditional model in Ref.[1] can accurately describe the behaviors of $I_{\rm sub}$ when the channel gate length is 300, 180, and 100 nm, respectively. However, for the 65 nm technology, the traditional model is completely inapplicable because $I_{\rm sub}$ grows more severely as $V_{\rm ds}$ increases. This can be understood as follows: for the 65 nm technology, the effect of drain induced barrier lowering becomes very serious. Moreover, the gate is not rectangular because of lithography as discussed in section 2.2.1. Both of the two factors lead to a large increase of $I_{\rm sub}$. In addition, the stress effects grow more seriously in short-channel devices and can not be neglected in the analysis of $I_{\rm sub}$ in 65 nm technology. Therefore, based on the traditional model, we propose a new model for $I_{\rm sub}$ in 65 nm technology in this work. We establish the new model as the function of $L_{\rm eff}$ instead of regular $L$, and explore layout parameters *SA* and *SB* to account for the stress effects of $I_{\rm sub}$ (Fig.5 (a)). By evaluating different values for these two parameters, the unsymmetrical stress effects of $I_{\rm sub}$ are, for the first time, included in our work (Fig.5 (b)). The proposed new model for $I_{\rm sub}$ is shown as

$$\begin{aligned} I_{\rm sub} = {} & \frac{\alpha_{\rm sub}\sqrt{q\varepsilon_{\rm si}N_{\rm cheff}(W^2+\alpha_W W)}}{(V_{\rm ds}^2+\alpha_{\rm ds1}V_{\rm ds}+\alpha_{\rm ds2})\exp(\alpha_{\rm L1}L_{\rm eff}^2+\alpha_{\rm L2}L_{\rm eff})} \\ & \times\left[1-\exp(-\frac{V_{\rm ds}}{V_{\rm T}})\right]\left[2-\exp\left(-\frac{SA}{SA_0}\right)\right. \\ & \left.-\exp\left(-\frac{SB}{SB_0}\right)\right]\exp\left(\frac{V_{\rm gs}-V_{\rm thlin}}{nV_{\rm T}}\right)(1+\alpha_{\rm bs}V_{\rm bs}). \end{aligned} \tag{6}$$

Table 1 shows the way of extracting the parameters in this model. The comparison of our model with the measured results in the typical condition ($V_{\rm bs}=0$, $V_{\rm gs}=0$) is shown in Fig.4. It is shown that our new model is in sheer agreement with the measured results.

#### 2.2.3. Fast table look-up model for $I_{\rm sub}$ simulation

As Equation (6) shows, $I_{\rm sub}$ depends on $V_{\rm ds}$, $V_{\rm gs}$ as well as $V_{\rm bs}$. Due to the complex expression for $I_{\rm sub}$, it takes much

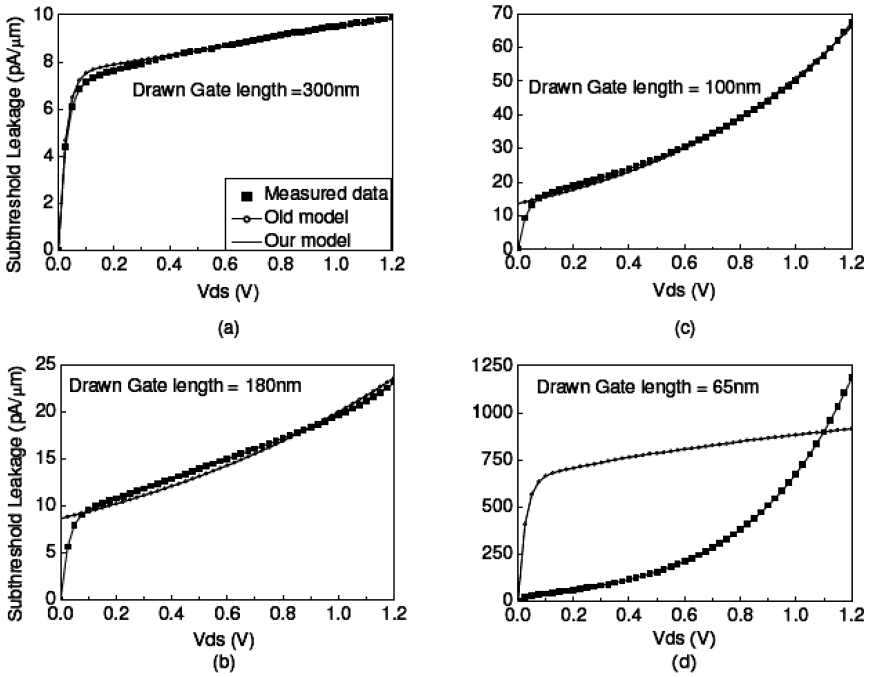


Fig.4. Comparison of the proposed subthreshold leakage current model with measurement results in the 65 nm process: (a) Drawn gate length = 300 nm; (b) Drawn gate length = 180 nm; (c) Drawn gate length = 100 nm; (d) Drawn gate length = 65 nm.

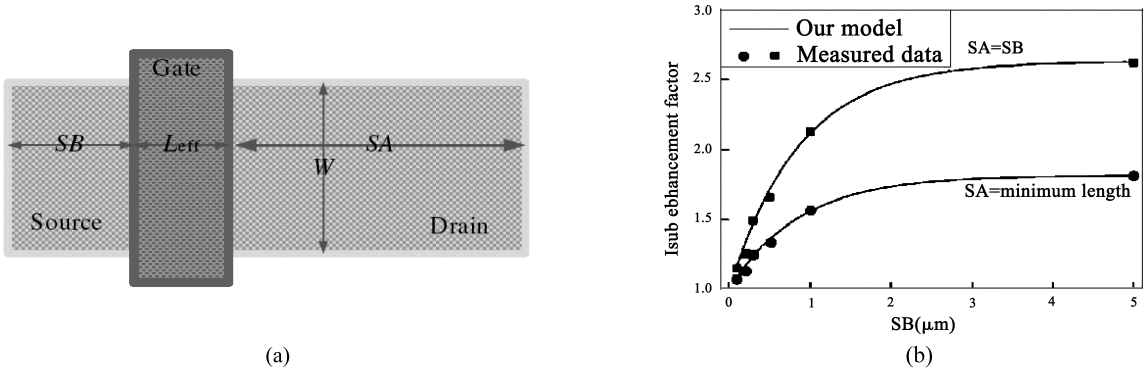


Fig.5. Layout parameters *SA* and *SB* explored in the proposed model: (a) *SA* and *SB* in the typical layout of MOSFET; (b) Comparison of our model results with measured data, both are normalized by the value of $I_{\rm sub}$ at *SA* = *SB* = minimum length.

more time to calculate $I_{\rm sub}$ by using the physical model. To reduce the simulation time, we develop a 3-D table for $I_{\rm sub}$ according to Eq.(6) to replace the previous complicated physical model. The superiority of using the table look-up model to conduct leakage current analysis can be clearly understood here. Once the table is established, the value of $I_{\rm sub}$ under a set of given $V_{\rm ds}$, $V_{\rm gs}$ and $V_{\rm bs}$ can be much more easily obtained through searching the 3-D table.

Since the table for $I_{\rm sub}$ needs 3-D data arrays, a 3-D Lagrange interpolation equation for our table model is developed as

$$g(x,y,z) = \sum_{i=0}^{n}\sum_{j=0}^{n}\sum_{k=0}^{n} g_{ijk}\Big(\prod_{\substack{s=0\\ s\neq i}}^{n}\frac{x-x_s}{x_i-x_s}\Big) \Big(\prod_{\substack{r=0\\ r\neq j}}^{n}\frac{y-y_r}{y_j-y_r}\Big)\Big(\prod_{\substack{t=0\\ t\neq k}}^{n}\frac{z-z_t}{z_k-z_t}\Big), \quad (7)$$

where $g_{ijk}$ is the value of the function when $x = i, y = j, z = k$.

If the point to be found is not in the table data, the 3-D interpolation is conducted to obtain the $I_{\rm sub}$ at this point by using the points nearby. Since the table or the data array for $I_{\rm sub}$ is three dimensional, there are eight points in the table around it, which construct a small cube. Therefore, the principle of the 3-D interpolation is to calculate the interpolation according to Eq.(1) by using eight vertexes of the small cube that encircles the point to be obtained. The linear interpolation can be used in every dimension to achieve good results. However, the relationship between $I_{\rm sub}$ and $V_{\rm gs}$ is exponential, which leads to extremely inaccurate results. Thus, we transform the exponential relationship to linear relationship by using the semi-logarithm coordinate in the $V_{\rm gs}$ dimension so that piecewise linear interpolation can be used to obtain satisfactory results. The semi-logarithm coordinate is also performed in the $V_{\rm ds}$ dimension for the same reason. Moreover, $I_{\rm sub}$ varies slowly with $V_{\rm bs}$, Thus, good results can be achieved through piecewise linear interpolation using the linear coordinate.

### 2.3. Spacing of data points

Two types of tables are available for table models, i.e. the uniform grid and the nonuniform grid. Though the uniform

Table 1. Extracting the parameters in this model.

| Step | Objective | Bias voltage | Selection of MOSFETs ($W^{\mu m}/L^{\mu m}$) |
|---|---|---|---|
| 1 | $\alpha_{ds1}, \alpha_{ds2}$ | $V_g = V_s = V_b$ = constant，$V_d$: 0−1.2V | 10/0.06 |
| 2 | $\alpha_{L1}, \alpha_{L2}$ | $V_g = V_s = V_b$ = constant，$V_d$ = 1.2V | 10/0.18,10/0.12,10/0.1,10/0.06,10/0.05 |
| 3 | $\alpha_{sub}, \alpha_W$ | $V_g = V_s = V_b$ = constant，$V_d$ = 1.2V | 1/0.06,0.6/0.06,0.3/0.06,0.12/0.06 |
| 4 | $\alpha_{bs}$ | $V_g = V_s = V_d$ = constant，$V_b$: 0−1.2V | 10/0.06 |
| 5 | $SA_0, SB_0$ | $V_g = V_s = V_b$ = constant，$V_d$ = 1.2V | $SA, SB$: 0.1，0.2，0.3，0.4，0.5，1.0 $\mu$m |

Table 2. Speedup and errors of the table look-up model for $I_{junc}$.

| Interpolation | Table size | Speedup | Average error | Max error |
|---|---|---|---|---|
| 1-D interpolation | 40 | 2.45X | 0.83% | 1.54% |
| | 60 | 2.42X | 0.62% | 0.95% |
| | 80 | 2.38X | 0.31% | 0.73% |
| | 100 | 2.36X | 0.29% | 0.57% |
| | 120 | 2.33X | 0.25% | 0.45% |

Table 3. Speedup and errors of table look-up model for $I_{sub}$.

| Interpolation | Table size | Speedup | Average error | Max error |
|---|---|---|---|---|
| 3-D Interpolation | $20 \times 8 \times 4$ | 2.67X | 1.25% | 1.94% |
| | $24 \times 12 \times 6$ | 2.65X | 0.78% | 1.53% |
| | $32 \times 16 \times 6$ | 2.62X | 0.54% | 1.27% |
| | $36 \times 20 \times 8$ | 2.59X | 0.39% | 1.11% |
| | $48 \times 24 \times 8$ | 2.58X | 0.31% | 1.07% |

voltage grid is fast and easy to implement, it would lead to large table size, making it almost impossible to be applied in many situations. This work uses the nonuniform grid because it is generally superior to uniform grid in terms of accuracy, performance, and memory requirement. We can set the appropriate number of data points according to the variation of leakage current with different voltages in different regions. For example, the accuracy requirement for analog and mixed signal simulation necessitate a fine grid in the $V_{gs}$ dimension for small gate voltages. Furthermore, because the bulk bias effects are very small and different bulk bias conditions would result in similar current characteristics, a relatively coarse voltage grid is sufficient in the $V_{bs}$ dimension.

## 3. Experimental results and discussion

The new table look-up models proposed in this paper have been implemented in the Hspice simulator. As discussed before, the proposed physical models are accurate for MOSFETs with different sizes in 65 nm technology, so we establish corresponding table models for MOSFETs with different $W$ and $L$ according to Eqs.(2) and (6). During the simulation stage, the simulator calculates the bias voltages and then calls the table models to obtain the corresponding leakage current. Our table look-up models have been tested on several large-scale industry circuits and obtained good results.

Table 2 shows the speedup and errors of using the presented table look-up models to calculate $I_{junc}$. The notation "40" in the second column represents a table which has 40 grids points in the $V_{ds}$ dimension. The third column shows the speedup of the simulation time of the new table look-up model compared with the traditional physical model. It is shown that the average speedup using the table look-up model is 2.39X. Note that the speedup of our model is little influenced by the variation of table size. The fourth and fifth column are the average and maximums errors of using our table look-up model for $I_{junc}$ analysis under different table sizes, respectively. It can be observed that the 1-D interpolation causes only small errors. Thus, the new table look-up model for $I_{junc}$ provides very accurate results. The influence of the table size on the table look-up model accuracy can be also seen in Table 2. It is shown that the accuracy of the table look-up model improves with the increase of the table size. However, when the table size grows to a certain scale, the speed of the accuracy improvement grows slowly. Therefore, there is a tradeoff between simulation accuracy and memory consumption.

The speedup and errors of using the presented table look-up models to calculate $I_{sub}$ are shown in Table 3. The notation "$20 \times 8 \times 4$" in the second column represents a table which has 20 grid points in $V_{ds}$ dimension, 8 points in $V_{gs}$ dimension, and 4 points in $V_{bs}$ dimension, respectively. This also means that the total number of data points stored in memory is 640. We can see from Table 3 that the speedup of the model for $I_{sub}$ (average 2.62X) is higher than that for $I_{junc}$.This is because that the calculation of $I_{sub}$ using the physical model consumes more time due to its more complex expression. In addition, the 3-D interpolation generates similarly small errors, and its accuracy also improves with an increase of table size. However, the tradeoff between accuracy and memory space becomes more serious here. The reason is that the 3-D data arrays with large table size take up much more memory space than does the 1-D data table.

## 4. Conclusion

New compact physical models for subthreshold leakage current and junction tunneling leakage current, which consider the process variations and novel effects in the nano-scaled process, are proposed in this paper. Novel table look-up models for leakage current analysis in 65 nm technology are then developed by using the appropriate interpolation techniques based on the presented physical models. Simulation results show that the new physical models can accurately estimate the leakage current in 65 nm technology and the use of the new table look-up models for leakage current analysis can achieve 2.5X speedup on average in this paper.

## References

[1] Mukhopadhyay S, Member S, Raychowdhury A, et al. Accurate estimation of total leakage in nanometer-scale bulk CMOS circuits based on device geometry and doping profile. IEEE Trans CAD, 2005, 24(3): 363

[2] Chudzik M, Doris B, Mo R, et al. High-performance high-*k*/metal gates for 45 nm CMOS and beyond with gate-first processing. Proc VLSI Tech, 2007: 194

[3] Agarwal K, Nassif S. Characterizing process variation in nanometer CMOS. Proc DAC, 2007: 396

[4] Singhal R, Balijepalli A, Subramaniam A, et al. Modeling and analysis of non-rectangular gate for post-lithography circuit simulation. Proc DAC, 2007: 823

[5] Meijer P B. Fast and smooth highly nonlinear multidimensional table models for device modeling. IEEE Trans Circuits Syst, 1990, 37(3): 335

[6] Schrom G, Stach A, Selberherr S. An interpolation based MOSFET model for low-voltage applications. Microelectron J, 1998, 29: 529

[7] Bourenkov V, McCarthy K G, Mathewson A. A hybrid table/analytical approach to MOSFET modeling. Proc Int Conf Microelectron Test Structures, Monterey, CA, 2003: 142

[8] Yang B, McGaughy B. An essentially non-oscillatory (ENO) high-order accurate adaptive table model for device modeling. Proceedings of the 41st Annual Conference on Design Automation, 2004: 864

[9] Bourenkov V, McCarthy K G, Mathewson A. MOS table models for circuit simulation. IEEE Trans Comput-Aided Des Integr Circuits Syst, 2005, 24(3): 352

[10] Fang G P, Yeh D C, Zweidinger D, et al. Fast, accurate MOS table model for circuit simulation using an unstructured grid and preserving monotonicity. Proceedings of the 2005 Conference on Asia South Pacific Design Automation, 2005: 1102

[11] Heloue K R, Azizi N, Najm F N. Modeling and estimation of full-chip leakage current considering within-die correlation. Proc DAC, 2007: 93