Silicide-block-film effects on high voltage drain-extended MOS transistors

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Abstract: Silicide-block-film effects on drain-extended MOS (DEMOS) transistors were comparatively investigated, by means of different film stack stoichiometric SiO_2 and silicon-rich oxide (SRO). The electrical properties of the as-deposited films were evaluated by extracting source/drain series resistance. It was found that the block film plays a role like a field plate, which has significant influence on the electric field beneath. Similar to hot-carrier-injection (HCI) induced degradation for devices, the block film initially charged in fabrication process also strongly affects the device characteristics and limits the safe operating area.

Key words: DEMOS; silicide-block-film; field plate
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1. Introduction

Today, high-voltage (HV) devices compatible with a standard CMOS process have become an accessible solution for power integrated circuits in automotive and consumer applications[1]. In the general class of HV devices, two different structures can be distinguished. The first type does not contain a field oxide, and a silicide-block-film on the drift region is required to ensure high voltage capability. This device is illustrated in Fig. 1(a) and is always referred to as the drain-extended MOS (DEMOS). The second type is known as the lateral double-diffused MOS (LDMOS), in which a field oxide is grown within the drift region to reduce the fringing fields at the gate edge.

Despite the different topology structures, HV devices commonly exhibit some specific features due to the high electric field handled, e.g. the impact-ionization effect. The works by Landgraf *et al.*[2] and Wang *et al.*[3] demonstrated that the extra electron-hole pairs could also generate in the drift region, which will cause the substrate current rising again with gate voltage increasing. Recent reports[4–6] also showed the potential reliability issues because of the two-peak substrate current. It has been clarified that there are two hot-carrier-injection (HCI) mechanisms: one at the channel edge and another occurring in the drift region not overlapped by the gate electrode. The device characteristics can be strongly affected by hot carrier injecting into the insulating oxide in the drift region. On the other hand, smart power ICs usually employ various silicide-block-film stacks for the integrated microelectronic devices, for example the one-time-programmable memory cells using thicker block film as the charge barrier layer[7]. Nevertheless, the impact of different block films on DEMOS transistors has not been extensively studied.

In this paper, we report the silicide-block-film effects on DEMOS transistors for the first time. First, the electrical properties of block films are evaluated by means of the extracted series resistance. The 2-D device simulator Medici provided the physical insights on the electric field distribution under the insulating oxide. Then the DC parameters of DEMOS transistors are comparatively studied and explained, including the substrate current, saturation current and breakdown voltage. It is demonstrated that the block film with trapped charges acts like a field plate, which strongly impact electric field beneath and device characteristics.

2. Devices and experiments

Figure 1 (a) shows the cross-section schematic of an n-channel DEMOS transistor, and Figure 1 (b) is the SEM image of a real structure. The thickness of gate oxide is 80 nm and the channel length (L_{ch}) is 2 μm. The distance between the drain and the channel (L_{dft}) is 1.2 μm. The drift region is lightly doped to sustain breakdown voltage higher than 30 V. Here, a block film on the drift region is employed to prevent the silicide formation. Based on the drain-extended technique, DEMOS transistor fabrication is compatible with the standard CMOS technology.

To investigate the silicide-block-film effects on DEMOS transistors, we arranged three samples with different block films as shown in Table 1. All block layers in this study were deposited by plasma enhanced chemical vapour deposition (PECVD) with thickness about 1500 Å. The silicon-rich oxide (SRO) were deposited using N_2O and SiH_4 as reactant gases and the gas flow ratio R_0 = $[N_2O]/[SiH_4]$ = 10. All samples

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Table 1. Samples used to investigate the silicide-block-film impact.

Sample	SA1	SA2	SA3
Block film material	PECVD 1500 Å SiO_2	PECVD 350 Å SiO_2 + 1150 Å SRO	PECVD 1500 Å SRO

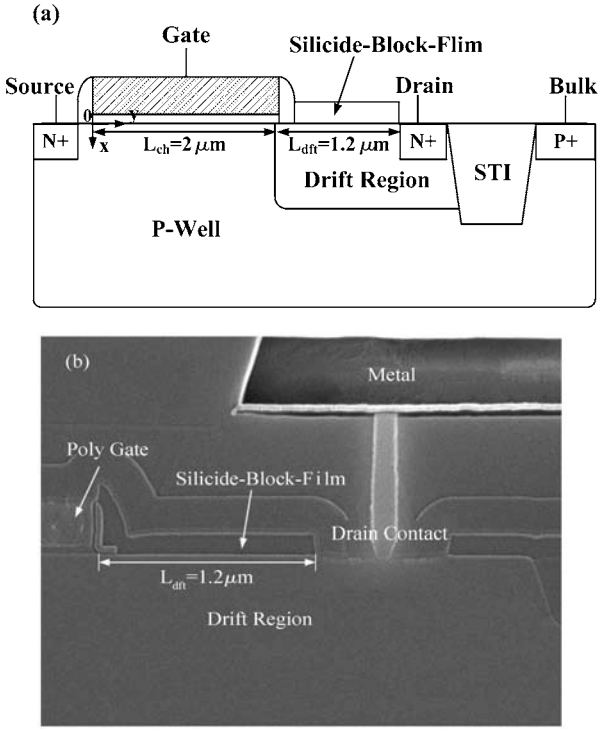

Fig. 1. Device structure of an n-channel DEMOS transistor: (a) Cross-section schematic; (b) SEM image of real structure.

were alloyed at 410 °C for 30 min in 100% hydrogen ambient to passivate dangling bonds at the Si/SiO_2 interface.

3. Results and discussion

3.1. Film properties and electric field beneath

To evaluate the block film electrical properties in real structures, we primarily compared the device characteristics in the triode region. The linear current and transconductance versus gate voltage curves are depicted in Fig. 2, respectively. It is shown that there are no significant differences in the sub-threshold region, or at the peak transconductance point, implying that the intrinsic channel region has not been impacted much by the block films. However, when gate voltage goes high, the linear current and transconductance curves deviate a little (SA1 > SA2 > SA3), which is known as the effect of source/drain series resistance (R_{sd}). Unlike the traditional MOS transistors, the DEMOS R_{sd} value is in fact modulated by the gate voltage due to the lightly doped drift region. To further clarify the deviation in the transfer curves, we extracted the gate-bias dependent R_{sd} through the methodology proposed by Ho[8]. As shown in Fig. 3, R_{sd} decreases as the gate bias increases, and the R_{sd} value for different samples is SA1 < SA2 < SA3. The R_{sd} increasing for different samples can be explained by the charge trapping effect of block layer. SRO is a two-phase material, with excess Si nanocrystals or nanoclusters (NCs) embedded in the SiO_2 matrix[9]. And it

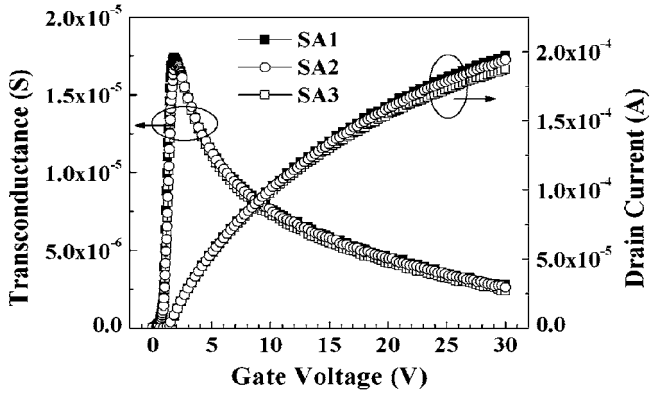

Fig. 2. Measured transconductance and drain current versus gate voltage curves at V_d = 0.1 V of samples SA1, SA2 and SA3.

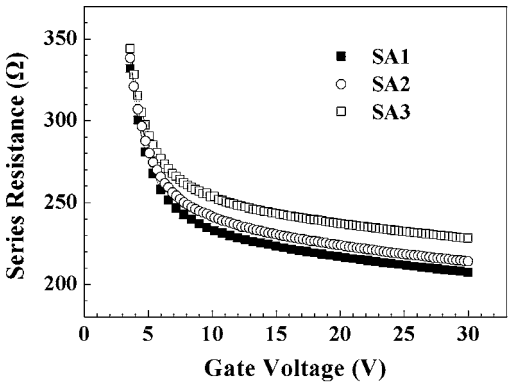

Fig. 3. Extracted source/drain series resistance versus gate voltage curves of samples SA1, SA2 and SA3.

is reported that the trapped charge density can be as high as 1×10^{12} cm^{-2} depending on the excess Si content and post thermal treatment[10]. Thus, it is reasonable to speculate that during the deposition process or subsequent annealing steps, there is a net negative charge trapping in the SRO layers, consequentially causing the R_{sd} higher.

For DEMOS transistors capped with block films, the electric field along the drift region should be influenced by the trapped charges above. Taking into account the two-dimensional effects, the electric field distribution is simulated by the numerical simulator Medici[11]. Here, the silicide-block-film is defined as an electrode totally containing 1×10^4 electrons or holes, and the charge magnitude is consistent with the trap density in SRO reported in Ref. [10]. Figures 4(a) and 4(b) show the electric potential contours with different block films under drain and gate voltage (V_d and V_g) of 30 V: the block film is supposed ideal in Fig. 4(a) and contains 1×10^4 electrons in Fig. 4(b). Compared with each other, the electric potential lines in Fig. 4(b) are sparser at the channel/drift junction boundary, and are more crowding at the block film edge. If further looking at the extracted electric field in Fig. 4(c), we can find that the block film with negative charges plays a role like a field plate with reverse bias[12]. The electric field at

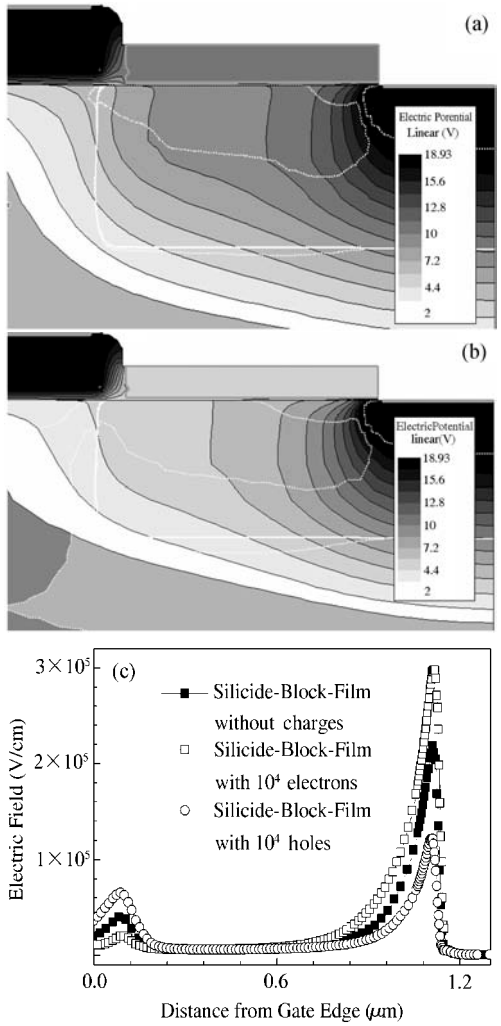

Fig. 4. Electric potential and electric field distribution with different block films under $V_d = V_g = 30$ V: (a) Electric potential contours with block film containing no charges; (b) Electric potential contours with block film containing 1×10^4 electrons; (c) Electric field distribution along the drift region with block film containing no charges, 1×10^4 electrons or holes.

the channel edge (E_{ce}) is released because the negative charges help deplete the drift region; meanwhile the field at the edge of block film (E_{fe}) is higher bearing some similarity to the effect that would occur at the radius of a planar junction. For block film with positive charges, the result is on the contrary.

3.2. Device characteristics

Based on the electric field analysis through simulation, the device DC characteristics are comparatively studied and explained. It is demonstrated that the silicide-block-film has significant influence on DEMOS transistors.

The substrate current versus gate voltage curves are depicted in Fig. 5. Obviously, for the first peak substrate current, SA1 > SA2 > SA3; while for the second peak, SA1 < SA2 < SA3, the substrate current of SA3 even gets to the current limiting. The difference between the substrate current curves can be explained by the electric field distribution beneath the insulating oxide. Firstly, let us look at the mechanisms for the two-peak substrate current[3]. When V_g is low, the first peak mainly

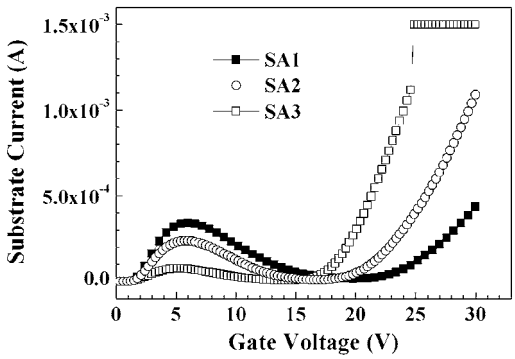

Fig. 5. Measured substrate current versus gate voltage curves at V_d = 30 V of samples SA1, SA2 and SA3.

comes from the impact ionization occurring at the pinch-off region near the gate edge; as V_g increases, the injected electron charge density becomes larger than the net doping concentration of drift region, as a result the depletion region at the channel/drift boundary cannot be maintained and the highest electric field shifts towards the n^+ drain. Therefore, the impact ionization near n^+ drain takes the main contribution to the second peak substrate current. According to the classical theory[13], the substrate current can be described as

$$\begin{aligned} I_b &= I_{b1} + I_{b2} \\ &= \int_0^{L_{ch}} I_d A_i e^{-\frac{B_i}{E_{ce}}} dy + \int_{L_{ch}}^{L_{ch}+L_{dft}} I_d A_i e^{-\frac{B_i}{E_{fe}}} dy, \end{aligned} \quad (1)$$

where I_d is the drain current, and A_i and B_i are associated with the impact ionization rate. The item I_{b1} and I_{b2} represent the first peak and second peak substrate current respectively. For most regions (the inversion channel or the neutral drift region), the electric field is so low that $\exp(-B_i/E) \approx 0$. The substrate current is mainly determined by the maximum electric field occurring at the channel edge or at the block film edge (E_{ce} or E_{fe}). Thus, for SA3 capped with SRO, the E_{ce} has been released and E_{fe} has been reinforced, consequentially the first peak substrate current becomes lower and the second goes higher. As for SA1 and SA2, the effect is also in agreement with the measurement data in Fig. 5.

Due to the two-stage impact ionization phenomenon, substrate current induced body effect (SCBE) becomes remarkable for DEMOS transistors. As shown in Fig. 6, when V_d is high, the saturation current is noticeably affected by the body effect. The region Ⅰ and region Ⅱ correspond to the first peak and second peak substrate current, respectively. The saturation current in Fig. 6(b) (SA2) goes more smooth in region Ⅰ, and turns up more quickly in region Ⅱ compared with SA1 in Fig. 6(a). As for SA3 in Fig. 6(c), the device even burns out, induced by the parasitic bipolar (source-well-drift region) turn on because of the highest substrate current. This limits the safe operating area for HV devices.

The impact of block films can be also observed in the breakdown characteristics. Interestingly, as shown in Fig. 7, the breakdown voltage goes up with the negative charge increasing (SA1 < SA2 < SA3). This is attributed to the two different and competing breakdown locations. It is known that

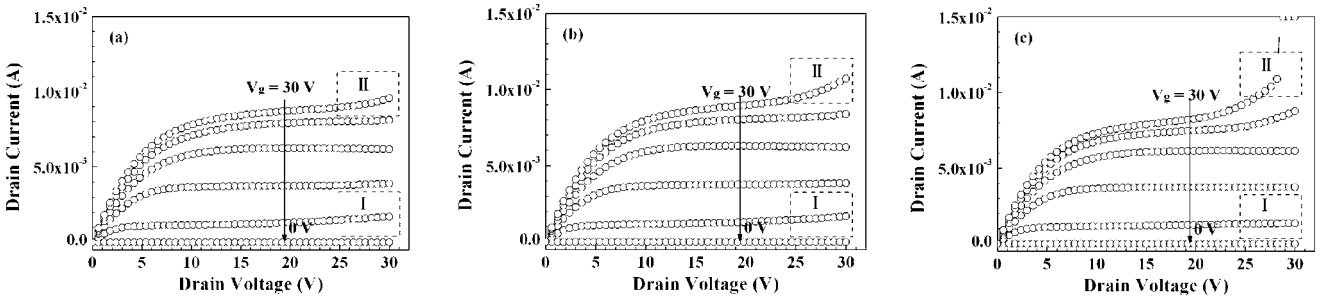

Fig. 6. Measured output characteristics of different samples: (a) SA1; (b) SA2; (c) SA3. The regions Ⅰ and Ⅱ correspond to the first peak and second peak substrate current, respectively.

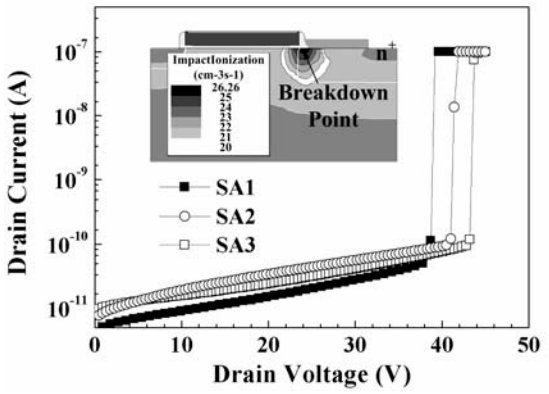

Fig. 7. Measured drain current versus drain voltage curves at $V_g = 0$ of samples SA1, SA2 and SA3.

the E_{ce} and E_{fe} determine the two possible breakdown points. For a real field plate with strong reverse bias, E_{fe} is always larger than E_{ce}, and the breakdown point will shift to the field plate edge. However, for the block film with limited trapped charges, E_{fe} is still smaller than E_{ce} under off state. This is verified by Medici simulator in the inset of Fig. 7. It is shown that under $V_d = 40$ V and $V_g = 0$ V, the breakdown point still occurs at the channel edge. Since the electric field at this location has been released, the breakdown voltage will increase.

4. Conclusion

In summary, the silicide-block-film effects on the DEMOS transistors were investigated in this paper. By means of the 2-D simulator Medici, it was found that the block film with trapped charges acts like a field plate, which strongly affects the electric field beneath. Then, the device DC characteristics were well evaluated and explained, including the substrate current, saturation current and breakdown voltage. Similar to HCI induced degradation for devices, the block film initially charged in fabrication process also has significant impact on device performances. This highlights the necessity to carefully select the block film material, or optimize layout design rules (e.g. L_{dft}) for DEMOS transistors in HV ICs.

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