Low voltage bandgap reference with closed loop curvature compensation

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Abstract: A new low-voltage CMOS bandgap reference (BGR) that achieves high temperature stability is proposed. It feeds back the output voltage to the curvature compensation circuit that constitutes a closed loop circuit to cancel the logarithmic term of voltage V_{BE}. Meanwhile a low voltage amplifier with the 0.5 μm low threshold technology is designed for the BGR. A high temperature stability BGR circuit is fabricated in the CSMC 0.5 μm CMOS technology. The measured result shows that the BGR can operate down to 1 V, while the temperature coefficient and line regulation are only 9 ppm/°C and 1.2 mV/V, respectively.

Key words: bandgap reference; low voltage reference; curvature compensation
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1. Introduction

Bandgap reference (BGR) is the most widely used in various analog and digital systems. Its performance and accuracy are very important. With increasing resolution of data converter systems and scaling down supply voltage, the low voltage and high temperature stability BGR are in great demands. Many techniques have been given[1–6] to achieve this goal. Some techniques are based on more complex fabrication processes, which are expensive, such as BiCMOS. Some concentrate on canceling the high-T terms of the Taylor series of the base–emitter voltage (V_{BE}) of a bipolar transistor. But all of those techniques mentioned above are based on open loop curvature compensation which can only guarantee a relatively high accuracy.

A new closed loop curvature compensation scheme is proposed in this paper. We create a closed loop circuit which can feed back the output voltage to the curvature compensation circuit. In the closed loop, the lower of temperature coefficient (TC) of output voltage is, the better the curvature compensation circuit could counteract the logarithmic term of V_{BE} of a bipolar transistor. On the other hand, the better the BGR counteracts the logarithmic term of V_{BE}, the lower TC of output voltage could be. So we can repeatedly regulate the compensation resistors in order to improve temperature stability of BGR. Finally, we can completely cancel the logarithmic term of V_{BE} of a bipolar transistor. Based on this technique, a practical circuit is demonstrated.

2. General principles of bandgap references

The relationship of base-emitter voltage to temperature can be expressed as[7]

$$V_{BE}(T) = V_G(T_r) - \frac{T}{T_r}V_G(T_r) + \frac{T}{T_r}V_{BE}(T_r) - \eta\frac{kT}{q}\ln\frac{T}{T_r} + \frac{kT}{q}\ln\frac{I_C(T)}{I_C(T_r)}, \quad (1)$$

where $V_G(T_r)$ is the bandgap voltage at temperature T_r, η is a constant depending on technology, which $\eta = 4 - n$ (n is a appropriate constant), q is the charge of an electron, $I_C(T)$ is the collector current injected into the bipolar transistor, and k is the Boltzman constant.

The principle of a BGR is to compensate the negative temperature coefficient of the voltage $V_{BE}(T)$ with the positive one of $V_{BE}(T)$. A typical CMOS BGR is shown in Fig. 1.

The voltage V_{ref} of BGR can be given by

$$V_{ref} = V_{EB3} + \frac{R_2}{R_1}\frac{kT}{q}\ln\frac{A_1}{A_2}, \quad (2)$$

where A_1 and A_2 are the emitter areas of Q1 and Q2, respectively. If R_1 and R_2 are carefully selected, the first-order T term of V_{BE} can be cancelled.

3. Closed loop curvature compensation technique

The idea of the proposed curvature-compensation technique is illustrated in Fig. 2. A closed loop is created which contains OTA3, OTA4 and transistors M5–M8, M10, and bipolar transistor Q4. OTA4 and R_5 convert the output voltage of V_{ref} to current which is copied by mirror-current of M6 and M10. Then bipolar transistor Q4 and resistor R_3 can generate

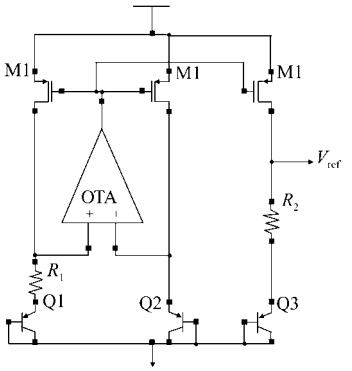

Fig. 1. Typical CMOS BGR.

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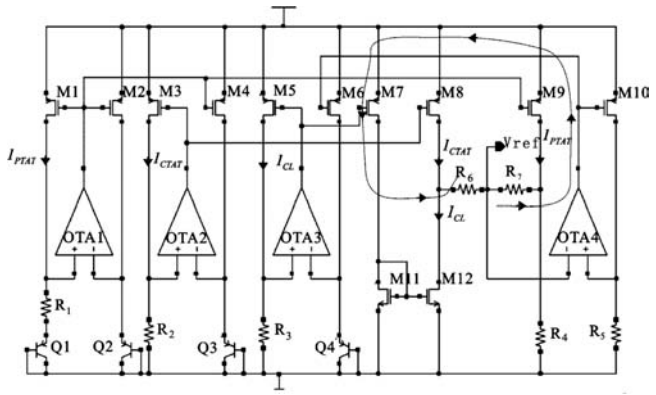

Fig. 2. Bandgap reference circuit.

current I_{CL}. Meanwhile we use I_{PTAT} to get current I_{CTAT}. In the closed loop, we repeatedly regulate the compensation resistors R_2 and R_3 so that the logarithmic term of I_{CL} can counteract that of I_{CTAT}. Finally, we can design high temperature stability BGR.

Figure 2 shows that voltage $V+$ of the operational amplifier (OTA) is equal to $V-$ because of feedback function of OTA. According to Eq. (1), a positive temperature current of V_{BE} can be given by

$$I_{\mathrm{PTAT}} = \frac{V_{\mathrm{BE2}} - V_{\mathrm{BE1}}}{R_1} = \frac{\Delta V_{\mathrm{BE}}}{R_1} = \frac{V_{\mathrm{T}} \ln n}{R_1} = \frac{kT}{q}\frac{\ln n}{R_1}, \tag{3}$$

where n is the ratio of the emitter areas of Q1 and Q2.

Transistors M2 and M4 are the mirror-current to copy the current I_{PTAT}. Then according to Eq. (1), we can get

$$I_{\mathrm{CTAT}} = \frac{1}{R_2}\left(V_{\mathrm{G}}(T_{\mathrm{r}}) - \frac{T}{T_{\mathrm{r}}}V_{\mathrm{G}}(T_{\mathrm{r}}) + \frac{T}{T_{\mathrm{r}}}V_{\mathrm{BE}}(T_{\mathrm{r}}) - \eta\frac{kT}{q}\ln\frac{T}{T_{\mathrm{r}}} + \frac{kT}{q}\ln\frac{I_{\mathrm{C3}}(T)}{I_{\mathrm{C3}}(T_{\mathrm{r}})}\right). \tag{4}$$

As the current I_{C3} equals I_{PTAT} which is proportional to temperature (see Eq.(3)), Equation (4) can be simplified by

$$I_{\mathrm{CTAT}} = \frac{1}{R_2}\left(V_{\mathrm{G}}(T_{\mathrm{r}}) - \frac{T}{T_{\mathrm{r}}}V_{\mathrm{G}}(T_{\mathrm{r}}) + \frac{T}{T_{\mathrm{r}}}V_{\mathrm{BE}}(T_{\mathrm{r}}) - \eta\frac{kT}{q}\ln\frac{T}{T_{\mathrm{r}}} + \frac{kT}{q}\ln\frac{T}{T_{\mathrm{r}}}\right). \tag{5}$$

Meanwhile, a closed loop is created which is shown in Fig. 2. OTA4 and R_5 convert the voltage V_{ref} to current which is copied by mirror-current of M6 and M10. According to Eq. (1), I_{CL} can be expressed by

$$I_{\mathrm{CL}} = \frac{1}{R_3}\left(V_{\mathrm{G}}(T_{\mathrm{r}}) - \frac{T}{T_{\mathrm{r}}}V_{\mathrm{G}}(T_{\mathrm{r}}) + \frac{T}{T_{\mathrm{r}}}V_{\mathrm{BE}}(T_{\mathrm{r}}) - \eta\frac{kT}{q}\ln\frac{T}{T_{\mathrm{r}}} + \frac{kT}{q}\ln\frac{I_{\mathrm{C4}}(T)}{I_{\mathrm{C4}}(T_{\mathrm{r}})}\right). \tag{6}$$

Because of feedback function of OTA4, the current I_{C4} of collector current of the bipolar transistor Q4 can be given by

$$I_{\mathrm{C4}} = I_{\mathrm{M10}} = \frac{V_{\mathrm{ref}}}{R_5}, \tag{7}$$

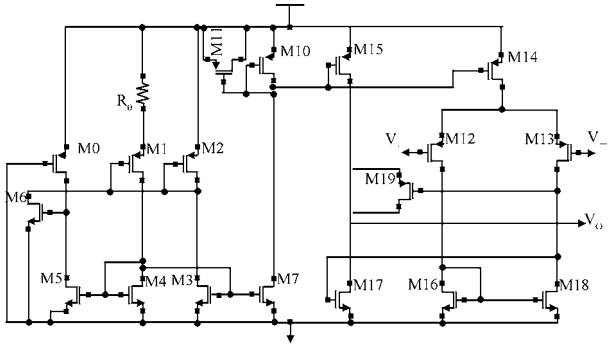

Fig. 3. Operational amplifier.

where resistor R_5 is a constant. If voltage V_{ref} was insensitive to variations in temperature I_{C4} would be a constant current. Therefore Equation (6) can be simplified by

$$I_{\mathrm{CL}} = \frac{1}{R_3}\left(V_{\mathrm{G}}(T_{\mathrm{r}}) - \frac{T}{T_{\mathrm{r}}}V_{\mathrm{G}}(T_{\mathrm{r}}) + \frac{T}{T_{\mathrm{r}}}V_{\mathrm{BE}}(T_{\mathrm{r}}) - \eta\frac{kT}{q}\ln\frac{T}{T_{\mathrm{r}}}\right). \tag{8}$$

In order to cancel $V_{\mathrm{T}}\ln\dfrac{T}{T_{\mathrm{r}}}$, we have

$$I_{\mathrm{CTAT}} - I_{\mathrm{CL}} = \left(\frac{1}{R_2} - \frac{1}{R_3}\right)V_{\mathrm{G}}(T_{\mathrm{r}}) + \left(\frac{1}{R_2} - \frac{1}{R_3}\right)\frac{T}{T_{\mathrm{r}}}\left[V_{\mathrm{BE}}(T_{\mathrm{r}}) - V_{\mathrm{G}}(T_{\mathrm{r}})\right] - \left(\frac{\eta - 1}{R_2} - \frac{\eta}{R_3}\right)\frac{kT}{q}\ln\frac{T}{T_{\mathrm{r}}}. \tag{9}$$

Assume we set up R_2 and R_3 to cancel the last term of Eq. (9) as follows:

$$\frac{R_2}{R_3} = \frac{\eta - 1}{\eta}. \tag{10}$$

Then Equation (9) can be expressed by

$$I_{\mathrm{CTAT}} - I_{\mathrm{CL}} = \left(\frac{1}{R_2} - \frac{1}{R_3}\right)V_{\mathrm{G}}(T_{\mathrm{r}}) + \left(\frac{1}{R_2} - \frac{1}{R_3}\right)\frac{T}{T_{\mathrm{r}}}\left[V_{\mathrm{BE}}(T_{\mathrm{r}}) - V_{\mathrm{G}}(T_{\mathrm{r}})\right]. \tag{11}$$

According to Eq. (11), the current is only including the first-order T term of temperature which can be compensated by current I_{PTAT}. In Fig. 2, we get

$$V_{\mathrm{ref}} = \left(\frac{1}{R_2} - \frac{1}{R_3}\right)V_{\mathrm{G}}(T_{\mathrm{r}})(R_4 + R_7) + \left(\frac{1}{R_2} - \frac{1}{R_3}\right)\frac{T}{T_{\mathrm{r}}}\left[V_{\mathrm{BE}}(T_{\mathrm{r}}) - V_{\mathrm{G}}(T_{\mathrm{r}})\right](R_4 + R_7) + \frac{kT}{q}\frac{\ln n}{R_1}R_4. \tag{12}$$

Therefore we have

$$f(T) = \frac{\partial V_{\mathrm{ref}}}{\partial T} = \left(\frac{1}{R_2} - \frac{1}{R_3}\right)\frac{1}{T_{\mathrm{r}}}\left[V_{\mathrm{BE}}(T_{\mathrm{r}}) - V_{\mathrm{G}}(T_{\mathrm{r}})\right](R_4 + R_7) + \frac{k}{q}\frac{\ln n}{R_1}R_4. \tag{13}$$

To set up proper R_4 and R_7 to make sure $f(T) = 0$. We can get a constant voltage V_{ref} which meets the requirement of simplification of Eq. (6).

$$V_{\mathrm{ref}} = \left(\frac{1}{R_2} - \frac{1}{R_3}\right)V_{\mathrm{G}}(T_{\mathrm{r}})(R_4 + R_7). \tag{14}$$

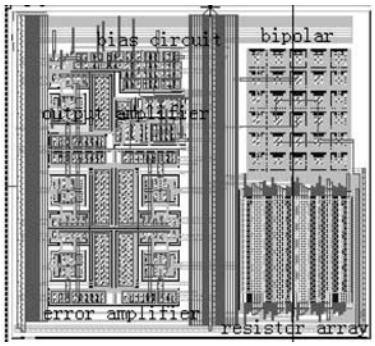

Fig. 4. Layout of circuit.

Table 1. Simulation results of OTA.

Parameter	Value
DC gain	50 dB
UGB (1p)	0.3 MHz
Phase margin	80
Power consumption	14 μW
Power voltage	1.5 V

From the analysis above, we found that a high temperature stability BGR could achieve only if we could remove the logarithmic term of $I_{CL} - I_{CTAT}$ completely (reference Eqs. (9)–(11)). Therefore the ratio of resistor R_2 and R_3 is key element of the circuit.

Figure 3 shows the operational amplifier circuit. All CMOS transistors are low threshold transistors. The threshold voltage of NMOS and PMOS transistors are 0.50 and 0.66 V, respectively. It is composed of three parts, i.e. startup circuit, bias circuit and two-stage amplifier. The startup circuit contains M0, M5 and M6 transistors. When the OTA starts up, M0 and M6 turn on, which provides a small current to flow through M2. Once the bias circuit works, the M5 turns off M6. Bias circuit is composed of M1–M4 transistors and resistor R_0, which provides a reference voltage for operational amplifier. Two stages operational amplifier includes M12–M18 transistors, and the PMOS transistor M19 is Miller compensation capacitor. Although the linearity of MOS capacitor is worse, compared to PIP capacitor the cost is nearly 10% lower; in this application the linearity is not very important. Therefore the MOS capacitor is used as compensation capacitor in the circuit. The simulation results are shown in Table 1.

4. Layout and results

The circuit was fabricated in CSMC 0.5 μm CMOS technology. The layout of BGR circuit contains resistor array, bipolar transistor, error amplifier, output amplifier and bias circuit, shown in Fig. 4. The resistor is P+ resistor. The area is about 0.16 mm^2.

The measured result shows that the temperature coefficient can achieve 9 ppm/°C over temperature range from 16 to 120 °C, which is much higher than simulation result of 0.92 ppm/°C. The main reason is mismatch of R_2/R_3 (Eq. (10)), which is about 1% in CMOS technology. If we assume the mismatch of R_2/R_3 is 1%, the simulation result shows that

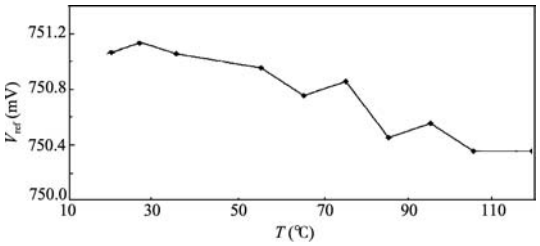

Fig. 5. V_{ref} variation with temperature.

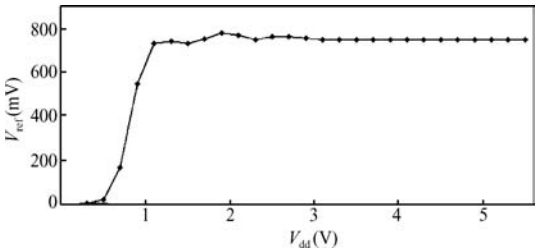

Fig. 6. V_{ref} variation with supply voltage.

the temperature coefficient would be as high as 7 ppm/°C. So trimming resistor could be used in order to improve the temperature coefficient in advanced. However, for saving cost we could also get a relatively small temperature coefficient without trimming resistor.

Compared with the proposed circuit in Ref. [6], our BGR can achieve a much lower TC. The output voltage over the temperature range is nearly between 750.4 and 751.1 mV in circuit proposed in this paper as shown in Fig. 5. The variation in V_{ref} with supply voltage is plotted in Fig. 6. The circuit achieved a line regulation performance of 1.2 and 8 mV/V for $3 < V_{DD} < 5.5$ V and $1 < V_{DD} < 5.5$ V (V_{DD} is power voltage) respectively.

5. Conclusion

Compared to other low voltage and open loop curvature compensation BGR, a new structure of closed loop curvature compensation is proposed. We create a closed loop circuit to cancel the logarithmic term of voltage V_{BE} which can achieve quite high temperature stability. Meanwhile a low voltage OTA with low threshold technology is designed to achieve a low voltage BGR with a fairly small TC in the low cost 0.5 μm CMOS technology.

The circuit is fabricated in the CSMC 0.5 μm CMOS technology. The measured results show that it can operate down to 1 V, while the temperature coefficient and the line regulation are only 9 ppm/°C and 1.2 mV/V, respectively. So we design a low voltage BGR with high temperature stability in the low cost 0.5 μm technology which can integrate in low voltage chips for many applications.

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