Modeling and analysis of power extraction circuits for passive UHF RFID applications*

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Abstract: Modeling and analysis of far field power extraction circuits for passive UHF RF identification (RFID) applications are presented. A mathematical model is derived to predict the complex nonlinear performance of UHF voltage multiplier using Schottky diodes. To reduce the complexity of the proposed model, a simple linear approximation for Schottky diode is introduced. Measurement results show considerable agreement with the values calculated by the proposed model. With the derived model, optimization on stage number for voltage multiplier to achieve maximum power conversion efficiency is discussed. Furthermore, according to the Bode-Fano criterion and the proposed model, a limitation on maximum power up range for passive UHF RFID power extraction circuits is also studied.

Key words: power extraction circuits; passive UHF RFID; model; voltage multiplier; power conversion efficiency; power up range

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1. Introduction

Due to the advantage of long operating range and low cost, ultra-high-frequency (UHF) radio frequency identification (RFID) applications have increased rapidly[1]. Passive RFID systems require contactless transmission of both the information and the power between transponder and reader. The RF energy radiated by the reader is used both to supply the passive UHF RFID transponder and to allow data transmission from the transponder to the reader through modulation of the backscattered radiation[2].

A voltage multiplier is typically used to rectify the incident alternating RF voltage and recover a DC supply voltage. In the application of UHF RFID transponders, the voltage multiplier is also utilized to detect the envelope of incident alternating RF voltage as an important functional block of demodulation circuit[3,4]. Thus, it can be concluded that the characteristics of RF section of UHF RFID transponder are strongly determined by the characteristics of voltage multiplier, which should be studied with more attention. Traditionally, voltage multipliers use the principle of Dickson's charge pump[5]. In order to reduce fabrication cost, diode-connected MOS transistors with a threshold voltage which can be decreased around 0.1 V are used for the voltage multiplier[6−10]. However, special care must be taken to minimize the substrate losses and parasitic capacitance of MOS transistors, which greatly reduce the RF-to-DC conversion efficiency. Schottky diodes, due to their excellent high frequency performance, low substrate losses and very fast switching, are the preferable choice for voltage multipliers. Recently, RFID application demands a low cost solution and pushes implementing Schottky diodes in standard CMOS process without adding costly procedure steps or layer masks[11−13]. As is known, the operating principle of the voltage multiplier is a nonlinear process and it is difficult to figure out how to optimize the voltage multiplier for maximum power conversion efficiency. There have been several theoretical analyses to solve this problem which can be divided into two methods. One is to directly simulate the voltage multiplier in the time domain[14,15]. This method usually takes too much time to reveal the true nature of the voltage multiplier. The other is to find a model which can explain the relationship between the design parameters and conversion efficiency[2,6,7,9,10,16,17]. Previous studies give various models for the multiplier using Schottky diodes or p-n junction diodes, but they are either too complex to be used for analysis[2] or too simple to reflect the nature of nonlinear effects of voltage multiplier[16,17]. Thus, depending on application requirements, a tradeoff must be made to choose a model with enough precision but less complexity.

In this paper, a simple mathematical model for voltage multiplier using Schottky diodes is derived to reveal the complicated relationships of important design parameters of voltage multiplier, such as input alternating RF voltage, output DC voltage, load DC current and number of multiplier stages. A simple linear approximation for Schottky diode is introduced to simplify the proposed model. To validate the model, two voltage multipliers, with two stages and four stages respectively, are designed and fabricated in EEPROM compatible 0.35 μm CMOS process. The relationships predicted by the model show considerable agreement with the measurement results. Furthermore, with the help of the proposed model, optimization of stage number of voltage multiplier to achieve maximum power conversion efficiency is discussed.

The capacitive input impedance of voltage multiplier is

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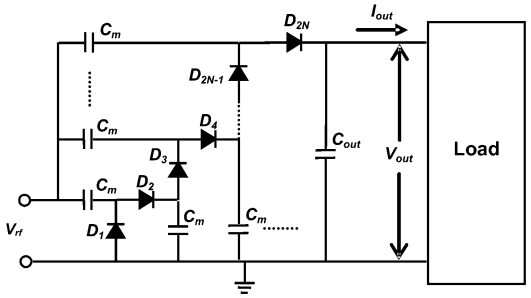

Fig.1. A typical N-stage voltage multiplier.

also predicted for matching the antenna. In practical applications, impedance match should be achieved over an operating bandwidth established to accommodate the electromagnetic compatibility regulations in different world regions. According to the Bode-Fano criterion[18,19], which is used to analyze the fundamental limitations on impedance matching, the limitation on maximum power up range for passive UHF RFID power extraction circuits is studied.

2. Modeling and analysis of voltage multiplier

In this section, a mathematical model is derived to show the nonlinear performance of voltage multiplier. With the help of the proposed model, optimization of number of stages to achieve maximum RF-to-DC conversion efficiency is discussed. The model also gives the input capacitive impedance which will be used for further study in the following sections.

2.1. Derivation of voltage multiplier model

A typical N-stage voltage multiplier is depicted in Fig.1. In order to increase high frequency performance and decrease power loss in the voltage multiplier, Schottky diodes are used. Let us suppose that a sinusoidal voltage with frequency f_0 and amplitude $V_{\rm rf}$ is applied at the input of voltage multiplier. The output DC voltage and output DC current are $V_{\rm out}$ and $I_{\rm out}$ respectively. The capacitors $C_{\rm m}$ in the multiplier have to be dimensioned large enough to be capable of driving the load current without considering the influence of the parasitic capacitance in Schottky diodes. A reservoir capacitor $C_{\rm out}$ is placed at the output of the multiplier to minimize the ripple of output dc voltage and store the supplied energy. As a consequence, it is possible to consider capacitors $C_{\rm m}$ and $C_{\rm out}$ as short-circuits in the ac analysis and as open circuits in the dc analysis. In the dc analysis, the $2N$ identical diodes are connected in series, their DC bias is

$$V_{\rm bias} = -\frac{V_{\rm out}}{2N}. \tag{1}$$

In the DC analysis, all diodes appear to lie in parallel and the incident sinusoidal voltage $V_{\rm rf}$ is directly applied to every diode. Therefore, the total voltage $V_{\rm d}$ that drops across each diode is given by

$$V_{\rm d} = -\frac{V_{\rm out}}{2N} + V_{\rm rf}\cos\left(2\pi f_0 t + n\pi\right), \tag{2}$$

where the variable n is the subscript of diodes in Fig.1.

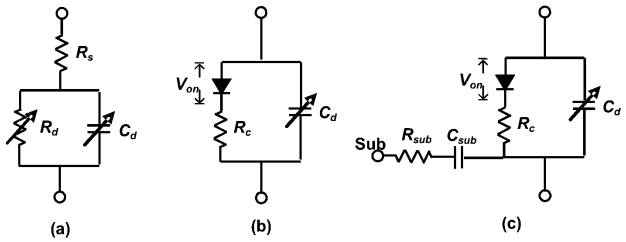

Fig.2. Equivalent circuit of Schottky diodes: (a) Typical circuit; (b) Simplified equivalent circuit; (c) Simplified equivalent circuit with substrate losses.

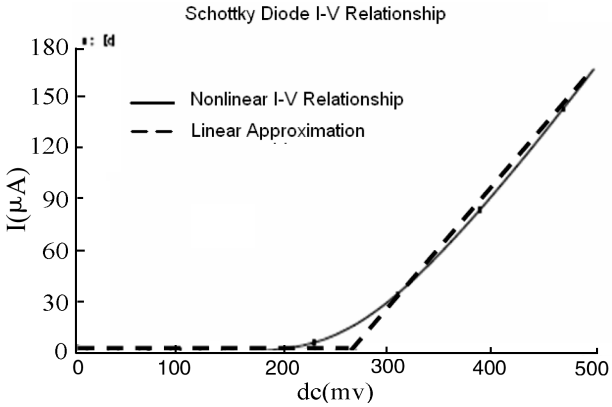

Fig.3. Nonlinear *I-V* relationship of Schottky diodes and linear approximation.

The equivalent circuit of a typical Schottky diode is shown in Fig.2(a). The diode consists of a series resistor $R_{\rm s}$, a nonlinear resistor $R_{\rm d}$ described by the I–V relationship of a diode at DC, and a nonlinear junction capacitance $C_{\rm d}$. Since the DC power required by passive RFID transponder is very low, the small DC output current of voltage multiplier makes the effect of the series resistance $R_{\rm s}$ negligible.

The current versus voltage relationship for a Schottky diode can be given by[20]

$$I_{\rm d} = I_{\rm sT}\left[\exp\left(\frac{V_{\rm d}}{V_{\rm t}}\right) - 1\right], \tag{3}$$

where $I_{\rm sT}$ is the reverse-saturation current and $V_{\rm t}$ is the thermal voltage. Substituting Eq. (2) into Eq. (3), the current $I_{\rm d}$ in each diode can be directly given as

$$I_{\rm d} = I_{\rm sT}\left[\exp\left(\frac{V_{\rm rf}}{V_{\rm t}}\cos(2\pi f_0 t + n\pi)\right)\exp\left(-\frac{V_{\rm out}}{2NV_{\rm t}}\right) - 1\right]. \tag{4}$$

In addition, the current across junction capacitance $C_{\rm d}$ is periodical and no energy is consumed, so it is not considered in Eq.(4). The exponential of a cosinusoidal function in Eq.(4) can be expressed using the modified Bessel functions series expansion[2]. However, the complexity of Bessel function makes the study of voltage multiplier more difficult. This problem is mainly caused by the nonlinear property of the diode resistor $R_{\rm d}$ which shows an exponential I–V relationship, shown in Fig.3.

In order to simplify the analysis of voltage multiplier, we have the following assumptions:

(1) Current across each diode $I_{\rm d} \approx 0$ when $V_{\rm d} < V_{\rm on}$, where $V_{\rm on}$ is a fixed forward voltage drop when the Schottky diode is on.

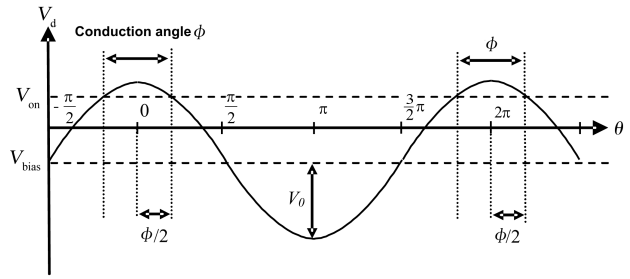

Fig.4. Schottky diodes bias versus angle.

(2) We assume that the change of forward-bias voltage is limited in a small range when Schottky diode is on and hence the nonlinear diode resistor R_d can be approximately considered to have a constant resistance when forward-bias voltage is larger than V_{on}.

The first assumption is based on the fact that the current across the diode is very small when forward voltage is less than a certain value which is about 0.3 V for Schottky diodes. The second assumption is reasonable considering that low power consumption of passive RFID transponder requires very small DC output current of voltage multiplier, leading to narrow conduction angle ϕ of Schottky diodes and hence small variation of forward-bias voltage when diode is on. Under these assumptions, the nonlinear resistor R_d with exponential I–V relationship can be simplified to an ideal diode in series with a linear resistor R_c, as shown in Fig.2 (b). The ideal diode is assumed to have a constant forward voltage drop V_{on} and a zero resistance when the diode is on, and have an infinite resistance when the diode is off. Consequently, the I–V relationship of the simplified model for Schottky diodes is depicted in Fig.3, and can be expressed as

$$I_d = \begin{cases} \dfrac{V_d - V_{on}}{R_c}, & V_d \geqslant V_{on} \\ 0, & V_d < V_{on} \end{cases} \tag{5}$$

Comparing with the complex nonlinear current law in Eq.(4), a reasonable approximation is utilized to achieve a linear current law in Eq.(5). With the simple linear current law, the complexity of voltage multiplier study can be reduced greatly.

From Eqs.(2) and (5), we can find that each diode in the multiplier is driven as a class C amplifier[6], shown in Fig.4, with a conduction angle ϕ given by

$$\phi = 2\arccos x \quad \text{with} \quad x = \frac{V_{on} - V_{bias}}{V_{rf}}. \tag{6}$$

With the simple linear law in Eq.(5), current in one period of incident sinusoidal voltage can be expressed with conduction angle[21]:

$$I_d(\theta) = I_{d\max}\left[\frac{\cos\theta - \cos\dfrac{\phi}{2}}{1 - \cos\dfrac{\phi}{2}}\right], \quad -\frac{\phi}{2} < \theta < \frac{\phi}{2}. \tag{7}$$

The multiplier DC output current I_{out} is the fundamental component of the diode current, and can be calculated by

$$I_{out} = \frac{1}{2\pi}\int_{-\frac{\phi}{2}}^{\frac{\phi}{2}} I_d(\theta)\mathrm{d}\theta. \tag{8}$$

Solving Eq.(8) with Eqs.(5)–(7), an analytical expression for I_{out} is given by

$$I_{out} = \frac{1}{\pi R_c}\left[\sqrt{1-x^2} - x\arccos x\right] \tag{9}$$

with $x = \dfrac{V_{on} - V_{bias}}{V_{rf}}$ and $V_{bias} = -\dfrac{V_{out}}{2N}$.

Since the input of multiplier is a sinusoidal voltage without DC component, it is possible calculate the input power of multiplier through ac analysis. In AC analysis, the capacitor C_m and C_{out} can be considered as short-circuit and the incident sinusoidal voltage is directly applied to each diode. So the average input power P_{in} is $2N$ times of the power dissipated in one diode and can be calculated by

$$P_{in} = 2N\frac{1}{2\pi}\int_{-\frac{\phi}{2}}^{\frac{\phi}{2}} V_{rf}(\theta)I_d(\theta)\mathrm{d}\theta. \tag{10}$$

Solving Eq.(10) with Eqs.(5)– (7), we get

$$P_{in} = \frac{NV_{rf}^2}{\pi R_c}\left[\arccos\, x - x\sqrt{1-x^2}\right] \tag{11}$$

with $x = \dfrac{V_{on} - V_{bias}}{V_{rf}}$ and $V_{bias} = -\dfrac{V_{out}}{2N}$.

The substrate losses in diodes are neglected in the above equation. In order to take substrate losses into consideration, we use the equivalent circuit of Schottky diode with substrate shown in Fig.2 (c), where R_{sub} and C_{sub} are the substrate parasitic resistance and capacitance, respectively. In the AC analysis, with the equivalent circuit of diodes, we can find that the voltage drop across the substrate parasitic resistor and capacitor in the diodes with even subscript is zero and no power is dissipated. Substrate losses only occur in the diodes with odd subscript and are given by

$$P_{sub} \approx \frac{1}{2}V_{rf}^2 R_{sub}(2\pi f_0 C_{sub})^2. \tag{12}$$

The approximation in the above equation is valid based on the assumption that $2\pi f_0 R_{sub} C_{sub} \ll 1$[4]. Thus, the total incident power of voltage multiplier is obtained by

$$P_{in} = \frac{NV_{rf}^2}{\pi R_c}\left[\arccos x - x\sqrt{1-x^2}\right] + NP_{sub} \tag{13}$$

with $x = \dfrac{V_{on} - V_{bias}}{V_{rf}}$ and $V_{bias} = -\dfrac{V_{out}}{2N}$.

Equation (9) can be solved by numerical iteration to get the value of V_{rf}, the amplitude of incident sinusoidal voltage, with fixed I_{out} and V_{out}. With the solution of V_{rf}, the average input power can be calculated using Eq.(13). Thus, the nonlinear operating principle is fully revealed by Eqs.(9) and (13).

2.2. Input capacitive impedance

A parallel of resistance and capacitance constitute the input equivalent impedance of voltage multiplier, as shown in Fig.5.

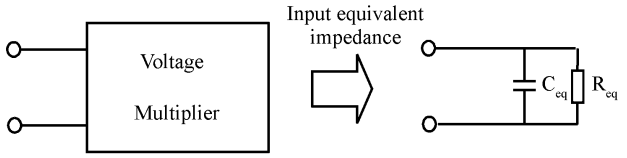

Fig.5. Input equivalent impedance of voltage multiplier.

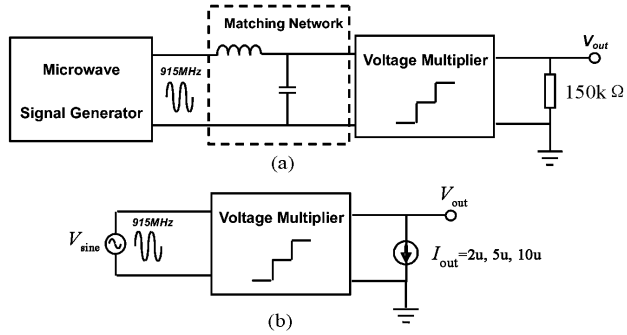

Fig.6. (a) Circuits schematic used for measurement; (b) Model validation used for analysis.

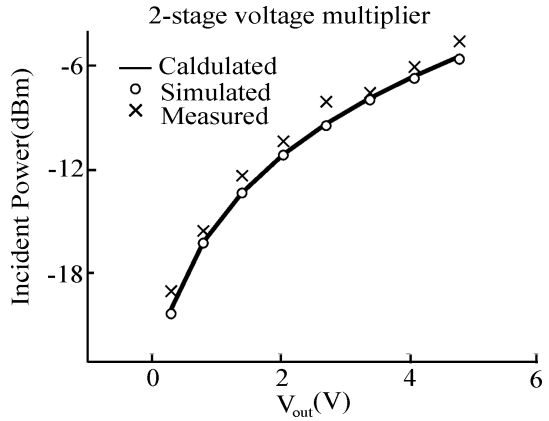

Fig.7. Required incident power versus the output voltage for a 2-stage voltage multiplier.

The input capacitance of voltage multiplier, considering the effects of ESD and pads, is given by

$$C_{eq} = 2N\bar{C}_d + C_{ESD} + C_{pad} \approx C_{ESD} + C_{pad}, \qquad (14)$$

where $\bar{C}_d$ is the average value of nonlinear diode capacitance C_d. The capacitance caused by diodes is around a few tens of feratofarads, which is insignificant compared with the ESD and pads capacitance which is around 400 fF. With this consideration, C_{eq} can be approximately given by C_{ESD}+C_{pad}.

The equivalent resistance of voltage multiplier is defined from power consumption, as follows:

$$R_{eq} = \frac{V_{rf}^2}{2P_{in}}. \qquad (15)$$

2.3. Validation of voltage multiplier model

In order to validate the derived model, two voltage multipliers, with two stages and four stages respectively, are designed and fabricated in EEPROM compatible 0.35 μm CMOS process. Circuit schematic used for measurement is shown in Fig.6 (a). The DC load resistance is 150 kΩ. As shown in

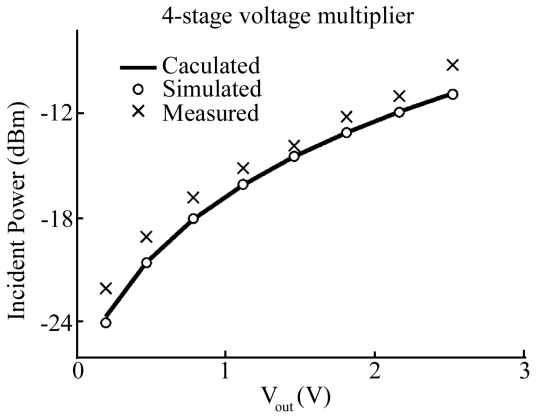

Fig.8. Required incident power versus the output voltage for a 4-stage voltage multiplier.

Table 1. Schottky diodes parameters for calculation.

V_{on} (V)	R_c(Ω)	C_{sub} (fF)	R_{sub} (kΩ)
0.28	320	11.5	5

Figs.7 and 8, calculation results for average input power of voltage multiplier using Eqs.(9) and (13) are compared with measurement results. Furthermore, simulations were done with Spectre simulator in transient simulation and the results are also compared. Schottky diode parameters used for calculation based on the EEPROM compatible 0.35 μm CMOS process are summarized in Table 1.

As shown in Figs.7 and 8, model based calculations and simulations are in excellent agreement. Measurements show considerable agreement with calculations and require a littler larger incident power than calculation results. The difference is considered to be caused by additional parasitic substrate capacitances which generate much more losses, as can be seen from Eq.(12). Nevertheless, unavoidable impedance mismatch between the matching network and rectifier, resulting in some of the incident power being reflected back, is also the possible reason for this difference. Although small difference exists between measurements and calculations, both the assumptions and the derived model are validated. The proposed model is accurate enough to be used for estimating the performance of the voltage multiplier. This is important because it can be used to predict the nonlinear operating principle of the N-stage voltage multiplier and achieve the nonlinear circuit optimization which usually takes a very long time. In the following section, with the help of the proposed model, optimization of stage number of voltage multiplier to achieve the maximum power conversion efficiency is discussed.

3. Stage number optimization of voltage multiplier

As shown in the proposed model in Eqs.(9) and (13), stage number N is a very important design parameter for voltage multiplier. Optimization on stage number to achieve maximum power conversion efficiency will be discussed in this section.

Power conversion efficiency η of the voltage multiplier is defined as the ratio of P_{out}, the DC power delivered to the load,

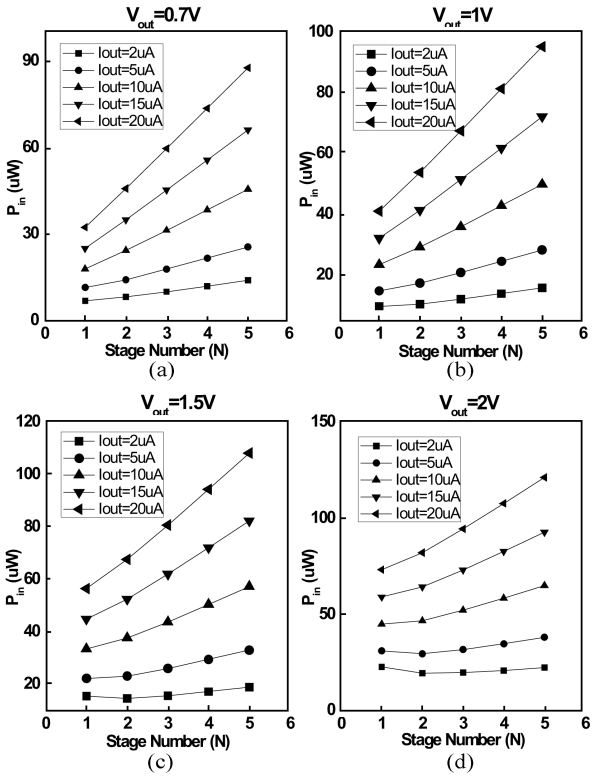

Fig.9. Required incident power for different DC load current $I_{\rm out}$ at a load voltage of (a) $V_{\rm out}$ = 0.7 V, (b) $V_{\rm out}$ = 1 V, (c) $V_{\rm out}$ = 1.5 V, and (d) $V_{\rm out}$ = 2 V.

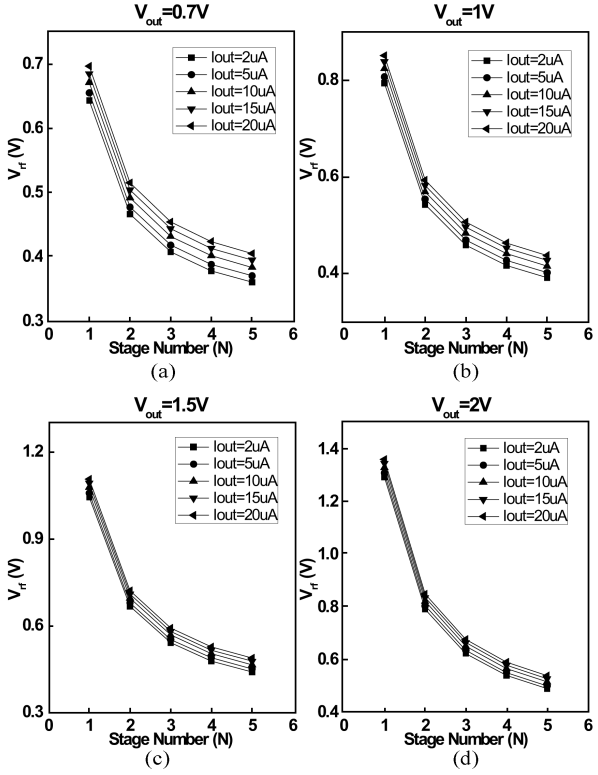

Fig.10. Amplitude of incident alternating voltage $V_{\rm rf}$ when (a) $V_{\rm out}$ = 0.7 V, (b) $V_{\rm out}$ = 1 V, (c) $V_{\rm out}$ = 1.5 V, and (d) $V_{\rm out}$ = 2 V.

to $P_{\rm in}$, the total incident alternating power. Thus,

$$\eta = \frac{P_{\rm out}}{P_{\rm in}}. \tag{16}$$

From the definition of voltage multiplier efficiency, for a fixed DC load power $P_{\rm out}$, the less the incident power is required, the higher the efficiency will be.

Since, from Eqs.(9) and (13), if the required DC loads voltage $V_{\rm out}$ and current $I_{\rm out}$ are specified, the minimum amplitude of incident alternating voltage and power, which allows the rectifier to supply a load current $I_{\rm out}$ at voltage $V_{\rm out}$, can be calculated. Thus, we define rectifier functions, as follows:

$$P_{\rm in}(N) = G(V_{\rm out}, I_{\rm out}), \tag{17}$$

$$V_{\rm rf}(N) = F(V_{\rm out}, I_{\rm out}), \tag{18}$$

where $P_{\rm in}$ and $V_{\rm rf}$ are both a function of N, the number of stages for the voltage multiplier.

We plot $P_{\rm in}(N)$ for different values of $I_{\rm out}$ and $V_{\rm out}$ in Fig.9. For a fixed stage number N and $V_{\rm out}$, $P_{\rm in}$ curves shift upward as $I_{\rm out}$ increases. This is because of the increased voltage drop across the finite output resistance of voltage multiplier. The corresponding amplitude curves of incident alternating voltage are also plotted in Fig.10.

As shown in Figs.9 (a) and 9 (b), when $V_{\rm out}$ is 0.7 or 1 V, $P_{\rm in}$ increases monotonically with stage number N when $I_{\rm out}$ is fixed. Thus, as the stage number increases, the power conversion efficiency severely decreases when input voltage amplitudes are low. The number of stages corresponding to the minimum input power is N = 1. From Figs.9 (c) and 9 (d), when $V_{\rm out}$ is 1.5 or 2 V, for large load current 10, 15, and 20 μA, $P_{\rm in}$ also increases monotonically with stage number N. However, it is possible to note that, when load current is small, the stage number corresponding to the minimum input power is shifted to higher value N = 2. The reason for this is the change of the substrate losses as functions of DC load current $I_{\rm out}$, voltage $V_{\rm out}$ and stage number N, which will be discussed in the following parts of this section.

As shown in Fig.10, for a fixed DC load voltage, less number of stages requires larger amplitude of incident alternating voltage $V_{\rm rf}$ at the input terminal of the voltage multiplier, which would result in larger substrate losses as can be seen from Eq.(12). However, the total substrate losses for an N-stage voltage multiplier are the N times of the $P_{\rm sub}$ as defined in Eq.(12). Thus, there are two important parameters, the $V_{\rm rf}$ and the stage number N, determining total substrate losses and it is possible to find the optimum stage number N to minimize the total substrate losses. We plot total substrate losses $NP_{\rm sub}$, as shown in Fig.11, corresponding to different cases plotted in Figs.9 and 10. As depicted in Figs.10 (a) and 11 (a), when the output DC load voltage is 0.7 V, the required incident $V_{\rm rf}$ is very small and the total substrate losses increase monolithically with the stage number N. Stage number is the dominant factor for the total substrate losses. Contrarily, as the $V_{\rm rf}$ increases, the stage number corresponding to the minimum total substrate losses is shifted to the higher value, for Fig.11 (b) is N = 2 and for Figs.11 (c) and 11 (d) is N = 3.

However, as shown in Figs.9 and 11, the stage number

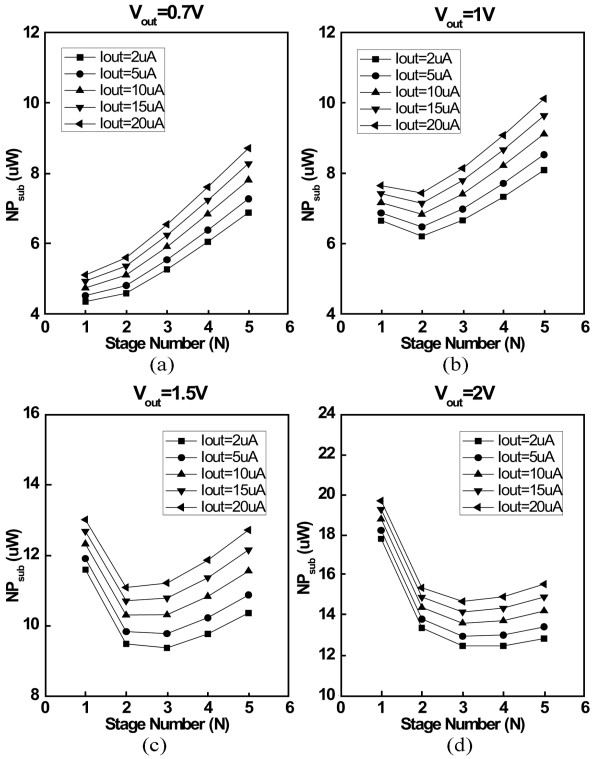

Fig.11. Total substrate losses for different DC load current $I_{\rm out}$ at a load voltage of (a) $V_{\rm out}$ = 0.7 V, (b) $V_{\rm out}$ = 1 V, (c) $V_{\rm out}$ = 1.5 V, and (d) $V_{\rm out}$ = 2 V.

corresponding to the minimum total substrate losses does not totally correspond to the minimum incident power. This is because of the power losses for a voltage multiplier including not only the substrate losses, but also the power losses across the output resistance of a voltage multiplier which would increase as the stage number increases for a fixed DC load current and load voltage.

Thus, as the stage number increases, the optimization will exist only when the decrease in substrate losses larger than the increase in power losses in the output resistance of voltage multiplier. Especially in case of large DC load voltage and small DC load current, when the total substrate losses are comparable to the power losses in the output resistance of voltage multiplier, it is possible to find the optimum number of stages to minimize the incident power, and hence maximize the power conversion efficiency η.

Thus, taking our design for example, as shown in Figs. 9 (a) and 9 (b), when $V_{\rm out} \leqslant 1$ V, the optimum stage number corresponding to maximum efficiency is $N = 1$. In case of $V_{\rm out}$ larger than 1V, when $I_{\rm out} \leqslant 5$ μA, the optimum stage number is $N = 2$, while $N = 1$ is also preferable when $I_{\rm out}$ is larger 5 μA. Furthermore, the substrate losses presented in the proposed model might be smaller than real condition. For increasing substrate losses as defined in Eq.(12), it is possible to find the optimum number of stages in even higher values. Although the examples plotted in Fig.9 are mainly based on the EEPROM compatible 0.35 μm CMOS process, the course of discussion and the proposed model can be applied to any other process.

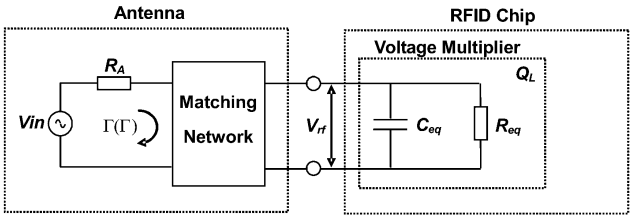

Fig.12. Antenna with matching network has to be matched to the RFID chip to achieve maximum power transfer.

4. Limitation on maximum power up range

The basic components of a UHF power extraction system are an antenna, a voltage multiplier and an impedance matching network. For the application of passive UHF RFID, adding an external matching network with lumped elements is usually prohibitive due to cost and fabrication issues. To overcome this situation, antenna is designed to be directly matched to the RFID chip[22,23], as shown in Fig.12. The equivalent input capacitive impedance $C_{\rm eq}$ and $R_{\rm eq}$ can be found from Eqs.(14) and (15).

In practical applications, impedance match should be achieved over an operating bandwidth established to accommodate the electromagnetic compatibility regulations in different world regions. Furthermore, resonant frequency of RFID tags often shifts considerably in the field because of their local environment (presence of conductive or dielectric materials, temperature variations and so on). A certain fraction of tags are thus never read. Tags should be designed to have intrinsically large bandwidths to minimize this problem.

In simple terms, perfect impedance matching (zero reflection coefficient) can only be achieved over a zero bandwidth, i.e., at a finite number of frequencies. Matching over a bandwidth usually means that the reflection coefficient looking to the load is less than some specified value over a range of frequencies $\Delta\omega$. The maximum impedance matching bandwidth of the network is governed by a criterion known as the Bode-Fano criterion, which will be described below.

4.1. Bode-Fano limit

Considering the single match case shown in Fig.12, this is the case originally analyzed by Bode[18]. The purely resistive source impedance $R_{\rm A}$ is to be matched to complex load with quality factor $Q_{\rm L}$ using a lossless matching network (using only inductors and capacitors). The load is considered to be a parallel R–C combination, with $Q_{\rm L}$= $\omega R_{\rm eq} C_{\rm eq}$. According to Bode–Fano criterion, the fundamental limitation on impedance matching takes the form[19]

$$\int_0^{\infty} \ln \frac{1}{|\Gamma(\omega)|} {\rm d}\omega \leqslant \frac{\pi}{R_{\rm eq} C_{\rm eq}}, \tag{19}$$

where $\Gamma(\omega)$ is defined as the reflection coefficient looking from the source. Since $0< \Gamma(\omega) <1$, we can divide Eq.(19) by –1, take the absolute value of both sides, and get

$$\left| \int_0^{\infty} \ln |\Gamma(\omega)| {\rm d}\omega \right| \leqslant \frac{\pi \omega_0}{Q_{\rm L0}}, \tag{20}$$

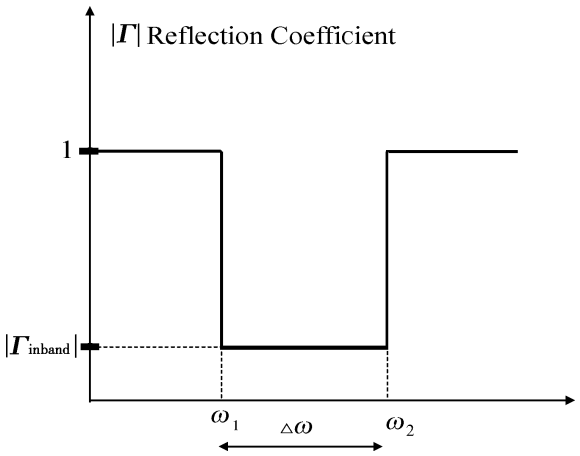

Fig.13. Reflection coefficient for maximum bandwidth.

where ω_0 is the center frequency of the matching bandwidth of interest, and $Q_{L0}=\omega_0 C_{eq} R_{eq}$.

Referring to Eq.(19), it can be observed that the maximum value of integral is limited by the load R_{eq} and C_{eq} [24]. Equation (20) expresses a fundamental gain-bandwidth-like constraint[25,26]. For a fixed load, a 'high gain' matching network, which usually means low Γ, can only be realized over a narrow bandwidth. Since the minimum area under the $\ln \Gamma(\omega)$ curve is fixed by Eq.(20), for a given load, the way to get a maximum bandwidth, as shown in Fig.13, is to have $|\Gamma| = 1$ along the entire band except for the band of interest ($\Delta\omega$) in which keeping $|\Gamma|$ constant ($|\Gamma| = |\Gamma_{inband}|$). This corresponds to the case of ideal matching networks. In this case, we get

$$\int_0^{\infty} \ln|\Gamma(\omega)|\mathrm{d}\omega = \Delta\omega \ln(|\Gamma_{inband}|). \tag{21}$$

Substitute Eq.(21) into Eq.(20), a theoretical upper bound on the achievable impedance match bandwidth is given by

$$\Delta\omega \leqslant \frac{\pi\omega_0}{Q_{L0}} \frac{1}{\ln\frac{1}{|\Gamma_{inband}|}}. \tag{22}$$

The equality in Eq.(22) holds when the impedance matching network is ideal as shown in Fig.13. From Eq.(22), we can find that there will be compromise between the matching bandwidth $\Delta\omega$ and the maximum power transfer to the load. If matching is to be performed to satisfy a certain $|\Gamma_{inband}|$, the bandwidth may have to be reduced. On the other hand, if matching is to be performed over a certain given bandwidth, the amount of power transfer to the load may have to be compromised. As stated above, in common passive UHF RFID applications, a certain bandwidth is usually required to accommodate the electromagnetic compatibility regulations in different world regions.

4.2. Upper bound of power up range

We now consider the power extraction systems of far-field UHF RFID application. The power available at the input of the tag antenna is given by

$$P_{AV} = G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 P_t, \tag{23}$$

where P_t is the power transmitted from reader, G_t and G_r are the gains of transmitting and receiving antenna, respectively, r is the distance between the reader and UHF RFID tag, and λ is the electromagnetic wavelength in the medium.

As shown in Fig.12, R_{eq} is the real part of input impedance of voltage multiplier and consumes power delivered by the antenna. The power dissipated at R_{eq} is P_{in}, the total incident power of voltage multiplier as expressed by Eqs.(13) and (17). The maximum possible value of P_{in} is P_{AV}, which corresponds to antenna impedance matched to the load. In general $P_{in} = (1-|\Gamma|^2)P_A$, where $|\Gamma|$ is the magnitude of the reflection coefficient as depicted in Fig.12. Thus, from Eq.(23), we get

$$P_{in} = \left(1 - |\Gamma|^2\right) G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 P_t. \tag{24}$$

Equation (22) can be written as

$$|\Gamma_{inband}|^2 \geqslant \exp\left(-\frac{2\pi\omega_0}{\Delta\omega Q_{L0}}\right). \tag{25}$$

Substituting Eq.(25) into Eq.(24), the relationship between Q_{L0}, bandwidth $\Delta\omega$ and operating distance r is given by

$$P_{in} \leqslant \left[1 - \exp\left(-\frac{2\pi\omega_0}{\Delta\omega Q_{L0}}\right)\right] G_t G_r \left(\frac{\lambda}{4\pi r}\right)^2 P_t. \tag{26}$$

In order to analyze the distance r, Equation (26) can be written as

$$r \leqslant \sqrt{G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \frac{P_t}{P_{in}} \left[1 - \exp\left(-\frac{2\pi\omega_0}{\Delta\omega Q_{L0}}\right)\right]} \tag{27}$$

From the proposed mathematical model in Eqs.(9) and (13), the P_{in} and V_{rf} are fixed for a given the DC load current I_{out} and V_{out}. Load quality Q_{L0} is expressed by $Q_{L0}=\omega_0 C_{eq} R_{eq}$. Thus, using the definition in Eqs.(17) and (18), Equation (27) is written as

$$r \leqslant \sqrt{G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \frac{P_t}{G(I_{out}, V_{out})} \left[1 - \exp\left(-\frac{2\pi}{\Delta\omega C_{eq} R_{eq}}\right)\right]} \tag{28}$$

From Eq.(15), we can find that the equivalent input impedance R_{eq} of voltage multiplier is fixed if P_{in} and V_{rf} are fixed. Thus, using Eqs.(15), (17) and (18) to express R_{eq}, we get

$$r \leqslant \sqrt{G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \frac{P_t}{G(I_{out}, V_{out})} \left[1 - \exp\left(-\frac{2\pi G(I_{out}, V_{out})}{\Delta\omega C_{eq} F^2(I_{out}, V_{out})}\right)\right]} \tag{29}$$

Equation (29) predicts the theoretical power up range for passive UHF RFID power extraction circuits for a given DC load current I_{out} and voltage V_{out}. Thus, the maximum power up range r_{max} is given by

$$r_{max} = \sqrt{G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \frac{P_t}{G(I_{out}, V_{out})} \left[1 - \exp\left(-\frac{2\pi G(I_{out}, V_{out})}{\Delta\omega C_{eq} F^2(I_{out}, V_{out})}\right)\right]}. \tag{30}$$

It can be observed that, if the transmitted power P_t, antenna transmitting antenna gain G_t and receiving gain G_r are given, the power up range is strongly determined by the impedance matching bandwidth $\Delta\omega$ and the input capacitance C_{eq} of voltage multiplier which is defined in Eq.(14). In order

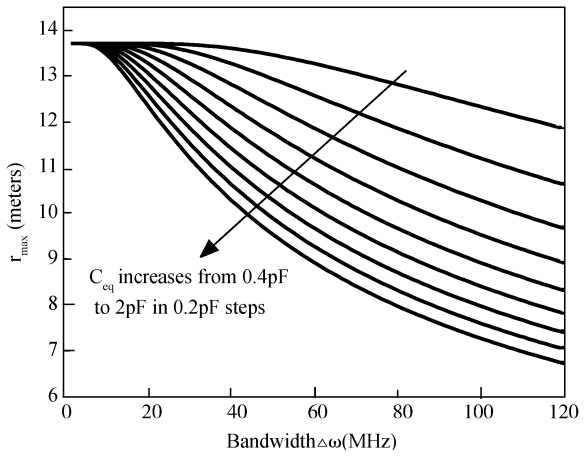

Fig.14. Theoritical maximum power up range for parameters C_{eq} varying from 0.4 to 2 pF in 0.2 pF steps.

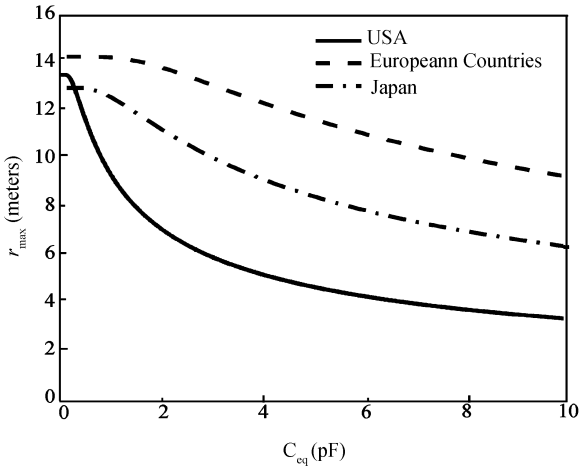

Fig.15. Theoritical maximum power up range for some allocated RFID bandwidth.

to achieve a long power up range, a narrow matching bandwidth and small input capacitance of voltage multiplier are required. From Eqs.(17) and (18), the function of G(I_{out}, V_{out}) and F(I_{out}, V_{out}) are stage number N dependent. To achieve a maximum power up range, as analyzed in section III, stage number N should also be optimized to achieve maximum power conversion efficiency according to a given minimum DC load current and voltage.

It is noticeable that, as $\Delta\omega c_{eq}$ decreases to zero, an upper bound limit for maximum power up range exists as follows:

$$r_{max}|_{\Delta\omega C_{eq}\to 0} = \sqrt{G_t G_r \left(\frac{\lambda}{4\pi}\right)^2 \frac{P_t}{G(I_{out}, V_{out})}}. \qquad (31)$$

However, Equation (31) only applies for impedance match at a certain frequency point (zero bandwidth) or zero input capacitance, neither of them is applicable for practical applications of passive UHF RFID. This is because of that, in practical applications, impedance match should be achieved over an operating bandwidth, and the input capacitance of voltage multiplier cannot be minimized to zero due to the influence of parasitic capacitance of ESD and package.

4.3. Power up range for practical UHF RFID applications

For the analysis of theoretical maximum range in practical applications, we set typical values for UHF RFID power extraction system. We have ω_0 = 900 MHz, G_r = 1.5 dBi, G_t = 4.5 dBi and P_t = 1 W, and suppose that one needs V_{out} to be at least 1.5 V at I_{out} = 2 μA for powering up the on chip circuitry. As discussed in Section 3, we set the stage number N = 2 for voltage multiplier to achieve maximum power conversion efficiency. Using the previously derived equation (30) and the proposed model, we plot the theoretical maximum power up range r_{max} as a function of bandwidth $\Delta\omega$ with C_{eq} varies from 0.4 to 2 pF in 0.2 pF steps.

As shown in Fig.14, r_{max} is a decreasing function of both $\Delta\omega$ and C_{eq}. Thus, to achieve long power up range, the power extraction circuits need to have narrow matching bandwidth $\Delta\omega$ and low input capacitance C_{eq}. It is noticeable that, when the bandwidth decreases to a value of about less than 10 MHz, all of the plotted r_{max} saturate to one maximum value given by Eq.(31), and that further decreases bandwidth barely improve the performance. In addition, as shown in Fig.14, narrow impedance match bandwidth reduces the influence of the C_{eq} variation.

The RFID bandwidths for European countries, United States of America and Japan are shown in Table 2. Using these three bandwidths, calculations of maximum power up range are also performed. For the three different bandwidth cases, we set ω_0 to be 866.5, 915 and 953 MHz, respectively. Furthermore, resonant frequency of RFID tags often shifts considerably in the field because of their local environment, such as the presence of conductive or dielectric materials, temperature variations and so on. To overcome this problem, some error margin is required. We set the matching bandwidths $\Delta\omega$ four times of the required bandwidths corresponding to these three cases, and they are 12, 104 and 24 MHz, respectively. The rest parameters for the power extraction systems, including G_r, G_t, P_t, I_{out} and V_{out}, are set the same as previously stated. For three allocated cases listed in Table 2, the maximum power up range r_{max} as a function of C_{eq} is plotted in Fig.15.

From Fig.15, we derive the same lessons as from Fig.14 that the maximum power up range decreases monotonically as the C_{eq} increases. The r_{max} in case of USA decrease more rapidly than another two cases. This is because of the largest impedance matching bandwidth required in case of USA. It is thus the same conclusion we get from Eq.(22) that matching over a bandwidth requires power transfer to the load to be compromised, and hence the power up range. As the decreasing of the input capacitance C_{eq}, the r_{max} in three cases saturate to three different maximum values given by Eq.(31). The difference is caused by different center frequency ω_0 of matching bandwidth and the final saturated value is inversely proportional to the center frequency ω_0. For the three given cases, the only way to enlarge the maximum power up range is to reduce the input capacitance C_{eq}, as the r_{mas} is a decreasing function of C_{eq}. As defined in Eq.(14), C_{eq} can be approximately given by C_{ESD}+C_{PAD} which are around 400 fF. Thus, when C_{eq}= 400 fF, as plotted in Fig.15, the maximum power up range approaches to the saturated value for the cases of

Table 2. Maximum power up rang for the three allocated cases.

Place	European countries	USA	Japan
DC load	I_{out} = 2μA; V_{out} = 1.5 V		
Environment	G_r = 1.5 dBi, G_t = 4.5 dBi and P_t = 1 W		
Frequency (MHz)	865–868	902–928	950–956
Bandwidth (MHz)	3	26	6
Center frequency ω_0 (MHz)	866.5	915	953
Matching bandwidth $\Delta\omega$ (MHz)	12	104	24
Power up range (m)	14.282	12.065	12.979

European Countries and Japan. In case of USA, an even lower input capacitance is required to maximize the maximum power up range, which is usually limited by the large size of ESD and package whose parasitic capacitance could hardly be reduced. We take C_{eq}= 400 fF for our analysis and the maximum power up range for the three allocated cases are summarized in Table 2.

4.4. Further consideration

The theoretical maximum power up range predicted in this section is the upper bound limits for the power up range based on the Bode-Fano criterion. In fact, the limits can be reached only with infinite-order matching networks. So we can only approach it as closely as possible using finite matching networks by increasing complexity.

In practical application of antenna design for UHF RFID, a simple L-section impedance matching network, which is a simple first order matching network, can be utilized to achieve a maximum efficiency[27]. It requires no additional elements and occupies no extra area. However, the impedance matching bandwidth of first order matching network is much shorter than Bode-Fano limit. It is clear that second-order matching networks provide a substantial increase in bandwidth[28] and the bandwidth will increase further for higher order networks. However, it rarely pays to use filter order higher than third, since the bandwidth increase from adding another order decreases rapidly with the increasing order of matching networks. Thus, second-order matching networks shall be the best choice for antenna design. It increases bandwidth by factors of 2 to 3 over first order networks and can get quite close to the Bode-Fano limit without adding much circuit complexity. Detailed analysis of antenna design for UHF RFID applications can be found in Refs.[22, 23, 25, 29], which is not in the scope of this paper and will not be discussed.

5. Conclusion

In this paper, modeling and analysis of far field power extraction circuits for passive UHF RFID applications are presented. A linear approximation for Schottky diode is used to reduce the complexity of modeling voltage multiplier. Thus, a simple mathematical model for voltage multiplier using Schottky diodes is derived to reveal the complicated relationships of important design parameters of voltage multiplier, such as input alternating RF voltage, output DC voltage, load DC current and number of multiplier stages. To validate the model, two voltage multipliers, with two stages and four stages respectively, are designed and fabricated in EEPROM compatible 0.35 μm CMOS process. The relationships predicted by the model show considerable agreement with the measurement results. Furthermore, with the help of the proposed model, optimization of stage number of voltage multiplier to achieve maximum power conversion efficiency is discussed. The capacitive input impedance of voltage multiplier is also predicted for matching the antenna. In practical applications, impedance match should be achieved over an operating bandwidth established to accommodate the electromagnetic compatibility regulations in different world regions. According to the Bode-Fano criterion, a limitation on maximum power up range for passive UHF RFID power extraction circuits is studied. Low input capacitance C_{eq} of voltage multiplier is required to maximize the power up range, which is strongly limited by the large parasitic capacitance due to ESD and package. A compromise also exists between the matching bandwidth $\Delta\omega$ and the maximum power up range r_{max}. Thus, if matching is to be performed over a certain given bandwidth, the power up range has to be compromised.

Although the analysis and examples described in this paper are mainly based on the EEPROM compatible 0.35 μm CMOS process, the course of discussion and proposed model can be applied to any other process.

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