A novel on-chip high to low voltage power conversion circuit*

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Abstract: A novel power supply transform technique for high voltage IC based on the TSMC 0.6 μm BCD process is achieved. An adjustable bandgap voltage reference is presented which is different from the traditional power supply transform technique. It can be used as an internal power supply for high voltage IC by using the push-pull output stage to enhance its load capability. High-order temperature compensated circuit is designed to ensure the precision of the reference. Only 0.01 mm^2 area is occupied using this novel power supply technique. Compared with traditional technique, 50% of the area is saved, 40% quiescent power loss is decreased, and the temperature coefficient of the reference is only 4.48 ppm/°C. Compared with the traditional LDO (low dropout) regulator, this power conversion architecture does not need external output capacitance and decreases the chip-pin and external components, so the PCB area and design cost are also decreased. The testing results show that this circuit works well.

Key words: power management; bandgap reference; high-order temperature compensation; push-pull output
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1. Introduction

In the designs such as DC–DC, AC–DC and class D amplifiers, considering the cost and power consumption, the low voltage is always used as the power supply on chip. So the inter-chip voltage conversion circuit is necessary. The on-chip power conversion solution affects the performance of the chip directly. Therefore the output voltage with high PSRR, good linear regulation and load regulation is required. Though the traditional on-chip power conversion solution can satisfy the requirement mentioned above, its large occupied area and high power consumption limit the chip packaging and application. As to these problems, a bandgap reference is directly used for power supply. The power conversion has less power consumption and map area, need not have external output capacitance, and decreases the chip-pin as well as external components, which is economical and practical.

2. Analysis of feasibility for the proposed design

2.1. Traditional high to low voltage conversion solution

The traditional high to low voltage conversion solution in high voltage IC is shown in Fig. 1. The TTL_BUFFER is generally used to generate roughly low voltage[1], which is used as the power supply of the voltage reference block. The reference voltage can be generated and used as the reference for the whole LDO block. LDO block finishes the high to low voltage conversion and uses this low voltage as the on-chip power supply. The traditional design solution adopts LDO with power transistor of DMOS to finish the high to low voltage conversion. In general, the area of DMOS is larger than normal MOS[2, 3]. Furthermore, traditional power supply transform technique needs no less than three circuit blocks. Thus the traditional design not only increases the cost, but also cannot satisfy the requirement of portable electronic product.

2.2. Principle of the proposed design

In Fig. 2, the circuit in the dashed line is the bandgap reference circuit[4], and QP1, QP2 and R_1 are the core circuit. R_{X1}–R_{X4} are the bias resistances. We use the bandgap structure to realize the power supply transform, decreasing the chip area and static power consumption.

Suppose $R_{X1} = R_{X3}$, $R_{X2} = R_{X4}$, the amplifier AMP has the equal input voltage, i.e, $V_A = V_B$, and neglect the base current, then we get:

$$I_{11} = \frac{V_C - V_A}{R_{X1}} = \frac{V_{EB\_QP1}}{R_{X1}} = \frac{V_C - V_B}{R_{X3}} = I_{21}. \quad (1)$$

$$I_{12} = \frac{V_A}{R_{X2}} = \frac{V_B}{R_{X4}} = I_{22}. \quad (2)$$

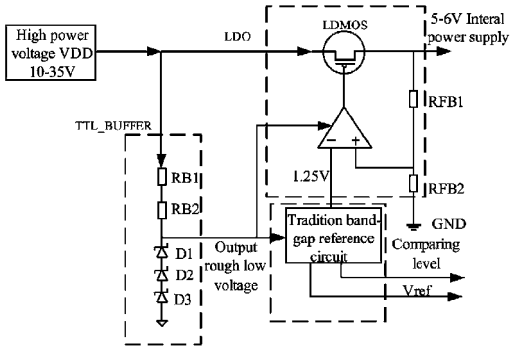

Fig. 1. Traditional power supply transform technique for high voltage IC.

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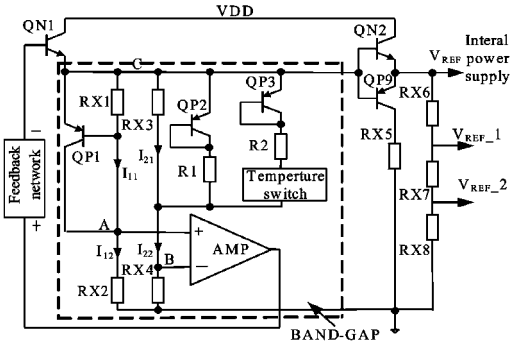

Fig. 2. Equivalent circuit of the proposed power supply transform technique.

From Fig. 2, the voltage across R_1 can be known as

$$V_{R17} = V_{EB\_QP1} - V_{EB\_QP2} = \Delta V_{EB}. \tag{3}$$

The current flow R_1 can be known as

$$I_{R5} = \frac{\Delta V_{EB}}{R_1}. \tag{4}$$

From Eqs. (1) and (4), I_{12} and I_{22} can be calculated as

$$\begin{aligned} I_{12} = I_{22} &= \frac{V_C - V_B}{R_{X3}} + \frac{\Delta V_{EB}}{R_1} = \frac{V_C - V_A}{R_{X1}} + \frac{\Delta V_{EB}}{R_1} \\ &= \frac{V_{EB\_QP1}}{R_{X1}} + \frac{\Delta V_{EB}}{R_1}. \end{aligned} \tag{5}$$

From Eq. (2) the voltage of A and B can be calculated as

$$V_A = V_B = R_{X2}\left(\frac{V_{EB\_QP1}}{R_{X1}} + \frac{\Delta V_{EB}}{R_1}\right) = R_{X4}\left(\frac{V_{EB\_QP1}}{R_{X3}} + \frac{\Delta V_{EB}}{R_1}\right). \tag{6}$$

The reference voltage can be induced as

$$V_{REF} = V_A + V_{EB\_QP1} - V_{EB\_QN2}. \tag{7}$$

As $V_{EB\_QP1} \approx V_{EB\_QN2}$ and $I_{C\_QP1} = I_{C\_QP2}$, so,

$$\begin{aligned} V_{REF} = V_A = V_B &= R_{X2}\left(\frac{V_{EB\_QP1}}{R_{X1}} + \frac{\Delta V_{EB}}{R_1}\right) \\ &= \frac{R_{X2}}{R_{X1}}\left(V_{EB\_QP1} + \frac{R_{X1}}{R_1}\Delta V_{EB}\right) \\ &= \frac{R_{X2}}{R_{X1}}\left(V_{EB\_QP1} + \frac{R_{X1}}{R_1} V_T \ln N\right), \end{aligned} \tag{8}$$

where N is the emitter area ratio of QP2 to QP1.

From Eq. (8), it can be concluded that the typical zero temperature coefficient voltage can be gotten by selecting the right ratio of R_{X1} to R_1. By adjusting the ratio of R_{X2} to R_{X1} we can get the regulated on-chip power supply V_{RES}[5]. V_{REF_1} and V_{REF_2} acting as the divided voltage of V_{REF}[6], can be used as low voltage reference and compared level. Moreover they are related only to the ratio of divided resistances, and the same good precision can be acquired as V_{REF}.

2.3. Low frequency PSRR of the proposed design

PSRR is one of the most important electrical characteristics, so high PSRR of low frequency[7] should be guaranteed. The following is the PSRR of low frequency for proposed power conversion solution.

According to Fig. 2, suppose that the equivalent resistance of CE of QN1 is r_{CE}, the equivalent impedance of node C is about $1/g_{mQN1}$, then we can get:

$$\begin{aligned} \mathrm{PSRR}_{DC} &= \frac{\dfrac{1}{g_{mQN1}\left[1 + A_{open}(\beta_N - \beta_P)\right]}}{\dfrac{1}{g_{mQN1}\left[1 + A_{open}(\beta_N - \beta_P)\right]} + r_{CE}} \\ &= \frac{1}{1 + g_{mQN1}\left[1 + A_{open}(\beta_N - \beta_P)\right] r_{CE}} \\ &\approx \frac{1}{g_{mNQ1} A_{open}(\beta_N - \beta_P) r_{CE}}. \end{aligned} \tag{9}$$

A_{open} is the open-loop gain of the circuit which is composed of AMP, feedback network, QN1, QP1, R_{X2}, QP2, R_{X4} and R_1. β_P and β_N are the coefficients of the positive feedback loop and negative feedback loop respectively, which can be expressed as

$$\beta_P \approx \frac{R_{X2}}{R_{X2} + \dfrac{1}{g_{mQP1}}}, \tag{10}$$

$$\beta_N \approx \frac{R_{X4}}{R_{X4} + R_1 + \dfrac{1}{g_{mQP2}}}. \tag{11}$$

$\beta_N > \beta_P$ is guaranteed by design, so the proposed power conversion can reach high PSRR when it works in lower frequency[8].

From the above analysis, it can be seen that the proposed power conversion solution is to design high voltage bandgap reference in essence. Therefore, the solution has high output voltage accuracy and zero temperature coefficient. QN2 acts as the output of reference, and it can not only realize the temperature compensation, but also can enlarge the load capability and insulate the high power.

3. Circuit design

Figure 3 is the practical schematic of on-chip power conversion solution, which is the actual circuit of high-voltage bandgap reference. The circuit is composed of four parts: (I) start circuit of high power voltage reference circuit, (II) core of the bandgap of high power voltage reference circuit, (Ⅲ) high-order temperature compensation network designed for high precision requirement, and (Ⅳ) the push-pull output stage for promoting the load capability.

The following is a detailed theoretical analysis for the proposed power supply transform circuit.

In Fig. 3, part I is the self bias current resource, and MD1, MD2 and QN1 can realize the functions of the start circuit and help the reference circuit break away from zero current state[4]. When power is on and high level EN makes MD3 on, the reference circuit will start[1].

From part II in Fig. 3, it can be known that the bandgap core circuit is composed of QP1, QP2, R_1, R_{X1}–R_{X4}. The differential operational amplifier consists of QP3, QP4, M5, M6, R_{X0}, M1, M2 and MD2. QN1 acts as emitter follower which constructs a negative feedback loop circuit cooperating with

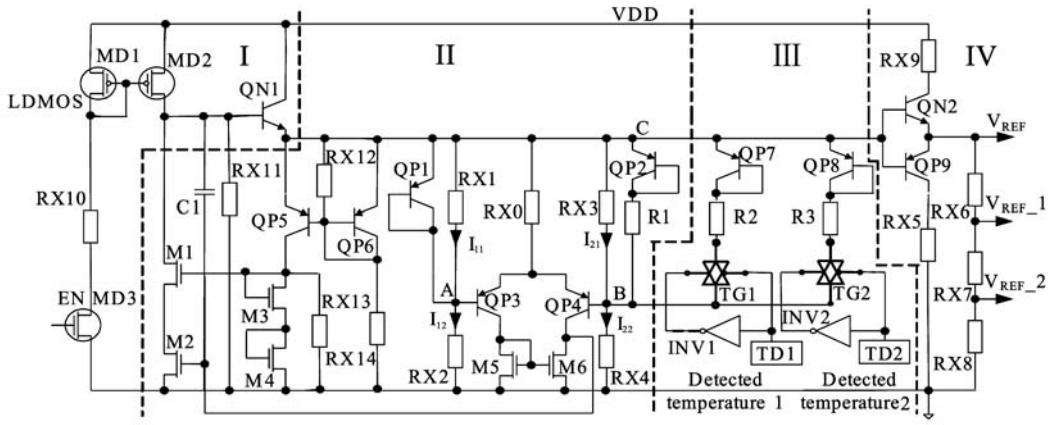

Fig. 3. Practical schematic of on-chip power conversion.

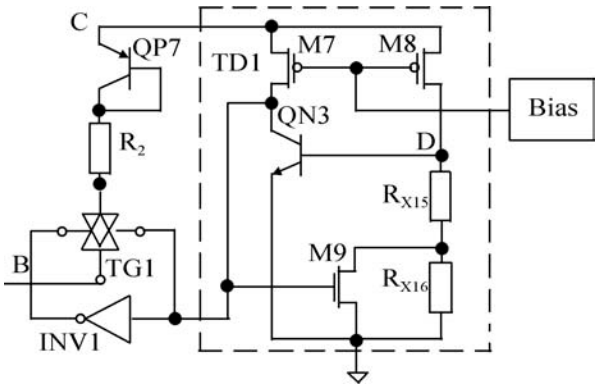

Fig. 4. Temperature detection circuit.

the differential amplifier. The DC bias circuit, which is composed of QP5, QP6, M3, M4, R_{X13} and R_{X14}, is used to supply bias to M1. So M1 has been in saturated region which makes the gain of amplifier more stable. C_1 is the Miller compensation capacitance[6]. In addition, the power of amplifier adopts the reference voltage directly, which can decrease the noise from power supply. So the stability of feedback loop can be increased[5].

Circuit part II can guarantee the precision of the reference by using amplifier and negative feedback. In order to further improve the precision of output, the high-order temperature compensation network[9] is presented. It shows in part III of Fig. 3 that, one-order compensation cell is composed of QP7, R_2, TG1, INV1 and TD1. A detailed schematic of the cell is shown in Fig. 4.

The temperature detection circuit uses I_{PTAT} current to detect the temperature in Fig. 4. When the temperature is T_0, TG1 is on. Suppose that the on-threshold of QN3 is V_{BEON1} at temperature T0, V_{BEON2} at temperature $T_0 - \Delta T$, the temperature hysteresis is ΔT, and voltage of D point is V_D, so,

$$\Delta T = \Delta V \left/ \frac{\partial V_{BE}}{\partial T}, \right. \tag{12}$$

$$\begin{aligned} \Delta V &= V_{BEON2} - V_{BEON1} = V_D(T_0) - V_D(T_0 - \Delta T) \\ &= I_{M8\_D}(R_{X15} + R_{X16}) - I_{M8\_D}R_{X15} \\ &= I_{M8\_D}R_{X16} = \frac{\partial V_{BE}}{\partial T}\Delta T. \end{aligned} \tag{13}$$

From the above deduction, we know that the temperature hysteresis ΔT can be adjusted by R_{X16}, the temperature point T_0 by R_{X15}. High-order temperature compensation[9, 10] can be added in reference through the circuit consisting QP7, R_2 and TD1.

In the proposed power supply transform solution, a third-order temperature compensation is shown in Fig. 3. We divide the temperature range into three parts: [−40 °C, T_1], [T_1, T_2] and [T_2, 125 °C]. The relation between current I_{22} and reference voltage V_{REF} in different temperature ranges is shown as

$$I_{22} = \begin{cases} \dfrac{V_C - V_B}{R_{X3}} + \dfrac{V_C - V_B - V_{EB\_QP2}}{R_1}, & -40\,^\circ\mathrm{C} \leqslant T \leqslant T_1, \\ \dfrac{V_C - V_B}{R_{X3}} + \dfrac{V_C - V_B - V_{EB\_QP2}}{R_1} + \dfrac{V_C - V_B - V_{EB\_QP2}}{R_2}, & T_1 \leqslant T \leqslant T_2, \\ \dfrac{V_C - V_B}{R_{X3}} + \dfrac{V_C - V_B - V_{EB\_QP2}}{R_1} + \dfrac{V_C - V_B - V_{EB\_QP2}}{R_2} + \dfrac{V_C - V_B - V_{EB\_QP2}}{R_3}, & T_2 \leqslant T \leqslant 125\,^\circ\mathrm{C}. \end{cases} \tag{14}$$

As $V_A = V_B$, $V_C - V_B = V_{EB\_QP1}$, $R_{X1} = R_{X3}$, $V_{EB\_QP1} \approx V_{BE\_QN2}$, so

$$V_{REF} = V_A + V_{EB\_QP1} - V_{BE\_QN2} = V_B + V_{EB\_QP1} - V_{BE\_QN2}$$

$$= I_{22}R_{X4} = \begin{cases} \left[\dfrac{V_{EB\_QP1}}{R_{X1}} + \dfrac{\Delta V_{BE}}{R_1}\right]R_{X4}, & -40\,^\circ\mathrm{C} \leqslant T \leqslant T_1, \\ \left[\dfrac{V_{EB\_QP1}}{R_{X1}} + \Delta V_{BE}\left(\dfrac{1}{R_1} + \dfrac{1}{R_2}\right)\right]R_{X4}, & T_1 \leqslant T \leqslant T_2, \\ \left[\dfrac{V_{EB\_QP1}}{R_{X1}} + \Delta V_{BE}\left(\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_3}\right)\right]R_{X4}, & T_2 \leqslant T \leqslant 125\,^\circ\mathrm{C}. \end{cases} \tag{15}$$

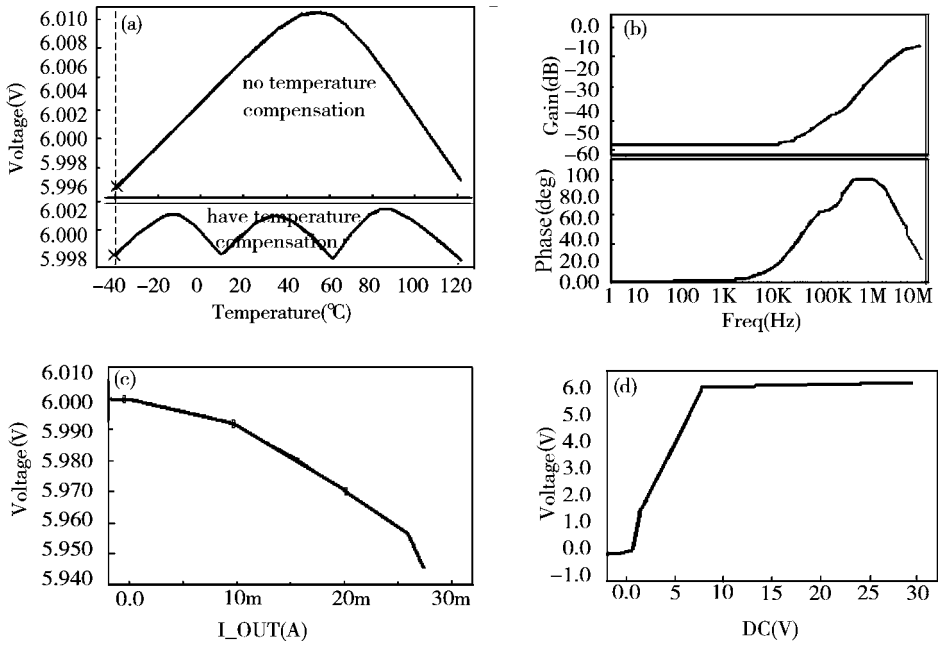

Fig. 5. Simulation waveforms for electronic characteristics: (a) V_{REF} without compensation versus V_{REF} with three-order compensation; (b) PSRR versus frequency of the proposed reference; (c) Output voltage varies with load current; (d) Simulated waveform for output varies with power voltage.

If higher precision is required, we can use n-order temperature compensation. So, V_{REF} with n-order temperature compensation range can be shown as

$$V_{REF} = I_{22}R_{X4} = \begin{cases} \left[\dfrac{V_{EB\_QP1}}{R_{X1}} + \dfrac{\Delta V_{BE}}{R_1}\right]R_{X4}, & -40\,^{\circ}\mathrm{C} \leqslant T \leqslant T_1, \\ \left[\dfrac{V_{EB\_QP1}}{R_{X1}} + \Delta V_{BE}\left(\dfrac{1}{R_1} + \dfrac{1}{R_2}\right)\right]R_{X4}, & T_1 \leqslant T \leqslant T_2, \\ \cdots\cdots \\ \left[\dfrac{V_{EB\_QP1}}{R_{X1}} + \Delta V_{BE}\sum\limits_{i=1}^{n}\dfrac{1}{R_i}\right]R_{X4}, & T_{n-1} \leqslant T \leqslant 125\,^{\circ}\mathrm{C}. \end{cases} \tag{16}$$

In the circuit of part Ⅳ in Fig. 3, the output is designed as transistor push-pull output stage. Then the reference circuit can not only supply powerful load capability, but also lower output resistance. R_{X9} is the current limit resistor which prevents the damage of QN2 caused by too large current. Compared with traditional LDO structure, no external capacitor is required in the structure of high voltage converting to low voltage, which decreases the chip-pin, external components, the cost of the system and the PCB area.

Based on the TSMC 0.6 μm BCD process, the proposed circuit was simulated using H-spice. The simulation results are shown in Fig. 5. Figure 5(a) is the comparison of V_{REF} with no compensation and three-order compensation. V_{REF} varies 13.9 mV at –40 to 125 °C without compensation while 4.3 mV with three-order compensation. The temperature coefficient decreases from 13.3 to 4.48 ppm/°C[11]. Figure 5(b) shows the PSRR versus frequency. The PSRR is 55 dB when the frequency is 10 kHz. This shows that the output voltage of the circuit design has a good PSRR. Figure 5(c) shows that V_{REF} varies with load current. The maximum output current can reach to 25 mA. The load regulation is 0.78%. Figure 5(d) is the V_{REF} versus power supply V_{DD}. The line regulation is 0.05%/V.

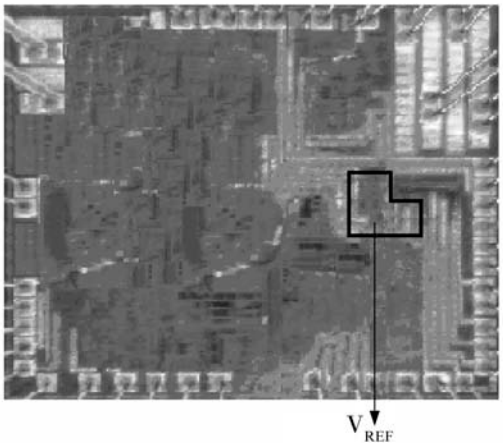

Fig. 6. Microphotograph of the chip with the proposed reference.

4. Microphotograph of the chip and testing results

Figure 6 is the microphotograph of class-D audio power amplifier with the proposed reference. The detailed location is shown in black box, whose area is 0.01 mm^2, and 50% less than the power supply structure of chip in Ref. [12].

Figures 7 and 8 show the testing results of the proposed circuit. When the testing condition in Fig. 7 is V_{DD} = 20 V, I_{load} = 15 mA, the testing result is V_{REF} = 5.98 V. In Fig. 8, When V_{DD} = 15 V, V_{REF} = 6 V, and the load current skipping from 10 to 20 mA, the testing results are: Ch4 is the ripple of V_{REF} and Ch1 is the load current. The result shows that the output voltage pulse is less than 10 mV and there is no ringing. The quiescent current is 16 μA, which is 40% lower than that in the traditional power supply transform technique.

Figure 9 is the simulation and testing results of V_{REF}.

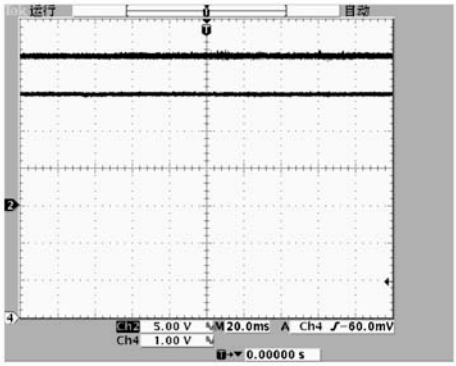

Fig. 7. Testing result of V_{REF} and V_{DD}.

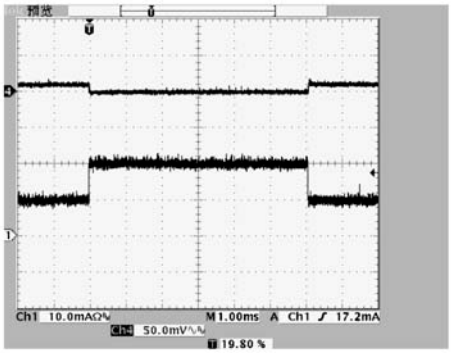

Fig. 8. Experimental result of load response.

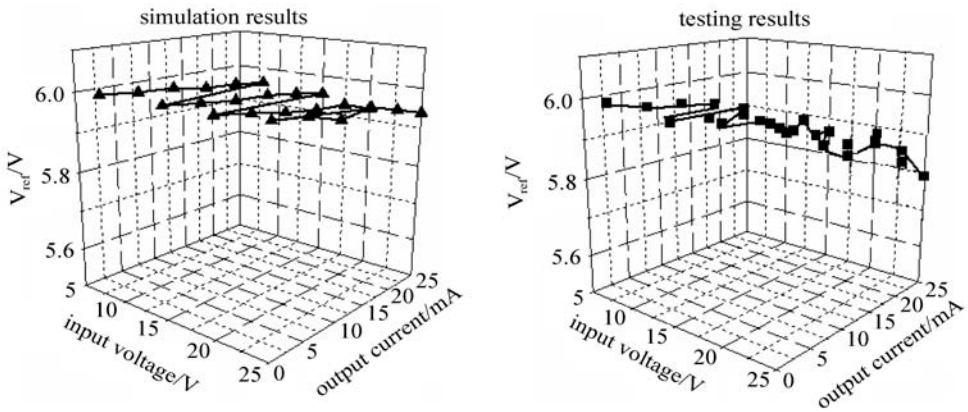

Fig. 9. Simulation and testing results of V_{REF}.

The results prove that the proposed reference circuit works well, the testing load regulation is 0.8%, and the testing line regulation is 0.045%/V.

5. Conclusion

Based on the TSMC 0.6 μm BCD process, a novel on-chip power conversion solution that is to design high voltage reference in essence is realized. Compared with traditional on-chip power conversion solution, the TTL_BUFFER conversion circuit and LDO circuit are canceled, and the proposed circuit not only saves the chip area but also lowers the quiescent current of the whole system. In addition, the proposed solution adds high order temperature compensation, improving the output precision. This power conversion architecture does not need external capacitance and decreases the chip-pin and external components; the PCB area and design cost are also decreased. The testing results show that it works well and can be widely used in similar high voltage IC design.

References

[1] Wang Hui, Wang Songlin, Lai Xinquan, et al. The design and realization of wide input and fast start up high precision voltage reference. Journal of Xidian University (Natural Science), 2008, 35(2): 272 (in Chinese)

[2] Bassin C, Ballan H, Declercq M. High-voltage devices for 0.5 μm standard CMOS technology. IEEE Electron Device Lett, 2000, 21(1): 40

[3] Ludikhuize A W. A versatile 7001200 V IC process for analog and switching applications. IEEE Trans Electron Devices, 1991, 38(7): 1582

[4] Ker M D, Chu C Y, Lo W Y. Low-voltage curvature-compensated bandgap reference. United States Patent, US 6987416 B2. Jan 17, 2006

[5] Meijer G C M, Schmale P C, Van Zalinge K. A new curvature-corrected bandgap reference. IEEE J Solid-State Circuits, 1982, SC-17(6): 1139

[6] Gunawan M, Meijer G C M, Fonderie J, et al. A curvature-corrected low-voltage bandgap reference. IEEE J Solid-State Circuits, 1993, 28(6): 667

[7] Marinca S. Bandgap voltage reference circuit with high power supply rejection ratio (PSRR) and curvature correction. United States Patent, US 6891358 B2. May 10, 2005

[8] Tham K M, Nagaraj K. A low supply voltage high PSRR voltage reference in CMOS process. IEEE J Solid-State Circuits, 1995, 30(5): 586

[9] Wang Hongyi, Lai Xinquan, Li Yushan, et al. A piecewise-linear compensated bandgap reference. Chinese Journal of Semiconductors, 2004, 25(7): 771

[10] Filanovsky I M. Voltage reference using mutual compensation of mobility and threshold voltage temperature effects. ISCAS 2000-IEEE International Symposium on Circuits and Systems, Geneva, Switzerland, 2000: 197

[11] Leung K N, Mok P K T. A sub-1-V 15 ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device. IEEE J Solid-State Circuits, 2002, 37(4): 526

[12] http://focus.ti.com/lit/ds/symlink/tpa3003d2.pdf