A low power 3–5 GHz CMOS UWB receiver front-end*

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Abstract: A novel low power RF receiver front-end for 3–5 GHz UWB is presented. Designed in the 0.13 μm CMOS process, the direct conversion receiver features a wideband balun-coupled noise cancelling transconductance input stage, followed by quadrature passive mixers and transimpedance loading amplifiers. Measurement results show that the receiver achieves an input return loss below −8.5 dB across the 3.1–4.7 GHz frequency range, maximum voltage conversion gain of 27 dB, minimum noise figure of 4 dB, IIP3 of –11.5 dBm, and IIP2 of 33 dBm. Working under 1.2 V supply voltage, the receiver consumes total current of 18 mA including 10 mA by on-chip quadrature LO signal generation and buffer circuits. The chip area with pads is 1.1×1.5 mm^2.

Key words: UWB; direct-conversion receiver; low power; RF CMOS; passive mixer
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1. Introduction

After the US federal communications commission (FCC) agreed in 2002 to open the 7500 MHz of spectrum in the 3.1–10.6 GHz frequency band for unlicensed use of ultra-wideband (UWB), UWB quickly emerged as a promising technology for high speed wireless communication within short distances (10 m). It is targeted to become a general solution for cable replacement, providing seamless connectivity between electronic consumer devices. The use of deep-submicron CMOS technology in UWB implementation is desirable to realize a high level of integration. However, this poses serious design challenges for front-end circuits. Design tradeoffs are required in bandwidth, gain, noise and linearity, with limited power consumption and supply voltage.

The WiMedia UWB adopts a multi-band OFDM approach, dividing this 7500 MHz spectrum bandwidth into 6 band groups and 14 non-overlapping bands spaced at 528 MHz bandwidth each, as shown in Fig. 1. This paper presents an RF receiver front-end for band group 1 (i.e., 3.1–4.7 GHz), which is mandatory for operation. Figure 2 shows the block diagram, which consists of a low noise transconductance stage at the input, followed by quadrature passive mixers for in-phase (I) and quadrature phase (Q) paths. Each mixer is loaded with a transimpedance amplifier (TIA). RF signals are sensed and converted into current signals at the transconductor, commutate through the time-varying switching transistors for down-conversion and flow into the transimpedance load[1]. The TIA synthesizes low impedance at the mixer output, and retains the current mode operation of the input transconductor. The overall voltage conversion gain (CG) can be approximated as

$$\mathrm{CG} = \frac{2}{\pi\sqrt{2}} g_{\mathrm{m}} R_{\mathrm{F}}, \tag{1}$$

where g_{m} is the effective transconductance of input stage, R_{F} is the transresistance of TIA, and a factor of $\sqrt{2}$ in the denominator is introduced to account for sharing the transconductor current between I and Q channels[2]. Besides the RF receiver path, a wideband poly-phase filter (PPF) and LO buffers are integrated to generate quadrature signals from an external LO source. All the signal paths are realized in differential style in order to suppress even order distortion as well as common mode noises.

2. Circuit design

2.1. Capacitor-cross-coupling transconductance stage

The transconductance stage employs a common gate structure utilizing capacitor cross coupling (CCC) technique[3], as shown in Fig. 3. Only one channel of quadrature mixer is shown for simplicity. Common gate input has superior wide-band input matching, linearity and stability over common source input stage. The use of CCC technique doubles effective g_{m} of the input transistors, leading to NF and IP3 improvement as well as power reduction. An off chip balun converts the single-ended signals received from antenna into balanced ones, and directly couples them to the differential input of CCC transconductor, with the center-tapped port providing a DC ground[4]. The input transconductor is loaded with a resonated LC tank that can be tuned to each 528 MHz band of operation, according to the WiMedia PHY standard. Tuning is accomplished through a digitally controlled capacitor array similar to Ref. [5]. Bias current of input transistors are injected from the center-tapped port of an on-chip differential inductor. The bias circuit introduces negligible noise since it contributes only common mode noise.

2.2. Passive mixer with reused padding inductor

Passive mixer is chosen for its low power consumption, while the loading TIA consumes relatively less power since it process low frequency baseband signals. Absence of DC current through switches also effectively eliminate $1/f$ noise[6, 7].

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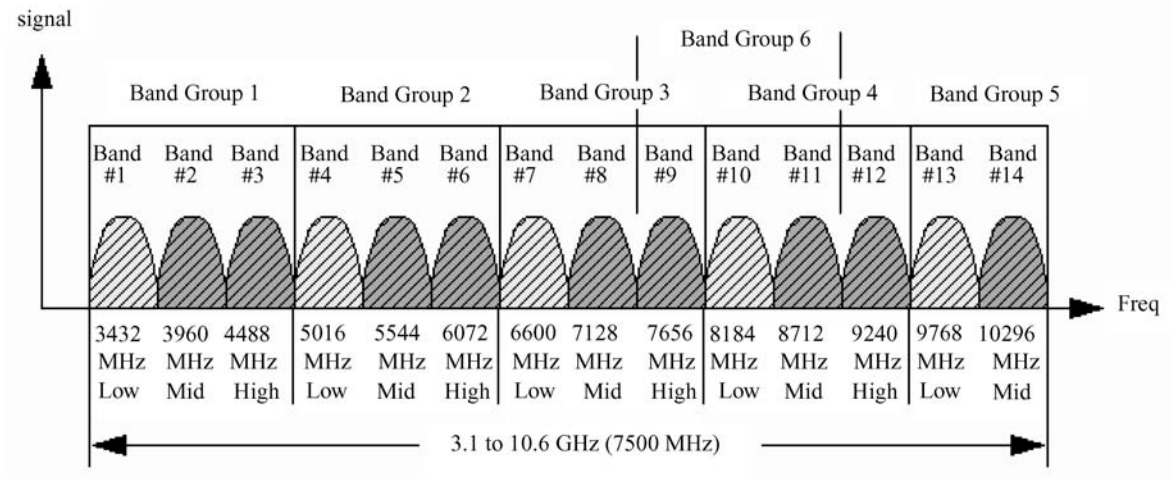

Fig. 1. WiMedia UWB band allocation.

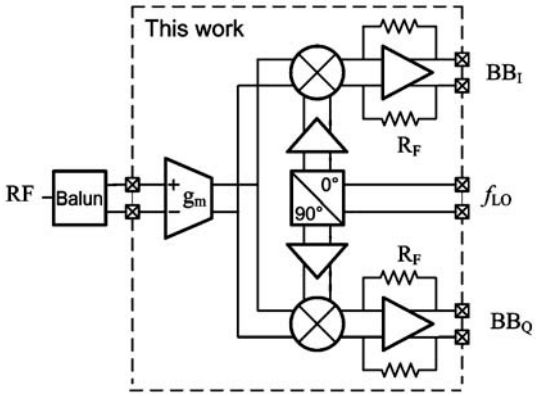

Fig. 2. Architecture of the receiver front-end.

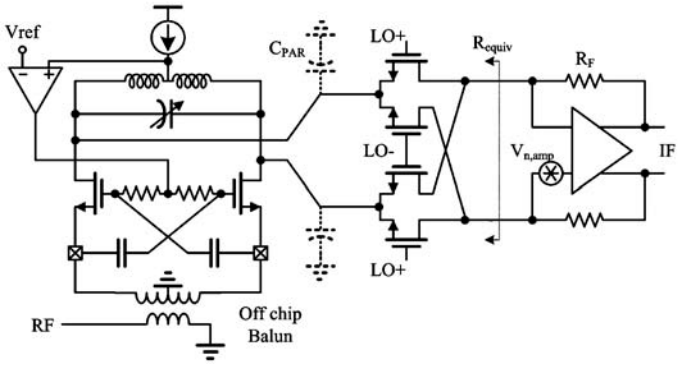

Fig. 3. CCC transconductor followed by passive mixer.

Although it is not a major problem in UWB, immunity to $1/f$ noise makes the proposed receiver an attractive candidate for low-cost multi-standard applications. Thermal noise in passive mixer originates from the conductance g_{ds} of the FET's channel:

$$\overline{i_n^2} = 8kTg_{ds}, \tag{2}$$

which means that larger transistor width can provide lower on-resistance and hence lower noise. However, larger transistor also results in larger parasitic capacitance C_{PAR}, which not only reduces achievable gain, but also couples LO current into the switches, leads to excessive $1/f$ noise[6]. Design tradeoff thus is required for optimum device size of the switch transistors.

For the passive mixer depicted in Fig. 3, C_{PAR} has another negative effect on noise performance. References [6, 8] pointed out that C_{PAR} and switches driven by LO can be considered as a switched capacitor network. Assuming the resonating LC tank is high impedance, the equivalent impedance looking into the mixer as seen by the following amplifier is

$$R_{equiv} = \frac{1}{2f_{LO}C_{PAR}}. \tag{3}$$

As a consequence, the opamp input referred noise $V_{n,amp}$ (including $1/f$ noise) is amplified by a factor of

$$1 + \frac{2R_F}{R_{equiv}} = 1 + 4R_F f_{LO} C_{PAR}. \tag{4}$$

Noise level is thus directly proportional to C_{PAR}, SNR degrades due to the amplification of opamp noise when driven by high frequency LO. In our proposed circuit, the inductor in the LC tank is reused to effectively tune out C_{PAR}, alleviating this problem. Moreover, since C_{PAR} is a nonlinear capacitance which consists of MOSFET C_{db} and C_{gd}, an RF current leakage path exists through C_{PAR}, causing additional harmonic generation. The resonating LC tank blocks the leakage path, so the mixer linearity can be enhanced[9].

Switch transistors should be biased slightly into the OFF overlap mode for optimum noise and IM2 performance[10]. A common mode feedback (CMFB) loop is employed to control the bias voltage of switches by sensing the common mode voltage at the center-tapped port of the differential inductor.

2.3. Variable gain TIA

TIA converts the down-converted current signal into voltage signal through the feedback resistor R_F. As shown in Fig. 4, the proposed TIA consists of two half-circuits of single transistor in shunt-shunt feedback. The value of feedback resistor R_F is a critical design parameter that affects overall receiver performance such as noise, linearity, bandwidth and gain. From small signal analysis in Ref. [11], the transimpedance gain of TIA is given as

$$\frac{V_{IFout}}{I_{IFin}} = -\frac{g_m R_F - 1}{g_m R_D + 1} R_D \approx -R_F, \tag{5}$$

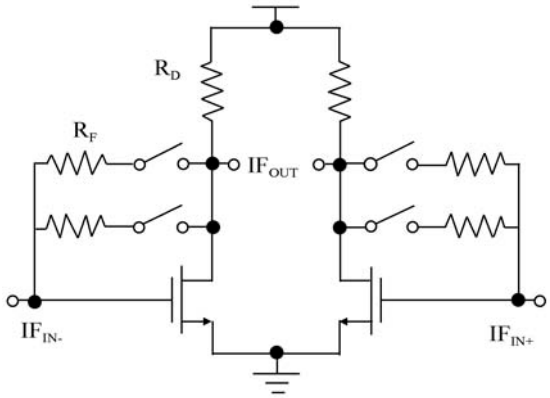

Fig. 4. Variable gain TIA.

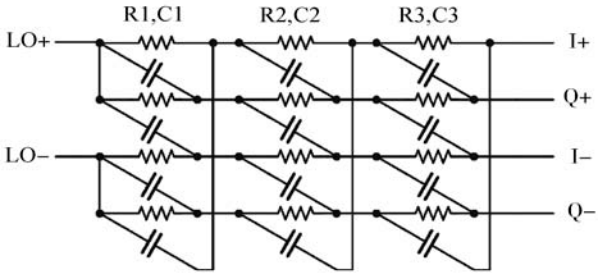

Fig. 5. RC polyphase filter.

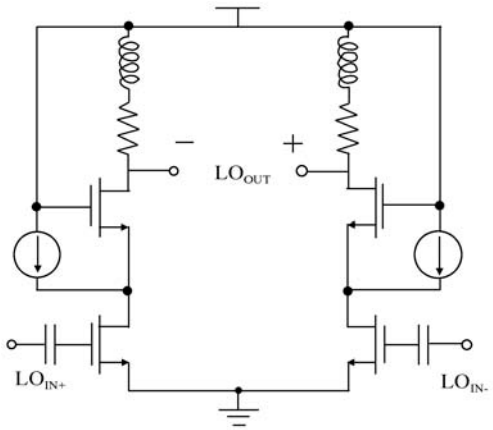

Fig. 6. LO buffer.

and the input referred noise current is

$$\overline{I_{\mathrm{n,in}}^2} = 4kT\left(\frac{\gamma}{g_{\mathrm{m}}R_{\mathrm{F}}^2} + \frac{V_{\mathrm{n,flicker}}^2}{R_{\mathrm{F}}^2} + \frac{1}{g_{\mathrm{m}}^2R_{\mathrm{F}}^2R_{\mathrm{D}}} + \frac{1}{R_{\mathrm{F}}}\right), \quad (6)$$

where γ is the transistor thermal noise factor and $V_{\mathrm{n,flicker}}$ is the input referred flicker noise. It is obvious that a large R_{F} is desirable for high gain and low noise. However, besides the bandwidth limitation, large R_{F} can seriously degrade linearity performance, which is explained as follows. The input resistance (R_{in}) of TIA is

$$R_{\mathrm{in}} = \frac{R_{\mathrm{F}} + R_{\mathrm{D}}}{g_{\mathrm{m}}R_{\mathrm{D}} + 1}. \quad (7)$$

Large R_{F} will increase R_{in}, thus force the passive mixer into the voltage switching mode. As the input signal level grows, the voltage swing starts to modulate the switching instance of the mixer, introducing additional distortion. A digital controlled variable R_{F} is adopted in the proposed design, which allows for optimum gain and noise performance in high gain mode, or optimum linearity in low gain mode.

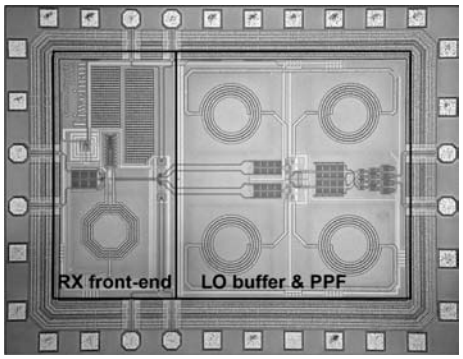

Fig. 7. Die photo.

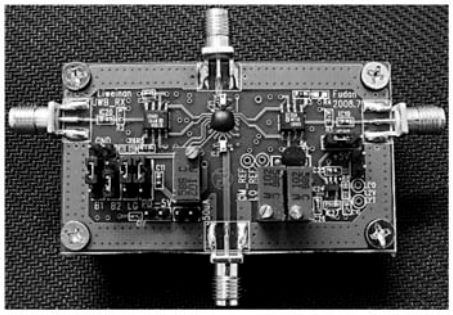

Fig. 8. Test PCB.

2.4. LO I/Q generation and buffer

Quadrature local oscillator (LO) generation is accomplished by a passive poly-phase filter (PPF), as shown in Fig. 5[12]. Unlike traditional I/Q generation by a divide-by-2 circuit, PPF does not require the LO source to run at $2f_{\mathrm{LO}}$ frequency, thus substantially reducing the overall receiver power consumption. In order to cover the 3–5 GHz bandwidth with sufficient margin for process variation, a three-stage cascaded RC PPF is adopted. To limit the loss introduced by passive RC network, the impedance of each successive stage is made larger so that it lightly loads the previous stage, and the impedance of first stage is made to match the 50 Ω external source at the desired frequency.

LO buffer amplifier is necessary to compensate loss due to passive PPF, so that quadrature LO signals are able to drive the mixer with adequate amplitude. A current bleeding pseudo differential amplifier is designed to boost gain and maximize output swing, as shown in Fig. 6. Inductive peaking technique is used at amplifier load for bandwidth extension. Simulation results show that a −1 dB bandwidth of 6 GHz and 15 dB gain can be achieved and the differential output swing approaches 1.5 V_{pp}.

3. Measurement results

The proposed receiver front-end was implemented in the SMIC 0.13 μm 1P8M RF CMOS process, and the total die area including pads is 1.1 × 1.5 mm^2. Figure 7 shows the die microphotograph. The chip is directly bonded onto a 4-layer FR-4 PCB for measurement, as shown in Fig. 8. The receiver

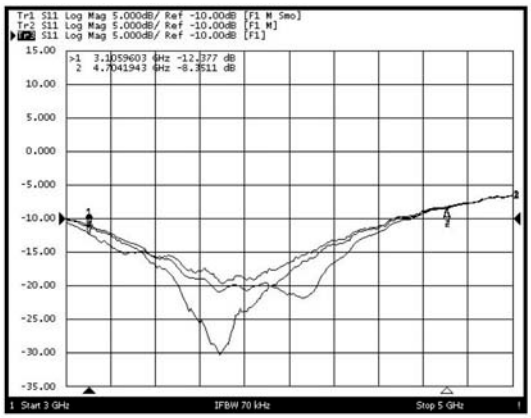

Fig. 9. Measured S_{11}.

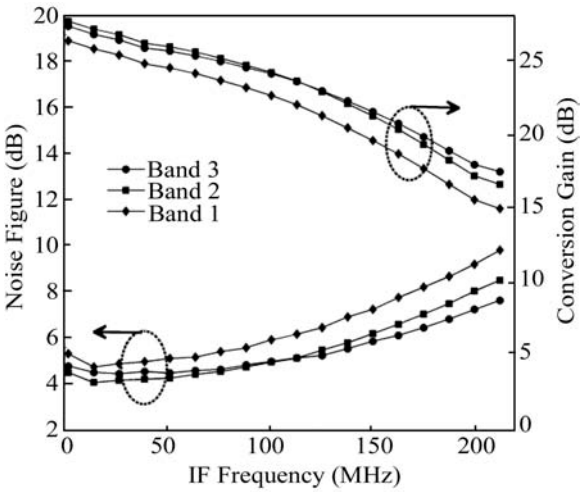

Fig. 10. NF and CG for 3 bands.

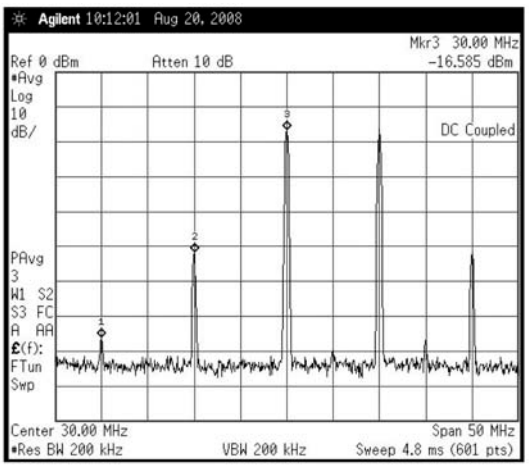

Fig. 11. Output spectrum in IM test.

front-end works under 1.2 V supply voltage and consumes a total current of 18 mA including the 10 mA consumed by LO buffers.

Figure 9 shows the measured S_{11} at the receiver input, when the LC tank is tuned to the 3 bands respectively. S_{11} is below –10 to –8.5 dB across 3.1–4.7 GHz frequency range, and reaches a minimum of –30 dB at 3.9 GHz. Conversion gain (CG) and noise figure (NF) is measured with Agilent noise source 346C and spectrum analyzer PSA E4440A. The measured center frequencies of each band are at 3.32, 3.6, and 4.22 GHz. Maximum conversion gain of 27 dB and minimum

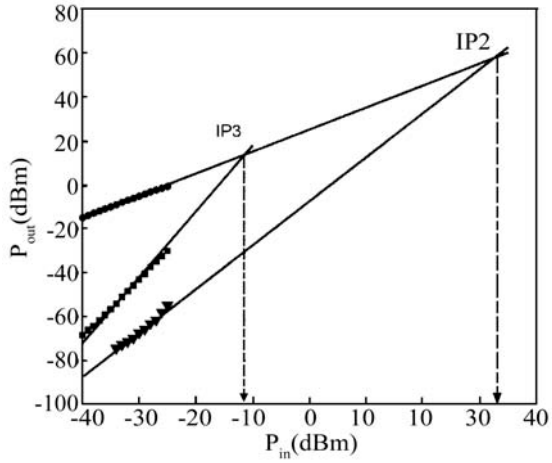

Fig. 12. IP3 & IP2.

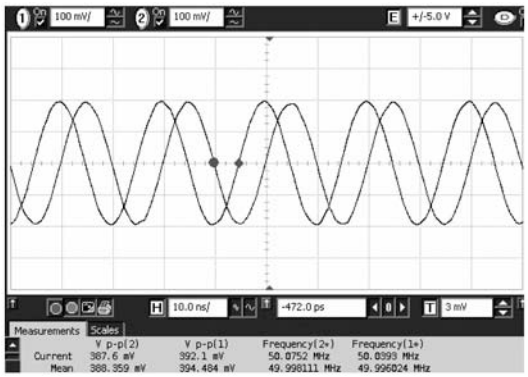

Fig. 13. Transient waveform of I/Q channel output.

noise figure of 4 dB are achieved, as depicted in Fig. 10. The 0.5 dB insertion loss of wideband balun (TDK HHM1583B1) is included in the noise figure, since the front-end circuit relies on this balun to provide signal conversion and DC bias. The measured IF bandwidth is only about 120 MHz, which is reduced by the large input capacitance of the off-chip buffer amplifier (4 pF) on test board. The buffer is used to convert the balanced mixer output into single-ended signal for spectrum analyzer. Noise figure also increases due to this external pole at IF frequencies beyond 120 MHz. It should not be a problem in the implementation of integrated receiver because on-chip VGA follows the mixer exhibits a much smaller loading capacitance.

Linearity test is performed by sweeping the power of 2-tone RF signals at the receiver input, whose frequencies are set to 4.25 and 4.26 GHz, spaced by 10 MHz apart, and LO frequency is set to 4.22 GHz. Figure 11 shows the spectrum components at receiver output, where down-converted fundamental tones are at 30 and 40 MHz, 3rd order IM products are at 20 and 50 MHz, and the 2nd order IM product appears at 10 MHz. Figure 12 shows the measured IIP3 of −11.5 dBm and IIP2 of 33 dBm when the receiver is in high gain mode.

The time-domain waveform of I/Q channel output is shown in Fig. 13, when RF input signal is −35 dBm at 4.25 GHz and LO frequency is 4.2 GHz. The measured result indicates I/Q gain mismatch of 0.14 dB and phase mismatch of 3.4 ° . Phase error is introduced from RC PPF I/Q generation, and component mismatch in the RF signal path as well.

Table 1. Performance compared to recent works.

Parameter	Ref. [13]	Ref. [14]	Ref. [15]	This work
Frequency range	3–8 GHz	3–5 GHz	3–8 GHz	3–5 GHz
CG (High/Low) (dB)	29.4	37/4	23	27/8
NF (H/L) (dB)	7.87	3.6	4.5	4/12.5
IIP3 (H/L) (dBm)	−9.9	−22/2	−7	−11.5/ − 6.6
IIP2 (H/L) (dBm)	N/A	N/A	18	33/36
Power consumption	22.5 mA @ 1.5 V	34 mA @ 1.5 V	32.5 mA @ 1.2 V	18 mA @ 1.2 V
Technology	0.18 μm CMOS	0.13 μm CMOS	65 nm CMOS	0.13 μm CMOS

$1/f$ noise can be measured by directly observing the receiver output spectrum, when the LNA input is terminated with 50 Ω impedance. $1/f$ noise corner is measured to be at 200 kHz, which proofs the effectiveness of passive mixer in suppressing $1/f$ noise. The measured performance is summarized in Table 1, with comparison to some recent published works. It indicates that the proposed receiver achieves a high performance with low power consumption.

4. Conclusion

A low power, low noise receiver front-end for 3–5 GHz UWB is presented in this paper. The proposed circuit consists of a low-noise transconductance input stage for *V*–*I* conversion, a current driven passive mixer for frequency translation and loading TIA amplifiers for *I*–*V* conversion at output. Several low power design techniques such as capacitance-cross-coupling transconductor, quadrature passive mixer and passive poly-phase filter are used to reduce the receiver power consumption. Measurement results proof that the RF front-end achieves a performance adequate to meet the WiMedia UWB specification, and the power consumption is favorably compared to previous works. The proposed circuit is also applicable to multiband/multimode wireless system such as software defined radio (SDR), for its wide bandwidth and good suppression of $1/f$ noise.

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