Design and analysis of a highly-integrated CMOS power amplifier for RFID readers

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Abstract: To implement a fully-integrated on-chip CMOS power amplifier (PA) for RFID readers, the resonant frequency of each matching network is derived in detail. The highlight of the design is the adoption of a bonding wire as the output-stage inductor. Compared with the on-chip inductors in a CMOS process, the merit of the bondwire inductor is its high quality factor, leading to a higher output power and efficiency. The disadvantage of the bondwire inductor is that it is hard to control. A highly integrated class-E PA is implemented with 0.18-μm CMOS process. It can provide a maximum output power of 20 dBm and a 1 dB output power of 14.5 dBm. The maximum power-added efficiency (PAE) is 32.1%. Also, the spectral performance of the PA is analyzed for the specified RFID protocol.

Key words: CMOS power amplifier; RFID reader; matching network; bonding wires
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1. Introduction

As the worldwide market of radio frequency identification (RFID) has been growing tremendously[1,2], RFID has become an essential field of research in modern industry. Potential applications of RFID are driving hardware developers to merge RFID readers into mobile devices, such as PDAs and cell phones. In the integrated-circuit (IC) design field, much effort is directed to develop low-cost, high-efficiency solutions for a RFID system. Meanwhile, the persistent scaling of CMOS technology has made CMOS-based single-chip solutions very competitive for such short-range wireless standards. So, it is necessary to implement highly-integrated CMOS RFID products, such as mobile RFID readers[3,4].

In all of the RF front-end components, the integration of the CMOS power amplifier (PA) remains a challenge. Because of the low breakdown voltage, low trans-conductance capacity, and poor passive devices in CMOS process, it is hard to design a fully-integrated CMOS PA with high output power, efficiency, and linearity. Considering the battery lifetime of mobile devices, high-efficient non-linear PAs can provide better performances in mobile RFID readers if the linearity demand is not so strict. Among all the non-linear power amplifiers, class-E PAs are frequently selected for the RF domain[5–7]. Recent studies have demonstrated than class-E CMOS PAs can provide a high efficiency above 40% when fully integrated[8] and above 60% with external matching components[9].

The inductor is a key component in the design of a PA. Traditionally, RF IC designs have incorporated off-chip surface-mounted inductors. While these inductors offer an extremely high quality factor (Q) and generally a good performance, they are disadvantageous in terms of board-level complexity and overall system cost. In this paper, possible integrated inductors are discussed to decrease both complexity and cost. An alternative is the on-chip spiral inductor. But this has a lower Q factor (often lower than 10) and a larger error of the inductor value and Q (the error is often greater than 10%)[10]. On the other hand, a feasible alternative to off-chip inductor are bondwires. These have a predictable value of the Q factor. But the main shortcoming in a manufacturing environment is the lack of tight control of the bonding process. This issue is addressed in a later section of this paper. Also improvement methods to the implementation of the bondwire inductor are treated in detail.

In this paper, the resonant frequencies of each matching network of the PA are derived firstly. Then emphasis is focused on the design of a 915 MHz CMOS class-E PA for mobile RFID reader applications. The chip is fabricated in the 0.18 μm 1P6M CMOS process. Bondwire inductors are used in the output stage of the PA to achieve a low-cost and high-efficiency solution. The PA can provide a maximum output power of 20 dBm. The PA presents a 1-dB output power of 14.5 dBm while delivering a maximum power-added efficiency (PAE) of 32.1%.

2. Analyses of matching networks

The matching performance of a multi-stage PA is largely determined by the resonant frequency of the matching networks. In the course of designing a PA, it is necessary to research the matching circuits for the purpose of optimization. For example, three matching networks are included in a two-stage class-E PA, as shown in Fig. 1.

In the output matching networks, there are two resonant circuits; L_1, C_1 and L_2, C_2. The resonant frequency should be designed to ω_0, which is the working frequency of the PA.

$$\omega_0 = \frac{1}{\sqrt{LC}}. \tag{1}$$

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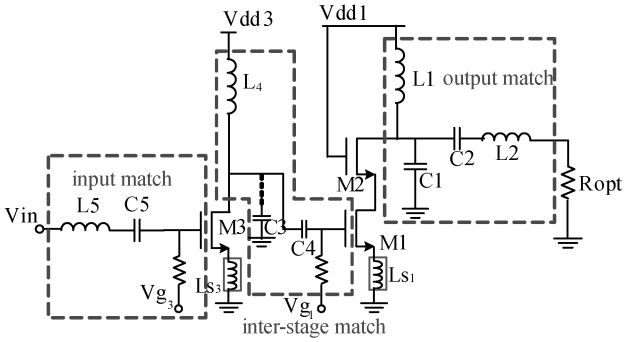

Fig. 1. Matching networks of class-E PA.

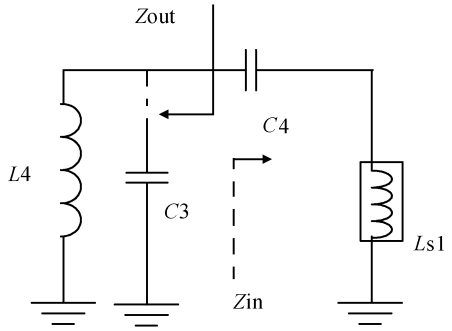

Fig. 2. Equivalent circuit of the inter-stage matching networks.

The equivalent circuit of the inter-stage matching networks is shown in Fig. 2. The impedance characteristic is shown as

$$Z_{\text{in}} = \text{j}\omega L_{\text{s1}} + \frac{1}{\text{j}\omega C_4} = \text{j}\omega(L_{\text{s1}} - \frac{1}{\omega^2 C_4}), \tag{2}$$

$$Z_{\text{out}} = L_4 // C_3 = \frac{\text{j}\omega L_4}{1 - \omega^2 L_4 C_3}. \tag{3}$$

To satisfy the conjugate matching condition, the output impedance of the input stage should be the complex conjugate of input impedance of the output stage. Thus, the resonant frequency of the inter-stage matching network can be derived as

$$\begin{aligned}\omega = \Big\{\Big[&\sqrt{(L_4C_3 + L_4C_4 + L_{\text{s1}}C_4)^2 - 4L_4L_{\text{s1}}C_3C_4} \\ &- (L_4C_3 + L_4C_4 + L_{\text{s1}}C_4)\Big] / 2L_4L_{\text{s1}}C_3C_4\Big\}^{1/2}.\end{aligned} \tag{4}$$

The purpose of the input matching network is to convert the input impedance to a specified value, such as 50 Ω. The equivalent circuit of the input matching networks is shown in Fig. 3. It can be derived that the input impedance is:

$$\begin{aligned}Z_{\text{in}} &= \text{j}\omega L_5 + \text{j}\omega L_{\text{s3}} + \frac{1}{\text{j}\omega C_{\text{gs}}} + \frac{G_{\text{m}}}{C_{\text{gs}}} L_{\text{s3}} \\ &= \text{j}\omega(L_5 + L_{\text{s3}}) + \frac{1}{\text{j}\omega C_{\text{gs}}} + \frac{G_{\text{m}}}{C_{\text{gs}}} L_{s3}.\end{aligned} \tag{5}$$

Thus, the resonant frequency of the input matching network can be derived as

$$\omega = \frac{1}{\sqrt{(L_5 + L_{s3})\, C_{\text{gs}}}}. \tag{6}$$

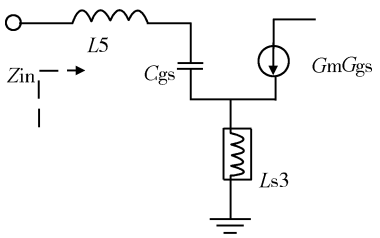

Fig. 3. Equivalent circuit of the input matching networks.

All the analyses in this section can provide the theoretic foundation for the design of the power amplifier.

3. Models of bandwire inductor and parrallel bondwires

Among all passive components, the inductor is a key component in the design of a PA. Unfortunately, a standard CMOS technology, which allows the realization of high-quality and exact-value inductors, does not exit. This is a dilemma for circuit designers, trying to select the inductors in PAs. The widely used inductor in CMOS process is the planar spiral inductor. It has a comparatively accurate 3D electromagnetic model and can be controlled exactly on the chip. But the Q values of planar inductors associated with CMOS processes are less than 10; sometimes as low as 3 or 4. This performance leads to power waste and, thus, a very low efficiency of the PA, especially at middle-to-high power output.

A feasible substitute to planar spirals in the output stage of a PA is the bondwire inductor. The main advantages of a bondwire inductor are its higher Q value and high self-resonant frequency, leading to a high efficiency and a high output power. On the other hand, the bondwires are a source of problems, especially causing instability.

In order to predict the inductance value as accurately as possible, the length of the bondwires must be controlled accurately. A handy rule of thumb to estimate the value of the bondwire is to use the relation 1 nH/mm[10]. To verify this relation, several S-parameters of individual bondwires and parallel bondwires are tested. For example, the left plot of Fig. 4 shows the test result of the S_{11} parameter of a 2 mm long bondwire with a 25-μm diameter from 20 MHz to 3 GHz. The estimation is proven by the value of 2.06 nH at 915 MHz. Meanwhile, the effective resistance of the tested bondwire is about 0.28 Ω. So, the Q of the individual bondwire is about 40 at 915 MHz.

There can be a substantial magnetic coupling between adjacent bondwires. So, the influence of magnetic coupling should be taken into account in the design. This coupling can be obtained by measuring the mutual inductance between bondwires. To obtain the mutual inductance value M of two parallel bondwires with equal length, the test result of S_{11} of two very close 2 mm long bondwires is also shown in the right plot of Fig. 4. The overall inductance value is 1.65 nH. So, the coupling coefficient can be derived as

$$k \approx \frac{M}{\sqrt{L_1 L_2}}. \tag{7}$$

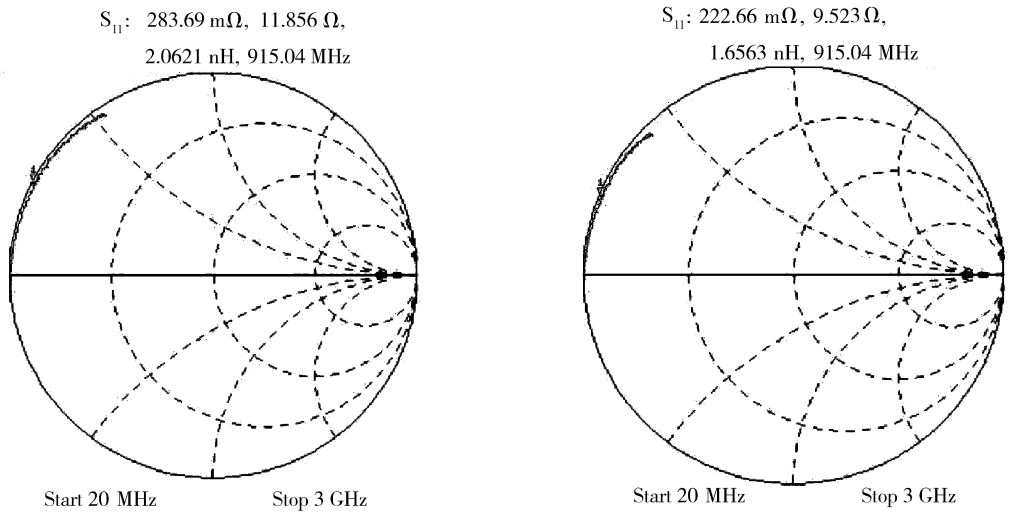

Fig. 4. S-parameter of a bondwire and its mutual inductance.

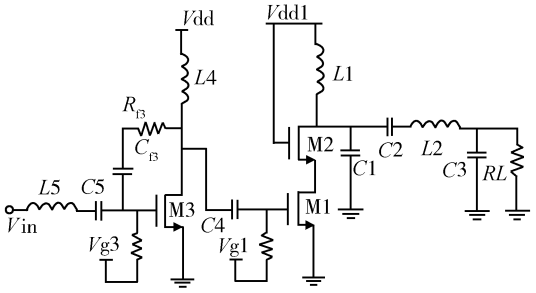

Fig. 5. Schematic of the class-E power amplifier.

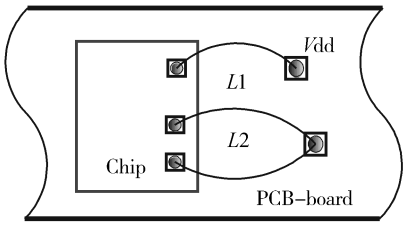

Fig. 6. Implementation of L_1 and L_2 with bondwires.

The determined Q value and coupling efficiency are utilized in the following design of a fully-integrated power amplifier.

4. Design of a class-E PA

Among all the switched-mode PAs, class-E is the most attractive candidate in terms of circuit simplicity and high frequency performance. Figure 5 shows the implemented two-stage class-E PA working at 915 MHz. The two stages are class AB and class E. Bondwire inductors are utilized for the drain inductor L_1 and the output stage inductor L_2. All the other components in the design are implemented on-chip.

Because the maximum drain voltage of a class-E power stage can be over 3.5 times the supply voltage, and the CMOS process sets the limit for the breakdown voltage of transistors, a cascode configuration along with the thick gate-oxide transistor M2 has been adopted to mitigate the oxide breakdown problem and, accordingly, to employ a larger supply voltage[11]. In the design, M1 is a 0.18-μm transistor and M2 is 0.34-μm transistor. With a supply voltage $V_{\rm dd}$ of 2.5 V, the maximum gate-drain voltage does not exceed 2 V, even for a input signal power as high as 0 dBm. Hence, the oxide breakdown does not occur. In the driver stage, resistor $R_{\rm f3}$ and capacitor $C_{\rm f3}$ form the series feedback to increase the overall stability.

For the output matching network, the components are selected so that the conditions of soft switching for class-E operation are met: (1) the voltage across the switch transistor M1 is zero when the switch is turned on; (2) the first derivative of the voltage is zero when the switch transistor is turned on. These conditions ensure no overlap between the current and voltage waveforms over the whole period of time. So, there is no power dissipation to the switch transistor, and a theoretical power efficiency of 100% can be achieved in the load. The components values can be calculated by[5]

$$R_{\rm opt} = \frac{8V_{\rm dd}^2}{P_{\rm out}(\pi^2+4)}, \tag{8}$$

$$C_2 = \frac{P_{\rm out}(\pi^2+4)}{8\omega V_{\rm dd}^2 Q_{\rm L}}, \tag{9}$$

$$L_2 = \frac{8V_{\rm dd}^2 Q_L}{\omega P_{\rm out}(\pi^2+4)}. \tag{10}$$

Also in the design, an output matching network was added after the L_2/C_2 resonator to transform the antenna resistance (50 Ω) into a lower value $R_{\rm opt}$. Furthermore, the inductor of the output matching network is added to L_2, forming a much larger inductor. The final value of L_2 can be as high as 10.5 nH. A sketch of L_2 with bondwire is illustrated in Fig. 6. It requires an exact orientation of the chip on the printed circuit board (PCB) board.

5. Experimental results

The proposed IC was fabricated in the 0.18-μm 1P6M CMOS process. The die photograph is shown in Fig. 7. It takes 1.1×2.5 mm^2 of silicon area including the pads. The two long

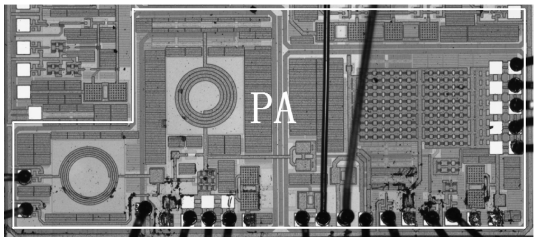

Fig. 7. Microphotograph of the chip.

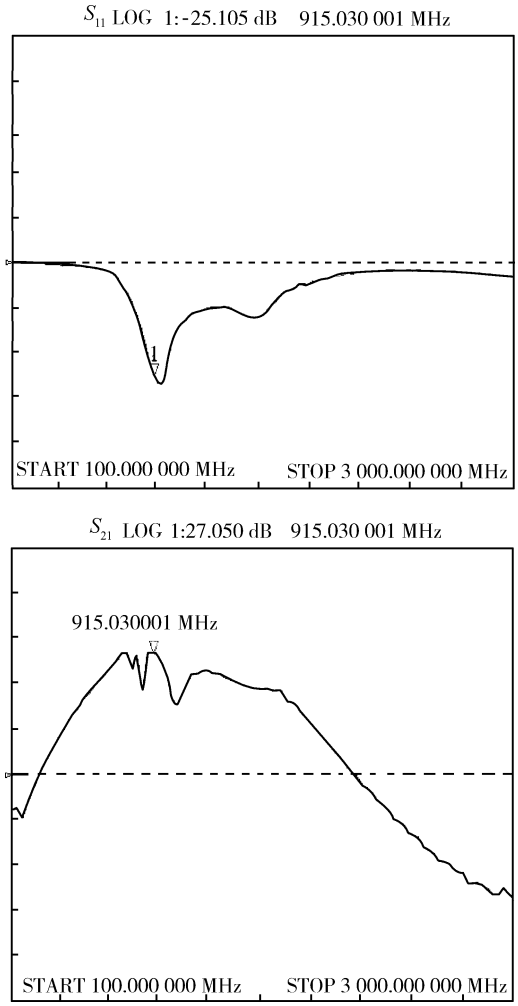

Fig. 8. Measured S-parameters (S_{11}, S_{21}) of the PA.

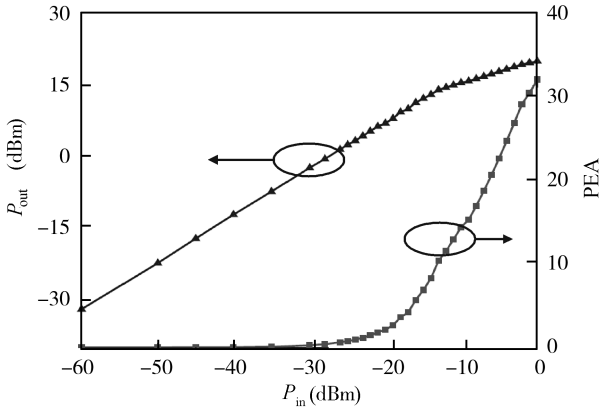

Fig. 9. Output power (P_{out}) and power-added efficiency (PAE) versus input power (P_{in}) of the PA.

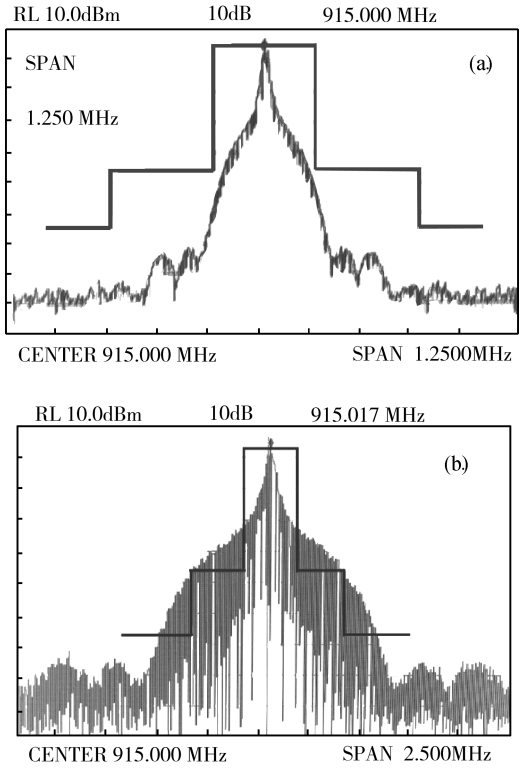

Fig. 10. Signal spectra of different data rates: (a) 10 kbps; (b) 40 kbps.

bondwires in the figure are the implementation of L_2 shown in Fig. 6. A PCB for testing the chip was also fabricated. The chip was directly glued to the PCB using an electrically and thermally conductive adhesive. Ground pads of the chip and the signal pads were wire-bonded to the gold-plated metal lines on the PCB.

The measured scattering parameters (S_{11}, S_{21}) of the PA are shown in Fig. 8. The PA can provide a small-signal gain of 27.0 dB at 915 MHz. The curve of S_{21} reveals the non-ideal matching of the resonator frequency of the driver and the output stages, thus, leading to a not ideal output power and efficiency. A possible improvement can be achieved by introducing a controllable capacitor to change the resonating frequency of the driver stage.

With a supply voltage of 2.5 V and a gate bias voltage of 0.52 V in the output stage, and a supply voltage of 1.8 V and a gate bias voltage of 0.85 V in the driver stage, the power amplifier consumes an overall DC current of 108 mA at an 1 dB output. The 1-dB output-power is about 14.5 dBm, and a maximum PAE of 32.1% is achieved. The maximum output power can be as high as 20.0 dBm. The measured output power and PAE are shown in Fig. 9.

The specified RFID protocol of ISO18000-6B is selected to verify the spectral performance of the PA[1]. The spectral mask is from the China National Standard[12]. When the transmitted data rate is 10 and 40 kbps, the corresponding signal spectra from the PA output are shown in Fig. 10. It can be seen that the 10 kbps data can satisfy the spectral mask while the 40 kbps data can not. In order to satisfy the faster transmitted data rate, a corresponding filtering method should be adopted before the transmitted data enters the PA.The latest paper reported a class-E power amplifier applied in RFID readers[13].

Table 1. Comparison of this work and Ref. [13].

Parameter	This work	Ref. [13]
Protocol	ISO18000-6B	EPC C1G2
Process	0.18 μm CMOS	0.25 μm CMOS
Frequency (MHz)	915	860–960
Gain (dB)	27	25
Supply voltage (V)	2.5	2.5
PAE	32.1%	> 35% @ 860–960 MHz
1 dB-output power (dBm)	14.5	> 24 @ 860–960 MHz
Structure	Two-stage class-E PA	Two differential class-E PAS polar transmitter
Area (mm^2)	2.75	3.52

A comparison of the PA performance in this work and the one in Ref. [13] is shown in Table 1. It can be seen that many parameters have the same value.

6. Conclusion

In this paper, a highly-integrated CMOS class-E PA for RFID readers is designed with the 0.18-μm CMOS process. Bonding-wire inductors are introduced in the output stage of the PA. Test and analyses focus on the merits and disadvantages of using a bonding wire. The designed PA can provide a maximum output power of 20 dBm. Its maximum power-added efficiency is about 32.1%. In order to improve the matching performance of the PA, resonant frequencies of each matching network are also derived in detail.

References

[1] ISO/IEC JTC 1/SC 31/WG 4 N0722: Information technology automatic identification and data capture techniques–Radio frequency identification for item management air interface–Part 6: parameters for air interface communications at 860–960 MHz, Nov. 2003

[2] EPC Radio-Frequency Identity Protocols: class-1 Generation-2 UHF RFID, Protocol for Communications at 860MHz–960MHz, Version 1.0.9, Jan 31th, 2005

[3] Khannur P B, Chen X, Yan D L, et al. An 860 to 960 MHz RFID reader IC in CMOS. IEEE Radio Frequency Integrated Circuits Symposium, 2007: 269

[4] Lee J, Choi J, Lee K H, et al. A UHF mobile RFID reader IC with self-leakage canceller. IEEE Radio Frequency Integrated Circuits Symposium, 2007: 273

[5] Sokal N, Sokal A. Class-E–a new class of high-efficiency, tuned single-ended switching power amplifiers. IEEE J Solid-State Circuits, 1975, SC-10: 168

[6] Mertens K L R, Steyaert M S J. A 700-MHz 1-W fully differential CMOS class-E power amplifier. IEEE J Solid-State Circuits, 2002, 37(2): 137

[7] Yoo C, Huang Q. A common-gate switched 0.9-W class-E power amplifier with 41% PAE in 0.25-μm CMOS. IEEE J Solid-State Circuits, 2001, 36(5): 823

[8] Aoki I, Kee S D, Rutledge D B, et al. Fully integrated CMOS power amplifier design using the distributed active-transformer architecture. IEEE J Solid-State Circuits, 2002, 37(3): 371

[9] Mazzanti A, Larcher L, Brama R, et al. A 1.4 GHz–2 GHz wideband CMOS class-E power amplifier delivering 23 dBm peak with 67% PAE. IEEE Radio Frequency Integrated Circuits (RFIC) Symp, Dig of Papers, 2005: 425

[10] Craninckx J, Steyaert M S J. A 1.8 GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler. IEEE J Solid-State Circuits, 1995, 30: 1474

[11] Sowlati T, Leenaerts D M W. A 2.4-GHz 0.18-μm CMOS Self-biased cascode power amplifiers. IEEE J Solid-State Circuits, 2002, 38(8): 1318

[12] Ministry of Information Industry of the People's Republic of China. 800/900 MHz RFID technology application rules (Try-out), April 20, 2007

[13] Shim S, Han J, Hong S. A CMOS RF polar transmitter of a UHF mobile RFID reader for high power efficiency. IEEE Microw Wireless Components Lett, 2008,18(9): 635