A capacitor-free CMOS LDO regulator with AC-boosting and active-feedback frequency compensation

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Abstract: A capacitor-free CMOS low-dropout (LDO) regulator for system-on-chip (SoC) applications is presented. By adopting AC-boosting and active-feedback frequency compensation (ACB-AFFC), the proposed LDO regulator, which is independent of an off-chip capacitor, provides high closed-loop stability. Moreover, a slew rate enhancement circuit is adopted to increase the slew rate and decrease the output voltage dips when the load current is suddenly switched from low to high. The LDO regulator is designed and fabricated in a 0.6 μm CMOS process. The active silicon area is only 770 × 472 μm^2. Experimental results show that the total error of the output voltage due to line variation is less than ±0.197%. The load regulation is only 0.35 mV/mA when the load current changes from 0 to 100 mA.

Key words: low-dropout regulator; AC-boosting and active-feedback; frequency compensation; capacitor-free
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1. Introduction

Power management is a very important issue in many portable electronic applications, e.g., cellular phones, handheld computes, and particularly implanted wireless biomedical chips. The low-dropout (LDO) linear regulator is one of the most popular power converters widely used in power management[1]. It is especially suitable for applications that require low-noise and precise supply voltages with few off-chip components. For a conventional LDO regulator, the closed-loop stability is achieved by the off-chip capacitor's equivalent series resistance (ESR), which provides an ESR zero for its open-loop transfer function and contributes pole-zero cancellation[2, 3]. In this method, however, the stability significantly depends on the ESR value that is not easily controlled and changes with temperature. Moreover, the frequency compensation can only be optimized in a narrow loading current range. This off-chip capacitor is the main obstacle for a full integration of LDO regulators in system-on-chip (SoC) designs. To overcome this issue, capacitor-free LDO regulators have been reported in Refs. [4–8]. These papers presented a way to remove the large external capacitor, while guaranteeing stability under all operating conditions. Removing the large off-chip capacitor also reduces the required board space and the overall cost of the design. In addition, removing the off-chip capacitor makes the LDO regulator suitable for SoC designs.

In this paper, a novel CMOS capacitor-free LDO regulator, which adopts a novel AC-boosting (ACB)[9] and active-feedback (AF)[10] frequency compensation (ACB-AFFC) technique, is proposed. The LDO regulator can maintain system stability independent of an off-chip capacitor. At the same time, the proposed LDO regulator can also provide a stable output under load conditions when using an off-chip capacitor. Moreover, a slew rate enhancement (SRE) circuit is presented.

2. Review of conventional LDO regulators

A conventional LDO system, as shown in Fig. 1, consists of an error amplifier, a PMOS power transistor M_{pass}, a voltage reference, and a feedback resistive network. The error amplifier compares V_{ref}, created by the voltage reference, with the feedback voltage V_{fb} and generates a voltage error signal which is fed into the gate of M_{pass} to change its overdrive. The change of overdrive adjusts the current of M_{pass} and causes the output voltage to be corrected to the proper level. The feedback loop needs a stable output voltage. Therefore, a large gain is required to ensure that the feedback loop requires stable, and frequency compensation becomes a critical issue in the LDO design. There is a trade-off between the loop gain and the bandwidth in the circuit. For the conventional circuit of Fig. 1, as analyzed in Ref. [3], the equivalent series resistance R_{esr} of the off-chip capacitor C_{out} is utilized to insert an ESR zero between low frequency poles and the unity gain frequency. However, the frequency response of the open-loop transfer function is different under different loading conditions. So the position of the ESR zero is strictly confined to a limited range. That is, R_{esr} and C_{out} must be designed very

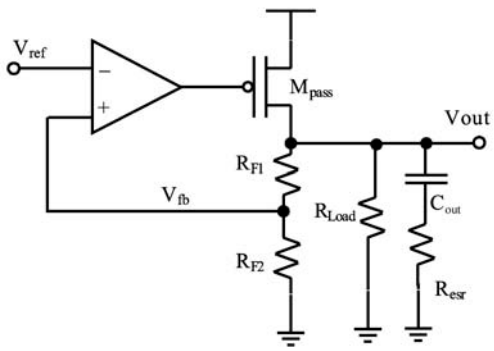

Fig. 1. Structure of a conventional LDO regulator.

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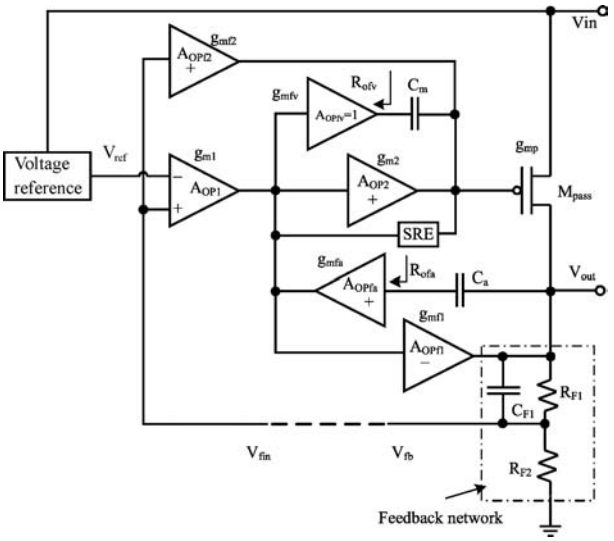


Fig. 2. Structure of the proposed LDO regulator.

carefully. On the other hand, the conventional LDO cannot be applied effectively to SoC designs due to the large off-chip capacitor needed for stability. So, a novel capacitor-free LDO structure with advanced frequency compensation, which overcomes the problems of the conventional LDOs, is presented in the next section.

3. Proposed LDO regulator

The architecture of the proposed LDO regulator adopting a novel ACB-AFFC technique is shown in Fig. 2. The AC-boosting compensation path is composed of the amplifier stage $A_{\rm opfv}$ and the compensation capacitor $C_{\rm m}$. The active-feedback compensation path consists of a feedback stage $A_{\rm opfa}$ and a compensation capacitor $C_{\rm a}$, which realizes the active-capacitive feedback network. $A_{\rm op1}$ is a high-gain error amplifier, which compares the reference voltage $V_{\rm ref}$ and the feedback voltage $V_{\rm fb}$, and $A_{\rm op2}$ is a high-gain high-output swing second stage. To achieve the push-pull effect at the output of $A_{\rm op2}$, a feedforward stage $A_{\rm opf2}$ is connected between the input of $A_{\rm op1}$ and the output of $A_{\rm op2}$. This feedforward stage $A_{\rm opf2}$ improves the transient response and simplifies the biasing scheme of the LDO regulator. The PMOS power transistor $\rm M_{pass}$ and the feedforward stage $A_{\rm opf1}$ form the push-pull output stage in the LDO regulator. SRE is the slew rate enhancement circuit, which will limit the drop of the output voltage when the load current of the LDO regulator is suddenly switched from low to high.

As shown in Fig. 2, the proposed LDO regulator can also be viewed as a feedback system consisting of a three-stage amplifier driving a large capacitive load, which is due to the internal power line under capacitor-free conditions or due to the off-chip capacitor. In the proposed technique, $A_{\rm opf1}$ and the active-feedback path (including $A_{\rm opfa}$ and $C_{\rm a}$) form a high-speed block (HSB), and $A_{\rm op2}$ and $\rm M_{pass}$ form a high-gain block (HGB). The HSB causes the high-frequency signals to bypass the slow-response HGB; therefore, the loop bandwidth of the proposed LDO can be further enhanced[10]. Besides, in this ACB-AFFC technique, an AC amplifier is also added in parallel with $A_{\rm op2}$, thus adding a second signal path to the second stage. The first path involving $A_{\rm op2}$ is a DC path used for a high DC gain, and the other path involving $A_{\rm opfv}$ is an AC path for boosting the high-frequency gain. That is to say, the AC path $A_{\rm opfv}$ creates another high-frequency high-speed path[9]. By adopting the mentioned two high-speed paths, the loop non-dominant pole of the proposed topology can be shifted to higher frequencies. Therefore, the loop gain-bandwidth product or the unity-gain frequency of the proposed LDO regulator is improved, and the stability of the LDO regulator is also improved. In contrast to using a passive-capacitive network, the compensation capacitors $C_{\rm a}$ and $C_{\rm m}$, which are connected in series with the gain stages $A_{\rm opfa}$ and $A_{\rm opfv}$, respectively, form the active-capacitive network in the proposed LDO regulator. This allows for a smaller compensation capacitor in this design.

The feedback network of the proposed LDO regulator consists of resistors $R_{\rm F1}$ and $R_{\rm F2}$, plus capacitor $C_{\rm F1}$. As reported in Ref. [5], a medium frequency zero should be created by the feedback-resistive network, in order to improve the stability of the LDO regulator. The transfer function of the feedback-resistive network can be written as[5]

$$\frac{v_{\rm fb}(s)}{v_{\rm out}(s)} = \frac{R_{\rm F2}}{R_{\rm F1}+R_{\rm F2}}\frac{1+s/z_{\rm f}}{1+s/p_{\rm f}}, \tag{1}$$

where zero $z_{\rm f} = (R_{\rm F1}C_{\rm F1})^{-1}$ and pole $p_{\rm f} = [C_{\rm F1}(R_{\rm F1}//R_{\rm F2})]^{-1}$. In order to cancel the effect of non-dominant poles in LDO regulators[5], the zero frequency should be lower than the pole frequency. That is to say, $R_{\rm F2}$ should be much smaller than $R_{\rm F1}$, so that $z_{\rm f} \ll p_{\rm f}$ can be achieved.

3.1. Stability analysis

The proposed LDO regulator is designed for SoC applications, and it is stable without an off-chip capacitor from a finite small current up to the full load current. Moreover, the LDO regulator adopts an advanced compensation scheme, and it is stable in the full load current range when an off-chip capacitor is connected at the LDO regulator output. However, the proposed LDO regulator has different loop-gain transfer functions under different modes of operation. There are two operation modes: with and without off-chip capacitor. In order to analyze the stability of the proposed LDO regulator in both modes, the following assumptions are made. These assumptions simplify the transfer function without losing accuracy with the goal of providing a clearer insight into the proposed structure.

(1) $g_{{\rm m}i}$, R_{oi} are the transconductance and the output impedance of amplifier stage $A_{{\rm op}i}$, respectively, where i = 1, 2, f1, f2, fv or fa. $g_{\rm mp}$ denotes the transconductance of $\rm M_{pass}$. C_1 and C_2 are the parasitic capacitances at the output of $A_{\rm op1}$ and at the gate of $\rm M_{pass}$, respectively.

(2) The equivalent input resistance of the common-gate amplifier stage $A_{\rm ofa}$ is equal to the reciprocal of its transconductance, i.e., $R_{\rm ofa} = 1/g_{\rm mfa}$.

(3) The loading capacitor $C_{\rm out}$ and the compensation

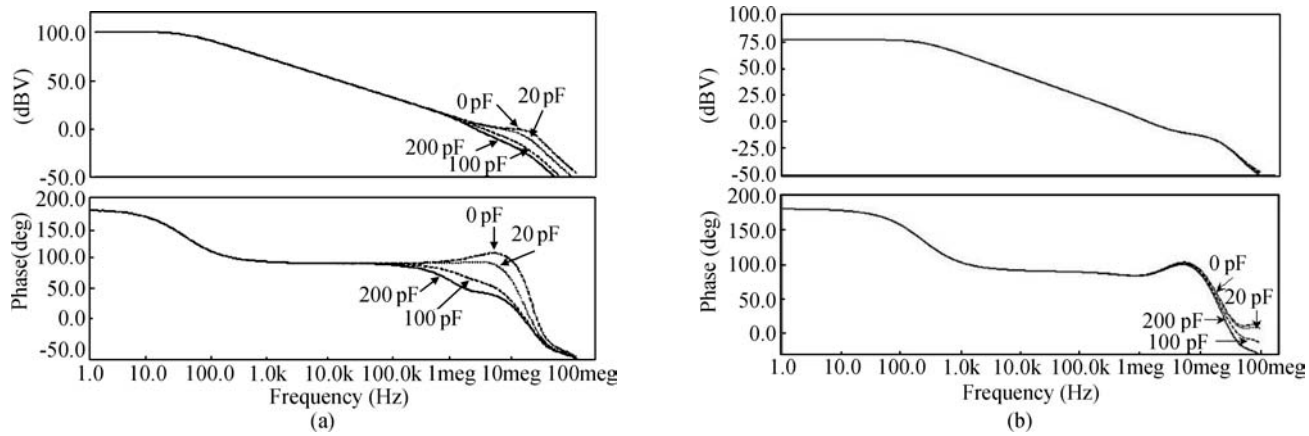


Fig. 3. Simulated loop gain of the proposed LDO regulator for different equivalent capacitances of the internal power line and without off-chip capacitor. (a) I_{out} = 100 μA; (b) I_{out} = 100 mA.

capacitors (C_a and C_m) are much greater than the lumped output capacitance of each stage (i.e., C_{out}, C_a and $C_m \gg C_1$, and $C_{out} \gg C_2$).

(4) The gains of each stage is much greater than one (i.e., $g_{m(1,2)}R_{o(1,2)}$, $g_{mp}R_{Load}$ and $g_{mfa}R_{o1} \gg 1$).

(5) The output resistance of A_{op2} is much greater than that of A_{opfv} (i.e., $R_{o2} \gg R_{ofv}$).

As shown in Fig. 2, the SRE circuit is a slew rate enhancement circuit, and it does not affect the frequency response of the LDO regulator. The SRE circuit will be analyzed in Section 3.2.

3.1.1. Without off-chip capacitor

In order to fully integrate LDO regulators into SoC designs, the off-chip capacitor should be eliminated. In this case, the load capacitance C_{out} results from the internal power line, and thus ESR does not exist. However, when the LDO regulator is used in SoC, it often has a minimum load current, which is about 100 μA to 10 mA depending on the application[5]. So the transconductance g_{mp} of M_{pass} will be very large, and the non-dominant poles of the proposed LDO regulator will shift to frequencies that are higher than the unity-gain frequency (UGF). Then the loop transfer function of the proposed LDO regulator can be approximated to

$$T_{\text{cap-free}}(s) = \frac{T_0(1 + s/z_1)(1 + s/z_2)(1 + s/z_f)}{(1 + s/p_{\text{-3dB}})(1 + s/p_f)}, \tag{2}$$

$$T_0 = g_{m1}g_{m2}g_{mp}R_{o1}R_{Load}R_{o2}R_{F2}\Big/(R_{F1} + R_{F2}), \tag{3}$$

$$p_{\text{-3dB}} = (g_{m2}g_{mp}R_{o1}R_{o2}R_{Load}C_a)^{-1}, \tag{4}$$

$$z_1 = \frac{(g_{mp}A_{2h}C_m + g_{mf1}C_{mp})g_{ofv}g_{m1}}{(g_{mp}g_{mf2}C_1 + g_{mf1}g_{m1}C_2)C_m}, \tag{5}$$

where $z_2 = g_{mfa}/C_a$, $C_{mp} = C_m + C_2$, C_{out} is the equivalent parasitic capacitance of the internal power line; $A_{2h} = (g_{m2} + g_{mfv})R_{ofv}$ can be regarded as the high-frequency gain of the second stage, which includes g_{m2} and the AC-boosting path g_{mfv}. From Eq. (2), it is concluded that all zeros are left-half-plane (LHP) zeros, and g_{mf2} only contributes an LHP zero but does not affect the location of the poles. $z_f \ll p_f$, and the effect of the pole p_f can be cancelled by z_f. The LDO regulator will be stable because it is similar to a single pole system. Under this condition, the load capacitance C_{out} comes from the internal power line and it is usually less than 200 pF[6, 8]. Figure 3 shows the simulated loop gain for different equivalent parasitic capacitances of the internal power-line without off-chip capacitor. When I_{out} = 100 μA, the phase margins are, respectively, 92 °, 84 °, 60 ° and 52 ° at C_{out} = 0, 20, 100 and 200 pF. For I_{out} = 100 mA, the phase margin is about 86 ° when C_{out} changes from 0 to 200 pF. From the simulation results, it is concluded that the system is stable under any operation condition that does not involve an off-chip capacitor.

3.1.2. With off-chip capacitor

In order to reduce the noise and the output voltage variation in the transient response, in some applications an off-chip capacitor is adopted. An off-chip capacitor affects the stability of the LDO regulator. In this situation, the zero $z_e = (R_{esr}C_{out})^{-1}$ will be located at a high frequency. Here, C_{out} is the off-chip capacitor and R_{esr} is the equivalent series resistance of C_{out}. That is to say, a low ESR is required. The simplified loop transfer function of the proposed LDO regulator can be given as

$$\begin{aligned} T_{\text{cap}}(s) = {} & [T_0(1 + s/z_1)(1 + s/z_2)(1 + s/z_e)(1 + s/z_f)] \\ & \times \left\{ \left(1 + \frac{s}{p_{\text{-3dB}}}\right) \left\{ 1 + s \left[R_{esr}C_{out} \right.\right.\right. \\ & \left. + \frac{g_{mf1}R_1C_mR_{ofv}C_2 + R_{ofa}C_{out}C_{mp}}{(g_{mp}A_{2h}C_m + g_{mf1}C_{mp})R_1} \right] \\ & + s^2 \frac{(R_{esr}g_{mf1}R_1 + R_{ofa})C_mR_{ofv}C_2C_{out}}{(g_{mp}A_{2h}C_m + g_{mf1}C_{mp})R_1} \\ & \left. \left. + \frac{(R_{ofa} + R_{esr})C_mR_{ofv}C_2C_1C_{out}}{g_{mp}A_{2h}C_m + g_{mf1}C_{mp}} s^3 \right\} \left(1 + \frac{s}{p_f}\right) \right\}^{-1}. \end{aligned} \tag{6}$$

In Eq. (6), all zeros are also LHP zeros. The cubic equation of the s term in the denominator of Eq. (6) can also be written as $G(s) = 1 + 1/p_1 + (p_1p_2)^{-1} + (p_1p_2p_3)^{-1}$. The pole p_3 is far away from the UGF because the dependence of p_3

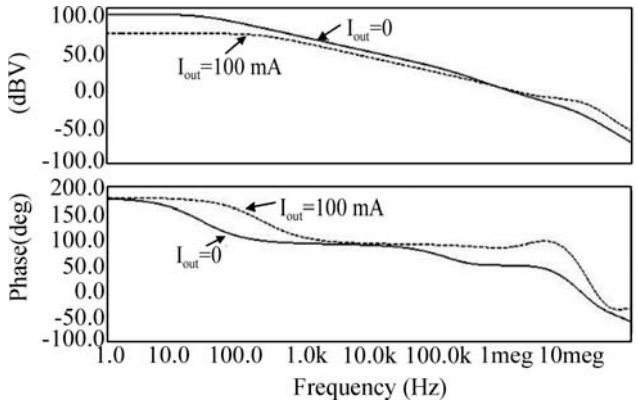


Fig. 4. Simulated loop gain of the proposed LDO with off-chip capacitor.

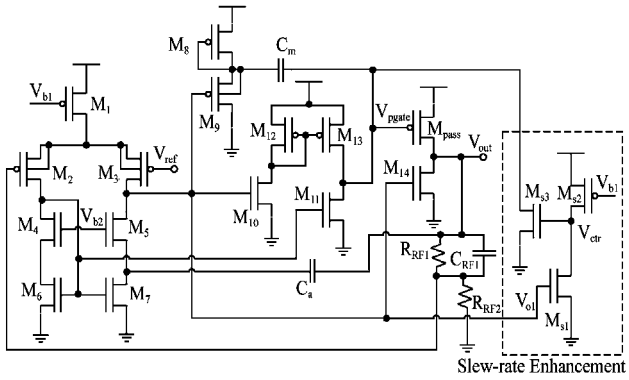


Fig. 5. Transistor-level circuit of the proposed LDO regulator.

on the parasitic capacitances C_1, and C_1 is very small. For the stability of the LDO regulator with off-chip capacitor, the pole p_3 is negligible. When the load current $I_{out} = 0$, the transconductance g_{mp} of M_{pass} is very small because the current from M_{pass} is very small. So, Equation (6) can be approximated to

$$T_{cap}(s) = \frac{T_0(1 + s/z_1)(1 + s/z_2)(1 + s/z_e)(1 + s/z_f)}{(1 + s/p_{-3dB})(1 + s/p_1 + s^2/p_1p_2)(1 + s/p_f)}, \quad (7)$$

$$p_1 = \frac{\left(g_{mp}A_{2h}C_m + g_{mf1}C_{mp}\right)R_1}{g_{mf1}R_1C_mR_{ofv}C_2 + R_{ofa}C_{out}C_{mp}}, \quad (8)$$

$$p_2 = \frac{1}{R_{esr}C_{out} + \dfrac{(C_mR_{ofv}C_2 - R_{esr}C_{out}C_{mp})R_{ofa}C_{out}}{g_{mf1}R_1C_mR_{ofv}C_2 + R_{ofa}C_{out}C_{mp}}}. \quad (9)$$

Since C_{out} is the off-chip capacitor and can be freely selected, it is practical to take the assumption of $p_1 < p_2$. According to Eq. (9), the zero z_e is close to the pole p_2, so a pole-zero elimination occurs. From the above analysis and assumption, it can be concluded that $g_{mp} > g_{mf1}$, $A_{2h} > 1$, and $g_{mf1}R_1 \gg 1$, and the pole p_1 is valid at $p_1 \leqslant g_{mp}A_{2h}(g_{mf1}R_{ofv}C_2)^{-1}$. In order to achieve $z_f < p_1$ in the current design, $R_{F1}C_{F1} > g_{mf1}R_{ofv}C_2(g_{mp}A_{2h})^{-1}$ should be satisfied. At the same time, in order to $z_f \ll p_f$, C_{F1} should be small, and thus the feedback resistor should be very large. Under this condition, the LDO regulator will be stable because the pole p_f is greater than the UGF. When there is a little increase of the load current, the LDO regulator is still stable since the relations of the poles and zeros are still valid.

When the LDO regulator drives a large load current, g_{mp} will be very large. In this situation, $p_e = (R_{esr}C_{out})^{-1}$ is created. Therefore, Equation (6) can also be approximated to

$$T_{cap}(s) = \frac{T_0(1 + s/z_1)(1 + s/z_2)(1 + s/z_f)}{(1 + s/p_{-3dB})(1 + s/p_{1n})(1 + s/p_f)}, \quad (10)$$

$$p_{1n} = \frac{R_{esr}(g_{mp}A_{2h}C_m + g_{mf1}C_{mp})R_1}{(R_{esr}g_{mf1}R_1 + R_{ofa})C_mR_{ofv}C_2}. \quad (11)$$

A new non-dominant pole p_{1n} is created. According to Eq. (11), $R_{F1}C_{F1} > g_{mf1}R_{ofv}C_2(g_{mp}A_{2h})^{-1}$ has to be satisfied in order to achieve the condition of $z_f < p_{1n}$. This is entirely the same result as derived from the stability analysis of a load current $I_{out} = 0$. So, the effect of the pole p_{1n} can still be canceled by the zero z_f. Besides, the pole p_f is still pushed to a higher frequency than UGF. Therefore, the LDO regulator is still stable. Figure 4 shows the simulated loop gain of the proposed LDO regulator with off-chip capacitor. When the load current changes from 0 to 100 mA, the phase margin varies from 52 ° to 85 °; so the system is stable.

From the above discussion on stability, the feedback resistors should satisfy $R_{F1} \gg R_{F2}$ in order to ensure $z_f \ll p_f$, and it is concluded that the required reference voltage should be smaller than the output voltage of the proposed LDO. In this paper, a reference voltage, which is smaller than 1 V, is adopted. At the same time, because of the effective pole-splitting effect by the ACB-AFFC, the nondominant pole frequencies are high. Therefore, a small capacitor C_{F1}, chosen to be 0.1 pF in this design, is required. In addition, the capacitor C_{F1} is connected to the output of the LDO regulator; so C_{F1} will not slow down the transient response.

3.2. Transistor-level circuit

The transistor-level circuit of the proposed LDO regulator is shown in Fig. 5. M1–M7 and M10–M13 realize, respectively, the error amplifier and the high-gain second stage. The differential pair (M2, M3) and transistor M10 generate transconductances g_{m1} and g_{m2}, respectively. The transconductance g_{mf2} (i.e. A_{opf2}) is realized by the transistor M11, which has a gate terminal connected to the gates of transistors M6 and M7. The quiescent current through A_{opf2} can be controlled by scaling the device ratios between transistors M6 and M11. In the transient state, the push-pull effect is achieved by transistors M11 and M13, which charge and discharge C_m during the negative slewing and positive slewing periods, respectively. M_{pass} is the power transistor of the proposed LDO regulator and the transistor M14 is the feedforward stage A_{opf1}. The feedback stage A_{opfa} is a common-gate amplifier. In order to minimize the systematic offset, the common-gate amplifier is realized by the transistor M5 of the error amplifier, and M5 generates g_{mfa}. M5 and compensation capacitor C_a form the active-capacitive-feedback network. The AC-boosting path is made up of M8, M9 and compensation C_m. In this design, the AC-boosting gain $A_{ofv} = 1$, which can be precisely controlled by the ratio of sizes of M8 and M9.

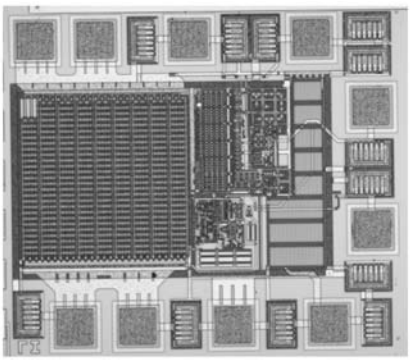


Fig. 6. Microphotograph of the LDO regulator.

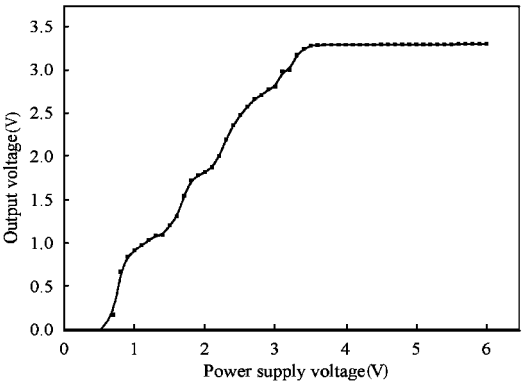


Fig. 7. Measured line regulation at I_{out}=1 mA.

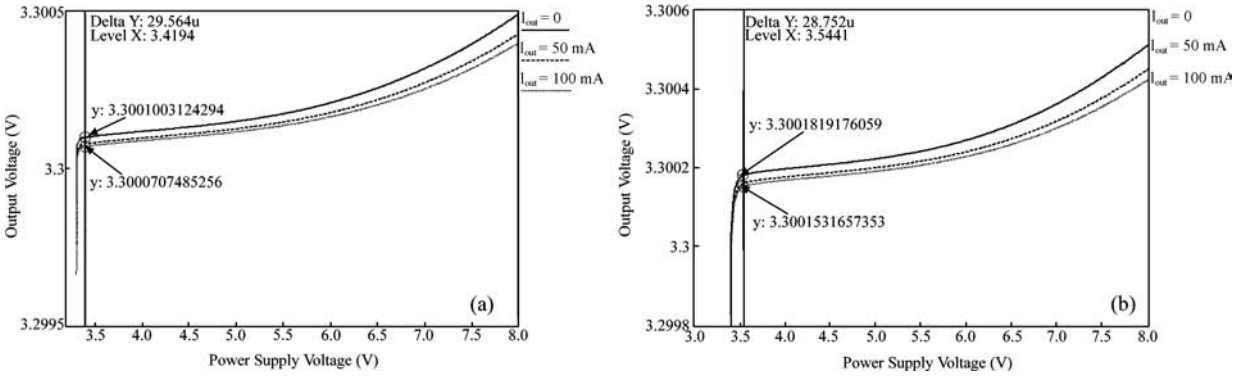


Fig. 8. Simulated line regulation at different load currents: (a) TT model; (b) SS model.

When the load current is suddenly switched from low to high, the output voltage V_{out} of the LDO regulator begins to drop. An output voltage dip will occur and the slew rate will be affected. In order to overcome this issue, an SRE circuit consisting of Ms1–Ms3 is designed, as shown in Fig. 5. For the SRE circuit, the saturation current in steady-state of Ms1 (i.e. I_{s1}) is larger than that of Ms2. So, the voltage V_{ctr} is low, causing the transistor Ms3 to turn off. With the load current I_{out} changing from low to high, the output voltage V_{out} of the LDO regulator will decrease, and the feedback voltage V_{fb} will drop. Thus, the voltage V_{o1}, which is the voltage V_{fb} amplified by the error amplifier A_{op1}, will also drop. This in turn decreases the current I_{s2}. It will make the voltage V_{ctr} increase enough to turn on Ms3, causing the gate voltage of the power transistor M_{pass}, i.e., V_{pgate}, to decrease. With M_{pass} sourcing more output current, the output voltage dip is reduced and the slew rate is enhanced. When the system is in steady-state, Ms3 turns off and the SRE does not affect the system.

4. Experimental results

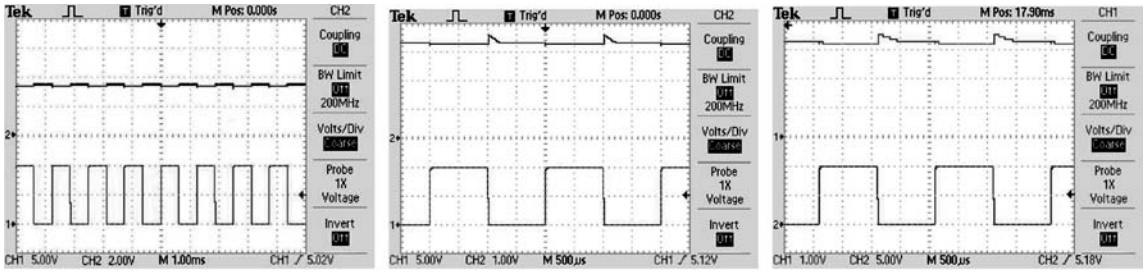
To verify the functionality of the proposed LDO regulator, it has been fabricated in the CSMC 0.6 μm CMOS process with V_{tn} = 0.728 V and V_{tp} = −1.02 V. The micrograph of the LDO regulator is shown in Fig. 6. The occupied chip area including pads and electrostatic discharge (ESD) protection circuits is 977 × 855 μm^2, and the active chip area (excluding pads and ESD) is 770 × 472 μm^2. The LDO is capable of operating down to 3.6 V when the output voltage is designed to be V_{out} = 3.3 V. The maximum output current is 100 mA with a dropout voltage of 300 mV.

The measured line regulation is given in Fig. 7. The output voltage deviation of the proposed LDO regulator is within 13 mV when the power supply voltage V_{DD} is changed from 3.6 to 6 V. As illustrated in Fig. 7, the proposed LDO regulator is capable of operating from 3.6 to 6 V, which covers a wide range of typical battery voltages. The simulated line regulation at different load currents is shown in Fig. 8. The simulation result indicates that the LDO regulator has a dropout voltage of about 120 mV and 240 mV with TT model and SS model, respectively. Due to the effect of technology drift and measurement precision, the measured dropout voltage is about 300 mV, and thus, it is about equivalent to the simulation result with the SS model.

Figure 9 shows the measured load transient responses of the proposed LDO regulator under three conditions: without off-chip capacitor, with a 0.22 μF off-chip capacitor, and with a 0.47 μF off-chip capacitor. Experimental results show that the proposed LDO regulator can respond quickly and can also rapidly recover to the preset output voltage. Moreover, the fast response time is beneficial for reducing the overshoot and undershot. Table 1 summarizes the performance of the proposed LDO regulator.

5. Conclusion

A capacitor-free LDO regulator with an AC-boosting and active-feedback frequency compensation technology is intro-



(a) (b) (c)

Fig. 9. Measured load transient responses at V_{DD} = 3.6 V: (a) 100 μA to 100 mA without off-chip capacitor; (b) 1 mA to 100 mA with C_{out} = 0.22 μF; (c) 1 mA to 100 mA with C_{out} = 0.47 μF.

Table 1. Performance summary of the LDO regulator.

Parameter		Ref. [4]	This work
Technology		0.5 μm CMOS	0.6 μm CMOS
Active chip area (μm^2)		600 × 480	770 × 472
Supply voltage (V)		4–7	3.6–6
Maximum output current (mA)		40	100
Quiescent current (μA)		39.8	120
Dropout voltage (mV)		200 @ 40 mA	300 @ 100 mA
Present output voltage (V)		3.8	3.3
Line regulation (mV/V)		4.6	5.42
Load regulation (mV/mA)		0.43	0.35
PSRR (dB)	100 Hz	–73.7	–70.8
	100 kHz	–33.9	–44.5

duced. The architecture of the proposed LDO regulator is simple and has a small silicon area. The theoretical analysis and the experiment results show that the proposed LDO regulator has an excellent performance. So the LDO regulator is well suited for SoC designs.

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