A current-mode buck DC–DC controller with adaptive on-time control

Li Yanming(李演明)[1,2,†], Lai Xinquan(来新泉)[1], Ye Qiang(叶强)[1], Yuan Bing(袁冰)[1], Jia Xinzhang(贾新章)[2], and Chen Fuji(陈富吉)[1]

(1 Institute of Electronic CAD, Xidian University, Xi'an 710071, China)

(2 Microelectronics Institute, Xidian University, Xi'an 710071, China)

Abstract: A current-mode buck DC–DC controller based on adaptive on-time (AOT) control is presented. The on-time is obtained by the techniques of input feedforward and output feedback, and the adaptive control is achieved by a sample-hold and time-ahead circuit. The AOT current-mode control scheme not only obtains excellent transient response speed, but also achieves the independence of loop stability on output capacitor ESR. In addition, the AOT current-mode control does not have subharmonic oscillation phenomenon seen in fixed frequency peak current-mode control, so there is no need of the slope compensation circuit. The auto-skip pulse frequency modulation (PFM) mode improves the conversion efficiency of light load effectively. The controller has been fabricated with UMC 0.6-μm BCD process successfully and the detailed experimental results are shown.

Key words: buck DC–DC; current-mode; adaptive on-time; loop stability; high efficiency
DOI: 10.1088/1674-4926/30/2/025007 **EEACC:** 1280; 2570D; 2570P

1. Introduction

For a complicatedly designed digital system (e.g. microprocessor, DSP and network system), the power supply is demanded to have the ability of fast transient response to the load. Especially, with the faster development of system operation speed, the demand on the transient response speed of the supply is getting higher. Because of the fixed switching period of conventional peak-current control schemes[1,2], the transient response speed is limited, and the slope compensation is needed to eliminate the subharmonic oscillation in the current loop when the duty cycle is greater than 50%[3–6]. Moreover, the slope compensation decreases the carrying capacity of the converter correspondingly[6,7].

As the clock is not needed to start a new cycle, the constant on-time (COT) control can trigger continuous on-time or off-time switching period when the load or line steps, so as to rapidly respond to changes in output. The techniques of input voltage feedforward and output voltage feedback can eliminate the effects of the input and output voltage on the switching frequency and make the converter operate in fixed switching frequency[8,9]. However, the biggest disadvantage of the voltage-mode on-time control is that enough ESR of output capacitor is needed to ensure the stability of the system[8–10], which restricts its application in the field demanding low voltage ripple. Besides, due to the existing of transmission delay, the switch frequency still will undergo some changes accordingly with the input and output voltage, especially when the duty cycle changes drastically and the switching frequency goes high.

A current-mode buck DC–DC controller circuit with adaptive on-time control is proposed in this paper, which is based on the techniques of the on-time controlled by input voltage feedforward and output voltage feedback. A sample-hold circuit is proposed to linearize the relationship between input voltage and on-time, and a charging time-ahead circuit is presented to eliminate the impact of transmission delay on switching frequency, which ensures that the switching frequency of the converter is independent on the inductor, output capacitor, input voltage, output voltage and load. The adaptive on-time (AOT) current-mode control not only obtains excellent transient response speed, but overcomes the dependence of loop stability on output capacitor ESR. Moreover, the AOT current-mode control has no subharmonic oscillation phenomenon, as a result, there is no need of the slope compensation. The input voltage is gained through sampling the signal of the switch mode when the high-side switch is on, which simplifies the pins of the chip and the application circuit. Concerned the efficiency, AOT control can change automatically into auto-skip PFM operation mode at light load, and the switching frequency decreases continuously with load decreasing, which improves conversion efficiency but does not increase output voltage ripple.

2. System design

2.1. Loop analysis

The schematic of a synchronous current-mode buck converter with the on-time control is shown in Fig.1, and its key operating waveforms in continuous conduction mode (CCM) are shown in Fig.2. During normal operation, error amplifier $g_{m(EA)}$ sets a current threshold corresponding to the voltage difference between the feedback voltage and the internal 0.75 V reference voltage. When the inductor current is rectified, the inductor current will be compared with the current

† Corresponding author. Email: ymli2004@126.com, xqlai@mail.xidian.edu.cn
Received 2 September 2008, revised manuscript received 14 November 2008

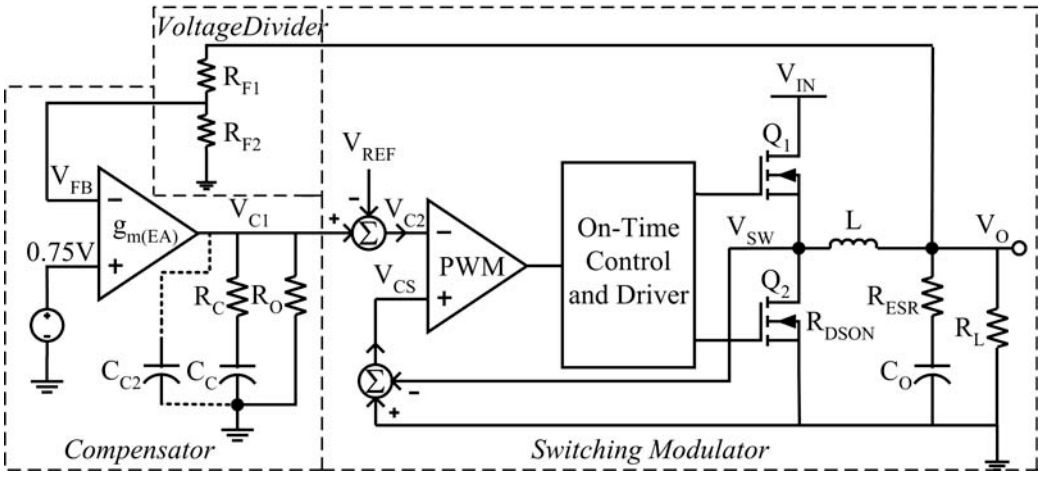

Fig.1. Schematic of current-mode buck converter with on-time control.

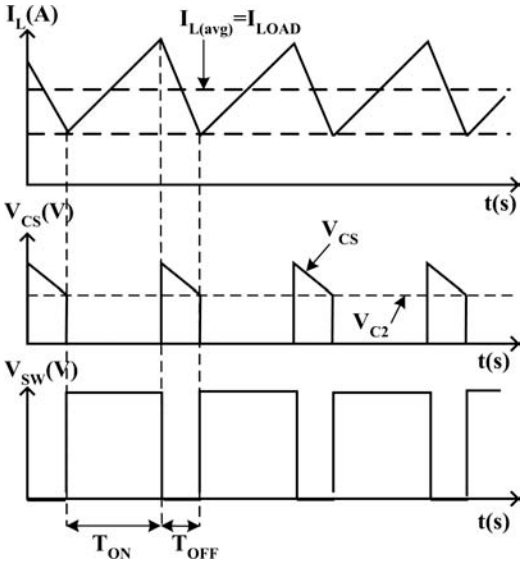

Fig.2. Key operation waveforms in CCM.

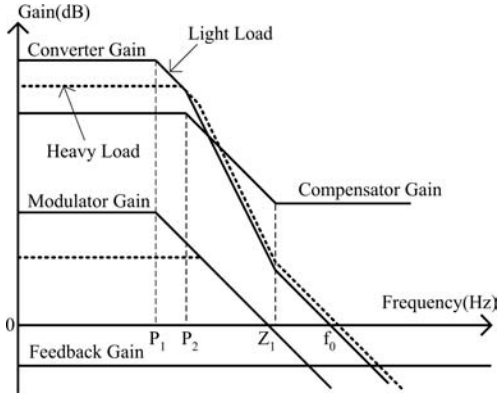

Fig.3. Frequency response of the proposed converter.

threshold. If the inductor current turns to be lower than the threshold, a high level signal from PWM will turn on high-side switch Q_1 and trigger the on-time one-shot timer. The high-side switch Q_1 turns off when the internal one-shot timer expires. The moment the feedback information indicates insufficient output voltage and inductor current becomes lower than current threshold, Q_1 turns on again. The procedure is repeated so that the controller can regulate the output effectively. The converter regulates output voltage by switching at a constant on-time and it modulates output power by adjusting the inductor valley current during the off-time.

The inductance current is sensed by the voltage drop V_{CS} via the conduction-resistance R_{DSON} of synchronous switch Q_2. This sampling method does not produce the additional sampling power loss, so it is beneficial to improve the conversion efficiency. Considering V_{C1} is too small, V_{C2} ($V_{C2} = V_{C1} - V_{REF}$) is generated by the level-shifting of V_{C1} to compare with V_{CS} at the PWM comparator.

As shown in Fig.1, the proposed buck converter can be partitioned into three portions, a voltage divider, a compensator, and a switching modulator. As the current-mode scheme directly controls the inductor current, a modulated current source including the power inductor can be linearized as a current source. This simplified model is true in the frequency space up to approximately a half of the switching frequency[11, 12].

The transfer functions of the three blocks are shown as

$$\begin{cases} H_1(s) = \dfrac{R_{F2}}{R_{F1} + R_{F2}}, \\ H_2(s) = -g_{m(EA)} \dfrac{R_O(1 + sC_CR_C)}{(1 + sC_CR_O)(1 + sC_{C2}R_C)}, \\ H_3(s) = g_{m(MOD)} \dfrac{R_L(1 + sC_OR_{ESR})}{(1 + sC_OR_L)}, \end{cases} \quad (1)$$

where $g_{m(EA)}$ is the transconductance of the error amplifier, $g_{m(MOD)}$ is the current sense transconductance of the modulator which is equal to $1/R_{DSON}$, R_O is the output resistance of the error amplifier, and R_L is the load resistance.

The system has two important poles. One is due to the compensation capacitor (C_C) and the output resistor of the error amplifier ($P_2 = 1/(2\pi C_CR_O)$), and the other is due to the output capacitor and the load resistor ($P_1 = 1/(2\pi C_OR_L)$). The system has one important zero ($Z_1 = 1/(2\pi C_CR_C)$), which is due to the compensation capacitor (C_C) and the compensation resistor (R_C). C_{C2} is used to cancel the zero caused by ESR of the output capacitor. In the case of ceramic capacitor, the ESR zero is much higher than the crossover frequency, so there is no need for C_{C2}.

The system crossover frequency, f_C, is of great significance where the feedback loop has the unity gain. Lower

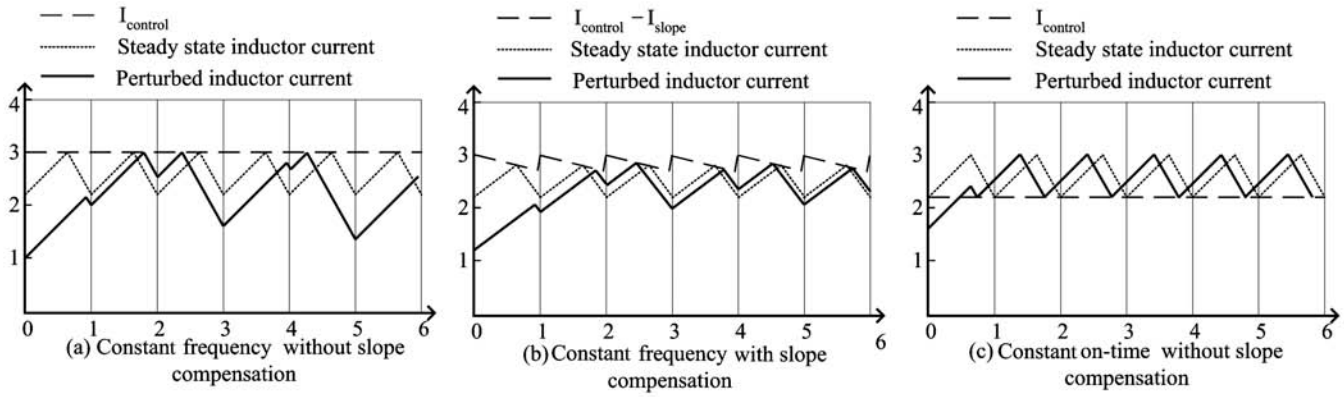

Fig.4. Comparison of inductor current for two current-modes.

crossover frequency results in slower line and load transient responses, while higher crossover frequency could cause system instability. However, the f_C should be kept below 1/3 of the switching frequency to avoid the effect of switching circuit delay. At crossover frequency, the total transfer function of the whole system, $H(s)$, is equal to 1, and we make the following assumptions: $1 + sC_CR_C \approx sC_CR_C$, $1 + sC_CR_O \approx sC_CR_O$, $1 + sC_OR_L \approx sC_OR_L$. So the f_C is given by

$$f_C = \frac{1}{2\pi}\frac{R_{F2}}{R_{F1}+R_{F2}}\frac{g_m}{C_O}\frac{R_C}{R_{DSON}}. \quad (2)$$

Note that higher R_C shows higher crossover frequency in cost of instability. If the transient response is not enough even with high R_C value, try to increase the output capacitance.

Figure 3 illustrates the frequency response of the converter using Bode diagram. In the light load conditions as the solid line shows, P_1 is the dominant pole while P_2 is the second pole. With the increase of load current as the dashed line shows, P_2 becomes the dominant pole while P_1 is pushed to a higher frequency. The frequency of Z_1 is near the crossover frequency of f_C which gives a 90° boost to the phase at the crossover frequency. For the load current changes in full ranges, the phase margin that a stable loop needs is guaranteed by Z_1. Changing the location of Z_1 can optimize the achieved phase margin.

It is well known that, for PWM duty cycles above 50%, the fixed frequency current-mode buck converters require a linear ramp (i.e., slope-compensation) to avoid subharmonic oscillation. The higher duty cycle is, the greater slope compensation is required[13]. However, the proposed on-time current-mode control topology does not need the slope compensation. Figure 4 provides an intuitive understanding of why the constant on-time current-mode control does not need slope compensation.

As seen in Fig. 4, a disturbance of inductor current causes the subharmonic oscillation phenomenon in fixed frequency peak current-mode control with large duty cycle, which can only be removed by adding the external slope compensation. However, if the inductor current suffers the same disturbance, the COT current-mode control will not appear the subharmonic oscillation phenomenon, and the disturbance of inductor current is eliminated only in one period without the slope compensation.

2.2. PFM operation mode in light load

On the one hand, the converter maintains working at a fixed frequency in CCM, and the switching frequency is determined by the T_{ON}. On the other hand, the synchronous switch will be shut down to make the system turn into discontinuous conduction mode (DCM) when the load current is lower than half of the inductor peak–peak current, and the loop will not trigger the next T_{ON} cycle until the output voltage is lower than the set value again. The interval between the every two switching cycles increases with the load decrease, which is called as auto-skip PFM operation mode. The start of the T_{ON} cycle is not controlled by the internal clock but only determined by the output voltage. Besides, each T_{ON} cycle appears separately, which is different from the "power save mode" in Ref.[2] and can avoid the increase of the output voltage ripple.

The combination of the PWM and PFM operation mode improves the conversion efficiency effectively. The test results show that the converter has a high efficiency in the load range of four orders of magnitude. Certainly, in the situations which have severe demand of the switching frequency, the system can always work in the forced PWM mode with fixed frequency by disabling the function of zero inductor current detect but in the cost of light load efficiency.

3. Circuit descriptions

3.1. Whole circuit implementation

The system function diagram of AOT control current-mode buck controller is shown in Fig.5. COMP1 is the current comparator which determines the turn-on of the high-side switch Q_1. COMP2 is the inductor current cross-zero comparator. When the inductor zero current is detected, the output signal of COMP2 will turn off Q_2, at the same time the system turns into PFM operation mode. To make sure the output signal of COMP2 available only when Q_2 is on, the gate signal of Q_2 is replaced by the delay of the DH signal to enable COMP2.

"Minimum Off Timer" is active after each T_{ON} to keep Q_1 off for the minimum time. In this way, the COMP1 will not be interrupted to generate misoperations of turning on Q_1 by

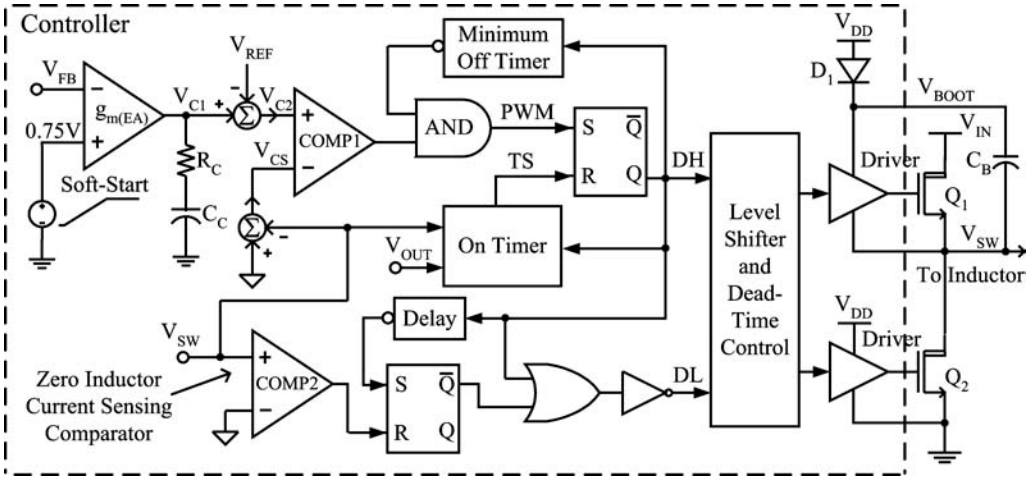

Fig.5. Function diagram of adaptive on-time control current-mode buck controller.

the switching noise in the off moment of Q_1. The minimum off time is 400 ns. When the load changes from light to heavy, V_{C1} is pulled up to a higher level quickly and COPM1 keeps outputting a low signal. So the converter works continuously at the switching period of turning on a T_{ON} time and turning off a minimum off-time, and the inductor current can response the change of the load rapidly. Contrarily, when the load changes from heavy to light, the output voltage is higher than the preset value and V_C will be pulled down to a lower level and COMP1 keeps outputting the low signal. Then Q_1 will not be turned on until output voltage turns to normal.

V_{DD} is 5 V power supply input for internal circuits and power switch gate driving circuits. The bootstrap structure is adopted in the driving circuit of the high-side switch. The driving circuit is composed by D_1 and C_B. V_{BOOT} is equal to $V_{DD} - V_{D1}$ when Q_1 is off, and V_{BOOT} is equal to $V_{SW} + (V_{DD} - V_{D1})$ (which is closed to $V_{IN} + (V_{DD} - V_{D1})$) when Q_1 is on. The driving circuit is always biased at the voltage of $V_{DD} - V_{D1}$. The advantages of the bootstrap structure are shown below: (1) The high-side switch is n-channel MOSFET whose on-resistance is smaller; (2) No additional high voltage power supply is needed; (3) None of high-voltage transistor is needed since the driving circuit is biased at a low voltage, which means taking much smaller chip area. But a level-shifter circuit is needed to provide a proper level logic for the high-side driving circuit. Meanwhile, the driving signal dead-time protection should be considered to avoid the two switches conducting at the same time.

3.2. AOT control and circuit implementation

The biggest disadvantage of COT control is that the switching frequency will change with the duty cycle. The relationship of duty cycle, D, and switching frequency, f_{SW}, is shown as

$$f_{SW} = \frac{D}{T_{ON}}. \tag{3}$$

The AOT control proposed in this paper can eliminate this change. Derived as follows: for the buck DC–DC converter,

$$T_{SW} = \frac{T_{ON}}{D} = \frac{V_{IN}}{V_{OUT}} T_{ON}, \tag{4}$$

where T_{SW} is the switching period. Supposing T_{ON} is inversely proportional to V_{IN} but proportional to V_{OUT}, T_{SW} would maintain as a constant no matter how V_{IN} and V_{OUT} change. Therefore, T_{ON} is redesigned as

$$T_{ON} = K_1 \frac{V_{OUT}}{V_{IN}}, \tag{5}$$

where K_1 = constant, and $T_{SW} = K_1$.

According to Eq.(5) we can conclude that the converter can maintain operating at a fixed frequency as long as T_{ON} is inversely proportional to the V_{IN} and proportional to the V_{OUT}. Figure 6 (a) presents the adaptive on-time generating circuit presented in this paper. In this generating circuit V_{IN} is sensed from switch mode, SW, when the high-side switch is on. Since the on-resistance of high-side switch is very small and the voltage drop across it can be neglected, this sampling method can not only decrease the amount of pins but also simplify the external application circuit design.

The divider resistance network is made up of R_1 and R_2 to serve as high-voltage insulation, the divider proportion $k = R_2/(R_1 + R_2)$. The sample-hold circuit consists of M_1 and C_1, where M_1 is the sampling control switch. M_1 turns on and V_{IN} is sampled by capacitance C_1 when the high-side switch is on. M_1 turns off as high-side switch is off and sensed voltage is kept in C_1. The delay time of the delay cell makes sure M_1 turns on only when high-side switch turn on. The voltage–current conversion circuit consists of the operational amplifier (OP), M_2 and R_3. The conversion relationship is expressed as $I_1 = V_{INS}/R_3$. C_2 is charged by I_1 through the current mirrors M_3 and M_4. When the charge voltage reaches V_{OUT}, the comparator COMP3 turns over and the on-time is over. At the very moment, C_2 is discharged quickly to 0 and the circuit is reset to wait for the next T_{ON} cycle.

Suppose $R_4 = 0$ and the charge time is T'_{ON}, then

$$T'_{ON} = \frac{C_2 V_{OUT}}{I_1} = R_3 C_2 \frac{V_{OUT}}{k V_{IN}} = T_{SW} \frac{V_{OUT}}{V_{IN}}, \tag{6}$$

where $T_{SW} = R_3 C_2 / k$ is the switching period. Equation (6) shows that T'_{ON} is inversely proportional to V_{IN} and proportional to V_{OUT}.

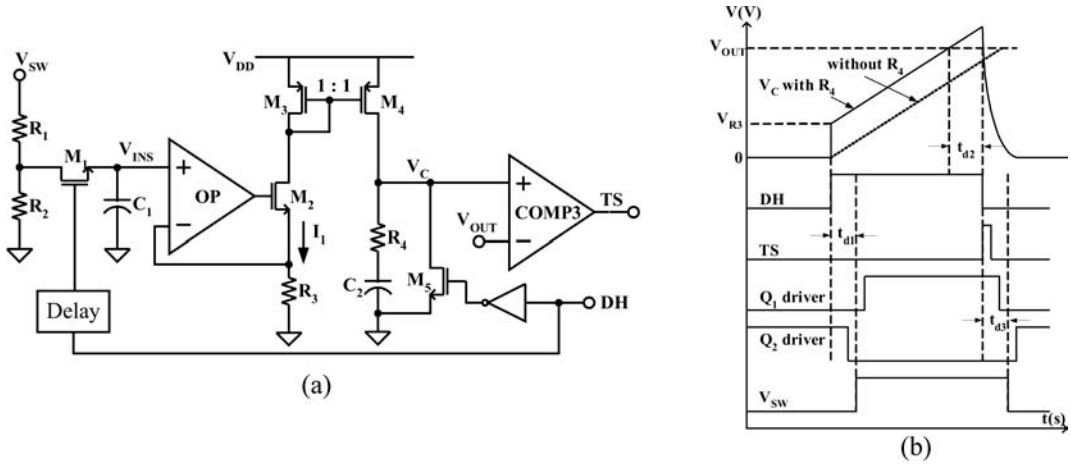

Fig.6. Adaptive on-time generation circuit and its charging curves: (a) Adaptive on-time generation circuit with time-ahead ability; (b) Charging curves.

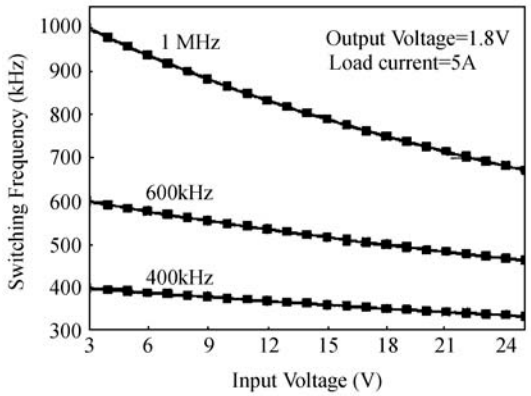

Fig.7. Simulation results of the effect of delay time on switching frequency.

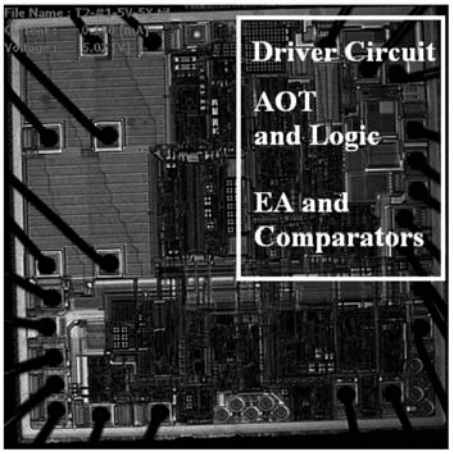

Fig.8. Micrograph of the proposed buck DC–DC controller.

As a matter of fact, the impact of transmission delay on the on-time should be considered. The delay time mainly includes the comparison time of COMP3, T_{D2}, and the transmission delay time of gate driving signal, T_{D1}. The charge time sequence is shown in Fig.6 (b). To simplify the analysis, we suppose that both the rising and falling edges of the switching MOSFET gate driving signal are ideal and calculate the value of on-time from the middle of the dead time. The comparison time of COMP3 is about 40 ns. The delay time from DH turning high to Q_1 turning on, T_{D1}, consists of logic delay, level-shifting delay and driving delay, which is approximately 20 ns. The delay time from DH turning low to Q_1 turning off, T_{D3}, consists of logic transmission delay, level-shifting delay and driving delay, which is approximately 20 ns. Since T_{D1} and T_{D3} are approximately equal and have the opposite effect on T_{ON}, their effect can be cancelled each other, and the practical T_{ON} is expressed as

$$T_{ON} = T_{ON}^{'} - T_{D1} + T_{D2} + T_{D3} \approx T_{ON}^{'} + T_{D2}. \quad (7)$$

The effect of T_{D2} on the switching frequency becomes stronger with T_{ON} decreasing. Figure 7 shows the relationships of switching frequency and input voltage when switching frequency is set to 400 kHz, 600 kHz, 1 MHz and T_{D2} is 40 ns. When the input voltage changes from 3 to 25 V, the switching frequency changes 60, 130 and 320 kHz respectively. Longer T_{D2} causes the larger change of switching frequency.

In order to eliminate the effect of the delay time on T_{ON}, a time-ahead quantity is introduced to offset the delay time. R_4 in Fig.6 (a) plays the time-ahead role. The theoretical derivation is shown as

$$V_C = V_{C1} + V_{R4} = \frac{T_{ON}^{'} I_1}{C_2} + I_1 R_4 = T_{ON}^{'} \frac{V_{INS}}{R_3 C_2} + \frac{V_{INS}}{R_3} R_4. \quad (8)$$

Making the equation equal to V_{OUT}, $T_{ON}^{'}$ can be calculated as

$$T_{ON}^{'} = R_3 C_2 \frac{V_{OUT}}{k V_{IN}} - R_4 C_2 = T_{SW} \frac{V_{OUT}}{V_{IN}} - R_4 C_2. \quad (9)$$

Combining with Eq.(7),

$$T_{ON} = T_{SW} \frac{V_{OUT}}{V_{IN}} - R_4 C_2 + T_D. \quad (10)$$

Choosing the proper parameter to ensure $R_4 C_2 = T_D$, we have $T_{ON} = T_{SW} \frac{V_{OUT}}{V_{IN}}$.

According to the analysis above, The T_{ON}, which is inversely proportional to the V_{IN} and proportional to the V_{OUT}, is obtained by the design of sampling maintain circuit and the charge time-ahead circuit. So the switching frequency of the converter can maintain constant with the change of V_{IN} and V_{OUT}, and has no correlation with the inductance, output capacitance and load.

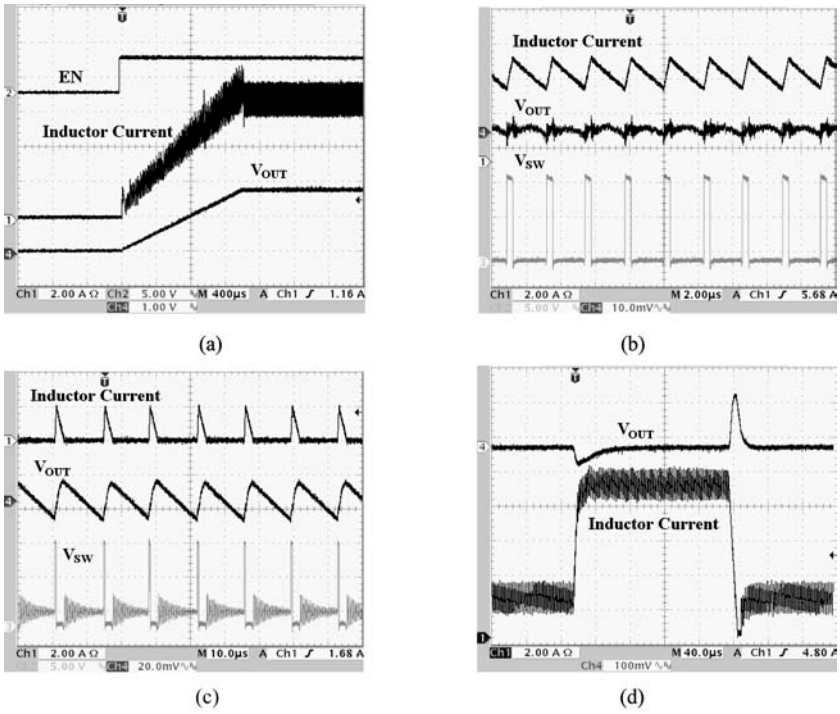

Fig.9. Operation waveforms (V_{OUT} = 1.8 V, V_{IN} = 12 V, C_{OUT} = 4 × 47 μF ceramic capacitor, L = 2.2 μH, high-side MOSFET: IRF7821, Low-side MOSFET: IRF8113); (a) Soft start; (b) CCM; (c) DCM; (d) Load transient response (2.5 to 9 A).

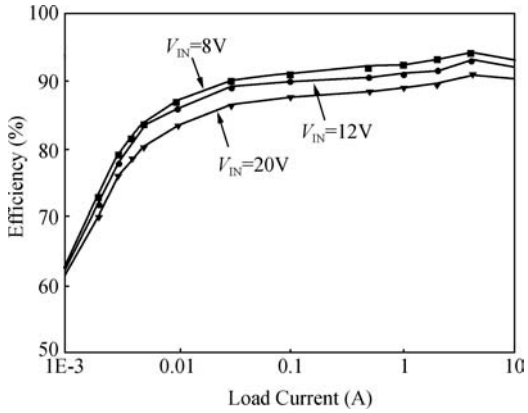

Fig.10. Efficiency versus input voltage.

3.3. Other circuit

The comparator COMP1, COMP2, COMP3 and the error amplifier shown in Figs.5 and 6 are designed with the typical differential structures. The bias currents and reference voltages for all the various analog building blocks are generated and derived from on-chip proportional-to-absolute temperature (PTAT) current generator and bandgap reference circuits. The controller also integrates the soft-start[14], power-good, over-voltage and under-voltage protection circuits. Although ultimately necessary for a practical solution, the design details of these circuits bring little value to the foregoing AOT current-mode scheme and are therefore excluded in this presentation.

4. Experimental results and discussions

The buck DC–DC controller presented in this paper has been integrated in a power supply IC of DDR memory which has been fabricated with UMC 0.6 μm BCD process. The micrograph of the IC is shown in Fig.8. The error amplifier, comparators, AOT and driving circuit are marked with white block in the layout whose total area is about 1.2 mm^2.

Figure 9 shows the operation waveforms of the system. Figure 9 (a) presents the soft-start waves of the converter, and the process of start-up is very smooth with time of about 1.3 ms. Figures 9 (b) and 9 (c) give the operation waveforms in CCM and DCM separately. With heavy load, the converter works in PWM mode at the fixed frequency of 400 kHz, and the output ripple is very small. With light load, the converter operates in the auto-skip PFM mode. In the PFM mode, the main MOSFET turns on to charge the output capacitor for a fixed time when the output is lower than the set value and then keep shutting down till the output is lower than the set value again. The switch from CCM to DCM appears at 1 A load. The switching frequency of PFM mode decreases with the load descending and the output voltage ripple is only 20 mV. As is shown in Fig.9 (d), the load current jumps from 2.5 to 9 A, the inductor current responses quickly, and the output voltage is almost steady with little change and no oscillation.

Buck controller has a 300 μA quiescent current, including the current consumption of reference, bias and other protection blocks. Figure 10 displays the converter efficiency curves respectively in the case of 1.8 V output voltage and 8, 12 and 20 V input voltage. It can be obtained that the efficiency is higher than 90% at the load range from 0.1 to 10 A for V_{IN} 8 V/12 V, and the lowest efficiency is also higher than 60% at 1 mA load which indicates that PFM mode made important contributions to the increase of light load efficiency. The relationship between switching frequency and V_{IN} is given in Fig.11. Although the input voltage changes from 3 to 25 V, the

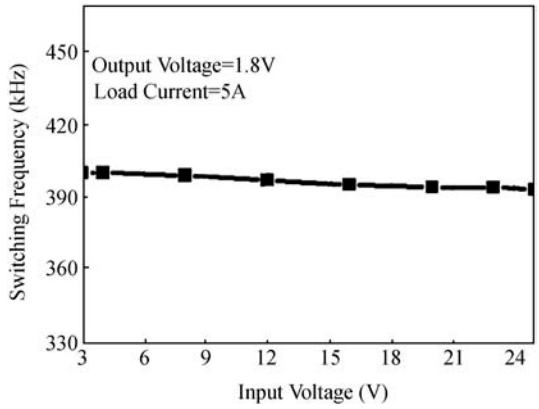

Fig.11. Switching frequency versus input voltage.

switching frequency variation quantity is less than 10 kHz.

5. Conclusion

A novel adaptive on-time control current-mode scheme for buck DC–DC converters is proposed, designed, built, and experimentally validated with an IC prototype from UMC 0.6 μm BCD process technology. With the AOT control, the converter can operate at 400 kHz fixed switching frequency which is not influenced by output, input and load. The current-mode AOT control not only overcomes the dependence of loop stability on output voltage ripple in the voltage-mode on-time control, but also obtains excellent transient response speed. Furthermore, the auto-skip PFM operation mode improves the conversion efficiency of light load greatly.

References

[1] Ma F F, Chen W Z, Wu J C. A monolithic current-mode buck converter with advanced control and protection circuits. IEEE Trans Power Electron, 2007, 22(5): 1836

[2] Yuan Bing, Lai Xinquan, Li Yanming, et al. High efficiency realization of a DC–DC converter at light loads for portable applications. Journal of Semiconductors, 2008, 29(6): 1198 (in Chinese)

[3] Fang C C. Exact orbital stability analysis of static and dynamic ramp compensations in DC-DC converters. Proceedings of the IEEE International Symposium on Industrial Electronics, 2001, 3: 2124

[4] Li Yanming, Lai Xinquan, Chen Fuji, et al. An adaptive slope compensation circuit for buck DC-DC converter. 7th Int Conf ASIC Proc, Guilin, IEEE Press, 2007: 608

[5] Ridley R B. A new continuous-time model for current-mode control. IEEE Trans Power Electron, 1991, 6(2): 271

[6] Ye Qiang, Lai Xinquan, Li Yanming, et al. A piecewise linear slope compensation circuit for DC-DC converters. Journal of Semiconductors, 2008, 29(2): 281 (in Chinese)

[7] Wang Hongyi, Lai Xinquan, Li Yushan. Reducing the slope compensation effect on the load capacity of DC-DC converters. Chinese Journal of Semiconductors, 2006, 27(8): 1484 (in Chinese)

[8] National Semiconductor Corporation. High voltage (80V) step down switching regulator. Online: http://cache.national.com/ds/LM/LM5007.pdf

[9] Texas Instruments. Dual synchronous step-down controller for low voltage power rails. Online: http://focus.ti.com/lit/ds/symlink/tps51124.pdf

[10] Li Yanming, Lai Xinquan, Yuan Bing, et al. Design and implementation of a Buck DC–DC controller with adaptive on-time control. Journal of Semiconductors, 2008, 29(7): 1396 (in Chinese)

[11] Mitchell D, Mammano B. Designing stable control loops. TI Analog Applicant, 2002

[12] Deisch C W. Switching control method changes power converter into a current source. IEEE Power Electronics Specialists Conference, 1978: 300

[13] Smith G. Understanding nonlinear slope-compensation: a graphical analysis-Part 1 & Part 2. National Semiconductor, 2007

[14] Li Yanming, Lai Xinquan, Yuan Bing, et al. An on-chip soft-start circuit for DC–DC switching regulators. Journal of Semiconductors, 2008, 29(6): 1210 (in Chinese)