A novel low-noise linear-in-dB intermediate frequency variable-gain amplifier for DRM/DAB tuners

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Abstract: A broadband CMOS intermediate frequency (IF) variable-gain amplifier (VGA) for DRM/DAB tuners is presented. The VGA comprises two cascaded stages: one is for noise-canceling and another is for signal-summing. The chip is fabricated in a standard 0.18 μm 1P6M RF CMOS process of SMIC. Measured results show a good linear-in-dB gain characteristic in 28 dB dynamic gain range of –10 to 18 dB. It can operate in the frequency range of 30–700 MHz and consumes 27 mW at 1.8 V supply with the on-chip test buffer. The minimum noise figure is only 3.1 dB at maximum gain and the input-referred 1 dB gain compression point at the minimum gain is –3.9 dBm.

Key words: VGA; noise-canceling; linear-in-dB; CMOS
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1. Introduction

Recently, digital radio broadcasting is widely researched worldwide. Digital radio mondiale (DRM)[1] and digital audio broadcasting (DAB)[2] have been introduced as digital standards for radio broadcasting in different frequency bands. However, most previous designs have less integration scale. Especially, as we know, there is no monolithic RF front-end in DRM band yet in the world. The required tuner should deal with the signals with input frequency from 148 kHz to 1.5 GHz. For DRM/DAB radio tuners, VGAs require a sufficiently high gain, a low noise figure (NF), and a high linearity. In addition, it is highly desirable to implement the amplifier in CMOS technology in order to perform a high level integration. This poses other design challenges due to the inferior RF characteristics of CMOS, such as large parasitic capacitance and low transconductance.

There are two existing solutions for VGAs, depending on whether the control signal is digital or analog. The digitally-controlled VGAs use a series of switchable resistors or switched-capacitors to achieve variable gain[3]. The gain varies as a discrete function of the control signals, which can lead to discontinuous signal phases that can cause problems in many systems. The VGAs controlled by analog signals typically adopt variable transconductance or triode transistor. With these topologies, the gains can be controlled continuously, but obtaining a wide exponential gain variation as a function of control voltage is a severe problem, especially in CMOS technology. In recent CMOS-based analog VGA designs, pseudo-exponential[4] and Taylor series[5] approximation functions are used in linear-in-dB gain control circuit implementations. But CMOS-based VGAs that adopt these functions typically offer less than 15 dB of gain variation. The VGAs that adopt the signal-summing technique using the Gilbert cell are reported in Refs. [6–8]. They offer a high operating frequency, a moderate noise, and a moderate distortion. Even so, it is hard to satisfy the high demand of noise and linearity in DRM/DAB system. An effective solution to achieve a wide exponential gain variation is to use the bipolar transistors[9], but this requires a high amount of power dissipation and is not compatible with the standard CMOS technologies. Some other approximate exponential functions are used to design VGAs to achieve wide exponential gain control[10]. Although 90 dB linear range is achieved, it suffers from narrow bandwidth and high distortion. This paper reports a new analog VGA that can provide a wide gain variation, low noise figure and low distortion.

2. Design specification

A double conversion low-IF DRM/DAB radio tuner architecture is shown in Fig. 1. The RF signal is received by the antenna and then is filtered by the band-pass filter arrays to get the signals of different frequency bands. At the first stage of the tuner, the weak RF signal is amplified by the LNA. Then, all-channel signals are converted down to 35.452 MHz first IF signals (I and Q) by a single quadrature mixer. At last, the RF signal is converted down to 173 kHz (DRM) and 2.048 MHz (DAB) second IF signals (II, IQ, QI, QQ) by a double quadrature mixer. The polyphase filters make it easier to reject the

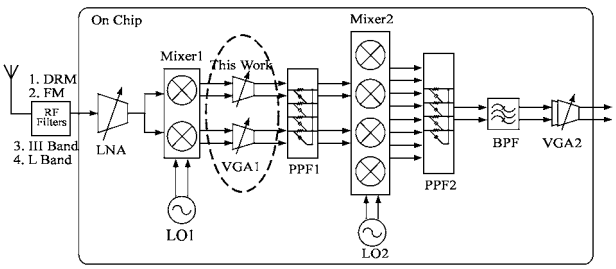

Fig. 1. A double conversion DRM/DAB tuner architecture.

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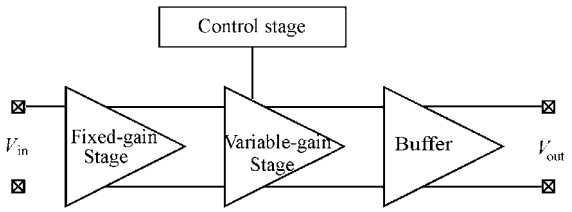

Fig. 2. Block diagram of the proposed VGA.

image signals compared to using an image reject structure as in heterodyne receivers.

We aim to design a low noise IF VGA for DRM/DAB systems. In a DRM/DAB system, the receiver requires at least 90 dB of dynamic gain variation and splits into RF and IF/baseband stages. There are three variable-gain stages in the proposed DRM/DAB tuner, the variable-gain LNA, the first VGA (VGA1) and the second VGA (VGA2). The complex double quadrature mixer (Mixer2) with polyphase filters (PPF1 and PPF2) after the VGA1 usually suffers from high insert loss and noise figure. Thus, to satisfy the total system design specifications, the gain of VGA1 must be high enough, meanwhile, the noise figure should be small. A NF of 10 dB and an input-referred 1 dB gain compression point (P_{1dB}) of –20 dBm are required at maximum gain to achieve a wide dynamic range receiver. The P_{1dB} is determined to be –8 dBm at minimum gain. The power dissipation target is 30 mW with the measurement buffers.

3. Circuit techniques

Figure 2 shows the block diagram of the overall VGA. The VGA adopts two amplifying blocks in cascade. The first stage is a fixed-gain amplifier exploiting the noise-canceling technique[11], while the second one is modified signal-summing variable-gain stages based on linear-in-dB gain control circuits[8]. The low NF characteristic is decided by the fixed-gain stage and the low distortion characteristic is decided by the variable-gain stage. Thus, compared with the previous work in Refs. [6–8], the noise and the distortion are decoupled. The buffer is added for the convenience of measurements, providing high-input and 50 Ω output impedance.

3.1. Fixed-gain stage

The fixed-gain stage is a full differential amplifier exploiting a noise-canceling technology. A half part of the circuit schematic is now taken into account in Fig. 3. The purpose of the circuit is to suppress noise contribution of input stage (M11 and M12). The noise current of M11 and M12 is given by

$$\overline{i_{n_{11}}^2} = 4kT\gamma g_{d_1}\Delta f + \frac{K}{f}\Delta f, \quad \overline{i_{n_{12}}^2} = 4kT\gamma g_{d_2}\Delta f + \frac{K}{f}\Delta f. \quad (1)$$

The first and the second parts are contributed by the channel thermal noise and the flicker noise of M11 and M12, respectively. The M11 and M12 are the current-reuse structure[12]. Two noise currents flow from R_f to R_s, and cause two

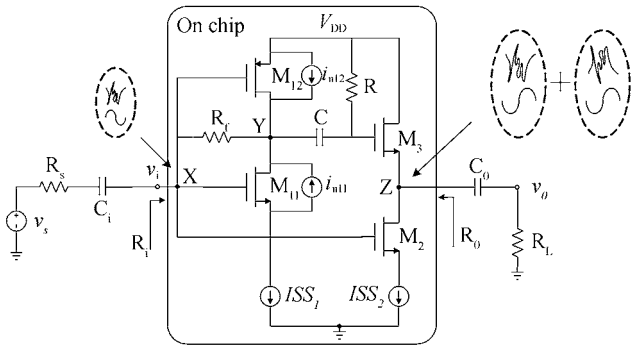

Fig. 3. Half part circuit schematic of the fixed-gain stage.

instantaneous voltages at nodes Y and X with the same phase. Then the noise voltage at node X($v_{X,n}$) is amplified by another common source MOSFET M2. The noise voltage at node Y($v_{Y,n}$) is followed by a source follower MOSFET M3. Two noise voltages are added together at node Z. Because of the opposite phase, two noise voltages $v_{X,n}$ and $v_{Y,n}$ will be cancelled by properly choosing the parameters of the MOSFET M2 and M3. On the other hand, the RF signals at node Z are added together with the same phase. Detailed analysis is presented as follows.

The input and output impedance can be calculated as

$$R_i \approx 1/g_{m1},\ R_o \approx 1/g_{m2}, \quad (2)$$

where the g_{m1} is equal to $g_{m11} + g_{m22}$ due to the current-reuse structure. With the input and output load impedance equaling to 50 Ω, the impedance matching condition is

$$g_{m1} = g_{m3} = 1/R_s. \quad (3)$$

The gain of M2 and M3 can be given by

$$A_{v,M_2} \approx -g_{m2}\left(R_L \| 1/g_{m3}\right) = -g_{m2}R_s/2, \quad (4)$$

$$A_{v,M_3} \approx g_{m3}R_L/\left(1 + g_{m3}R_L\right) = 1/2. \quad (5)$$

The output noise voltage due to the noise of the matching device, $v_{o,n}$ is then equal to

$$v_{o,n} = v_{X,n}A_{v,M_2} + v_{Y,n}A_{v,M_3} = i_{n_1}\left[R_s\left(-g_{m2}R_s/2\right) + \left(R_s + R_f\right)/2\right], \quad (6)$$

where $i_{n1} = i_{n11} + i_{n22}$. Upon noise cancellation $v_{o,n} = 0$, the noise-canceling condition can be calculated as

$$g_{m2} = \left(1 + \left(R_f/R_s\right)\right)/R_s. \quad (7)$$

Equation (8) shows that the channel thermal noise and flicker noise of first input matching stage can be easily cancelled by properly choosing g_{m2} of the second stage of the amplifier. The input impedance matching and the noise can be easily decoupled by this technology. The gain of the half circuit based on Fig. 3 becomes

$$A_v = v_{o,s}/v_{i,s} = -R_f/R_s. \quad (8)$$

The noise figure of the LNA in Fig. 3 can be written as

$$\mathrm{NF} = 1 + \frac{\overline{v_{o,n,M_1}^2} + \overline{v_{o,n,R_f}^2} + \overline{v_{o,n,M_2}^2} + \overline{v_{o,n,M_3}^2} + \overline{v_{o,n,R_L}^2}}{A_v^2 \times 4kTR_s}, \quad (9)$$

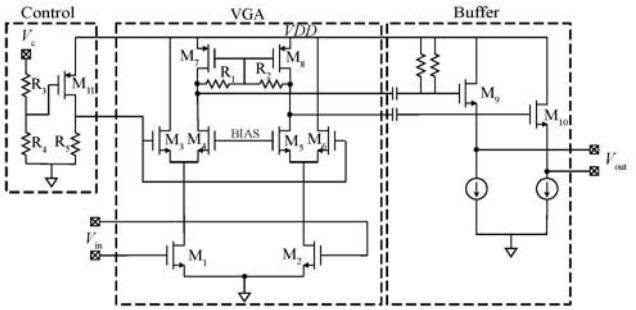

Fig. 4. Circuit schematic of variable-gain stage.

where $\overline{v_{\mathrm{o,n}}^2}$ is used to quantify the output noise of different device, where the index of $\overline{v_{\mathrm{o,n}}^2}$ refers to the contribution of each device. Upon noise cancellation, Equation (9) can be rewritten as

$$\begin{aligned}
&\overline{v_{\mathrm{o,n,M_1}}^2} = 0,\\
&\overline{v_{\mathrm{o,n},R_\mathrm{f}}^2} = 4kTR_\mathrm{f},\\
&\overline{v_{\mathrm{o,n,M_2}}^2} = (4kT\gamma g_{\mathrm{m_2}} + K/4f)\,R_\mathrm{o}^2 = kT\gamma\,(R_\mathrm{s}+R_\mathrm{f}) + KR_\mathrm{s}^2/4f,\\
&\overline{v_{\mathrm{o,n,M_3}}^2} = (4kT\gamma g_{\mathrm{m_3}} + K/4f)\,R_\mathrm{o}^2 = kT\gamma R_\mathrm{s} + KR_\mathrm{s}^2/4f,\\
&\overline{v_{\mathrm{o,n},R_\mathrm{L}}^2} = 4kTR_\mathrm{L}.
\end{aligned} \tag{10}$$

Replaced the terms in Eq. (9) by the expressions in Eq. (10), Equation (9) becomes

$$\mathrm{NF} = 1 + \frac{R_\mathrm{s}}{R_\mathrm{f}} + \left(\frac{R_\mathrm{s}}{R_\mathrm{f}}\right)^2 + \frac{\gamma}{4}\frac{R_\mathrm{s}}{R_\mathrm{f}}\left(\frac{2R_\mathrm{s}}{R_\mathrm{f}}+1\right) + \frac{KR_\mathrm{s}^3}{8kTR_\mathrm{f}^2 f}. \tag{11}$$

In Eq. (11), the parameter R_s and R_f are used to quantify the source load impedance and the feedback resistance. The parameter γ is noise parameter of transistors. For a deep-submicron MOSFET, the value of γ is usually between 1 and 3. K is an experiential parameter. Equation (11) shows that the noise figure at cancellation is mainly determined by the feedback resistance R_f. Thus, NF can be easily designed much lower than 3 dB by increasing the feedback resistance R_f.

3.2. Variable-gain stage and control stage

Signal-summing topology has been widely used in low-power and high-frequency VGA design[8]. Figure 4 shows the circuit schematic of the proposed signal-summing variable-gain stage with exponential gain control. Compared with the previous work in Ref. [8], the proposed variable-gain stage used PMOS transistors M7 and M8 as a load instead of a resistor, resistors R_1 and R_2 are used as a common-mode feedback circuit, and the tail current source is eliminated to enhance the linearity of VGA in low voltage supply process. With the same linear-in-dB gain characteristics on the control voltage, the output voltage swing is larger than the design in Ref. [8], especially at the low-gain mode when the input signal is a large signal. The reason is that the DC equivalent resistance of PMOS load in proposed VGA is large than the resistor in Ref. [8], while the AC small-signal equivalent resistance maintains the same. The DC voltage at the drain of the PMOS M7 and M8 is around 1.3 V in low-gain mode, while the DC voltage of resistor load in Ref. [8] is 1.7 V. So, the total harmonic distortion in proposed VGA is much smaller than the previous signal-summing VGA design.

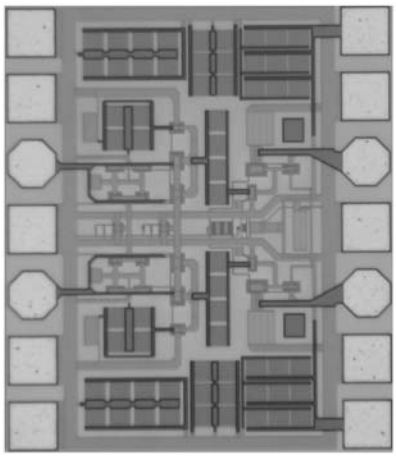

Fig. 5. Micrograph of variable-gain amplifier.

The exponential gain control circuit is shown in Fig. 4. The PMOS transistor M11 works in linear region and in common-source configurations. By combining the variable-gain stage and the exponential gain control circuit, the logarithmic current gain of the circuit becomes linear along with the control voltage as follows[8]:

$$\mathrm{Gain_I\,(dB)} = 10\lg K_1 + 10C\lg e + 10K_2\lg eV_\mathrm{c}, \tag{12}$$

where the K_1 and K_2 can be written as

$$K_1 = \frac{W_3}{W_4\,(V_{\mathrm{GS4}} - V_{\mathrm{TH4}})},\quad K_2 = \frac{R_4R_5}{R_3+R_4}\mu_P C_{\mathrm{ox}}\frac{W_{11}}{L_{11}}. \tag{13}$$

4. Measurement results

The VGA was fabricated in the SMIC's 0.18 μm RF CMOS process. A micrograph of VGA is shown in Fig. 5. The die size is 0.6×0.7 mm^2. The chip was measured in the test laboratory of the Institute of RF- & OE-ICs, Southeast University. The standard PGSGSGP probes for differential input and output were added to perform an on-wafer measurement. The major test equipments include Cascade probe station, Agilent network analyzer E5071B and spectrum analyzer E4440A. The VGA characteristics were measured through on-chip buffer circuits.

Figure 6(a) shows the measured S_{21} of VGA with the control voltage from 0.2 to 1.6 V in 0.2 dB step. This VGA operates up to 700 MHz, the DC blocking capacitors for connecting the two cascaded stages of the signal-summing VGA cause gain reduction at lower IF frequency. Figure 6(b) shows the linear-in-dB characteristics at 35, 300, and 600 MHz. The linear-in-dB variable-gain range is from –10 to 18 dB. The measured NF both at high-gain mode and low-gain mode is shown in Fig. 7. The minimum NF is 3.1 dB at 250 MHz. In the desired frequency band for IF VGA of DRM/DAB tuner, the NF is lower than 10 dB. The rising of NF at low frequency

Table 1. Summary of measured results.

Temperature (°C)		27
Supply Voltage (V)		1.8
Current Consumption (mA)		7 (core) + 8 (buffer)
Frequency (MHz)		25–700
Control voltage range (V)		0.2–1.6
Linear-in-dB gain range (dB)		−10 to18
NF (dB) @ 50 Ω	At maximum gain	3.1–10.7 @ 30–700 MHz
	At minimum gain	7.7–20.2 @ 30–700 MHz
Input-referred 1 dB gain compression point (dBm)	At maximum gain	−17.8 @ 35 MHz
	At minimum gain	–3.9 @ 35 MHz

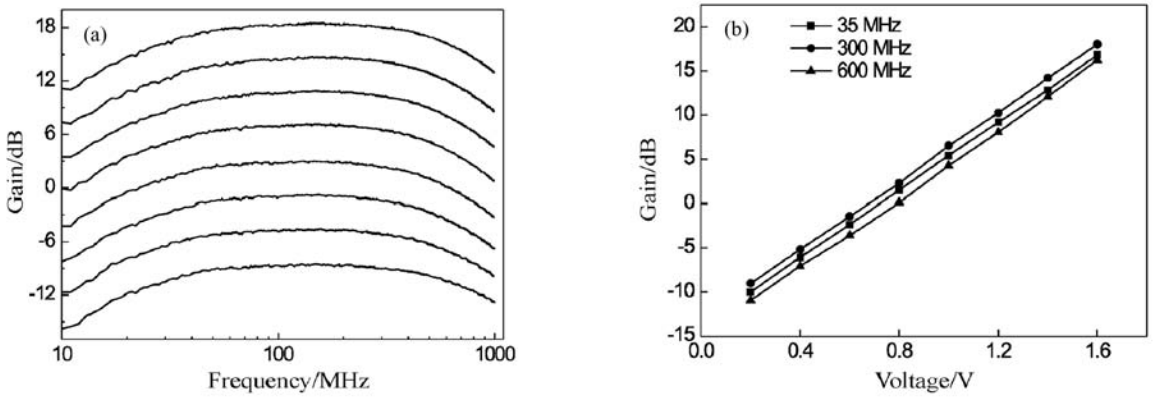

Fig. 6. Measured S_{21} versus (a) control voltage and (b) linear-in-dB characteristics.

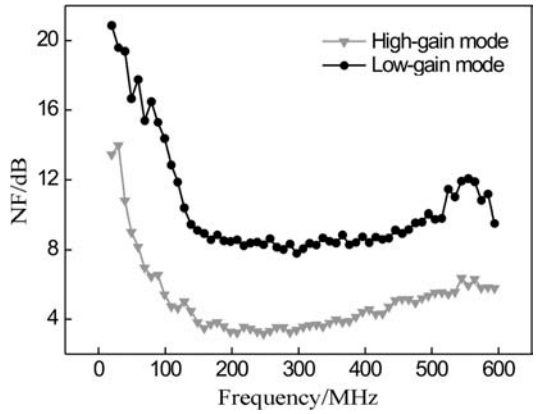

Fig. 7. Measured NF at high-gain mode and low-gain mode.

is due to the $1/f$ noise of transistors. The measured results are summarized in Table 1.

Compared with the VGA circuits reported in previous papers, some key parameters are better. In Ref. [6], the NF is 5 dB with the bandwidth around 500 MHz. In Ref. [8], the NF is 6.2 dB at maximum gain, while the P_{1dB} is –9 dBm. The linear-in-dB gain range is only 12 dB. In Ref. [13], the NF is 8.7 dB with the bandwidth around 100 MHz.

5. Conclusions

A new low-noise linear-in-dB intermediate frequency variable-gain amplifier for DRM/DAB tuner is demonstrated. The VGA comprises two cascaded stages of the first noise-canceling stage and the second signal-summing stage. A PMOS transistor in linear region serves as exponential gain control. This chip is fabricated with the SMIC 0.18 μm 1P6M RF CMOS process. The measured results show that this chip is suitable for the tuner in DRM/DAB communication systems.

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