A voltage-controlled ring oscillator using InP full enhancement-mode HEMT logic

Du Rui(杜睿)†, Dai Yang(戴杨), Chen Yanling(陈燕凌), and Yang Fuhua(杨富华)

(Research Center of Semiconductor Integration, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)

Abstract: A voltage-controlled ring oscillator (VCO) based on a full enhancement-mode InAlAs/InGaAs/InP high electron mobility transistor (HEMT) logic is proposed. An enhancement-mode HEMT (E-HEMT) is fabricated, whose threshold is demonstrated to be 10 mV. The model of the E-HEMT is established and used in the SPICE simulation of the VCO. The result proves that the full E-HEMT logic technology can be applied to the VCO. And compared with the HEMT DCFL technology, the complexity of our fabrication process is reduced and the reliability is improved.

Key words: VCO; E-HEMT; InP
DOI: 10.1088/1674-4926/30/3/035001 **EEACC:** 2570

1. Introduction

With extremely high gain, ultra-low noise figure and immunity from body effects, the InP-based HEMT has definite predominance in ultra-high-speed and low-noise applications. Utilizing the E-HEMT technology, a single-rail can be used instead of a dual-rail for the power supply, and the level-shift buffer between the stages can be dismissed. So the research of the high performance E-HEMT is attracting a lot of attention. An E-HEMT with an Ir/Ti/Pt/Au gate whose transition frequency is 151 GHz has been reported[1]. However, due to the complicated manufacturing process to integrate both enhancement-mode and depletion-mode HEMTs in the vertical direction, the direct coupled FET logic (DCFL) circuit, which is most widely used in compound semiconductor LSI, always fails to yield high enough for a large scale production.

In this paper, an E-HEMT is designed and fabricated for the full enhancement-mode HEMT logic[2]. Pt is still used as the Schottky contact metal in the gate fabrication but the gate anneal process is removed to avoid the reliability problems caused by the high diffusivity of Pt in InAlAs. Compared with the diode-connected E-HEMT load, the complex load used in the full enhancement-mode HEMT logic brings about larger output swing. And compared with all the DCFL configurations, the full enhancement-mode HEMT logic is insensitive to the variance of the threshold in the process, which is beneficial to suppress the phase noise in the oscillation circuit. According to the modeling of the device, a voltage-controlled ring oscillator is proposed and verified by SPICE simulation. Compared with the LC VCO which has low phase noise but large chip area, the proposed VCO avoids the using of spiral inductors. Using the EBL to obtain smaller gate length of HEMT, the proposed VCO is expected to operate in the millimeter wave band and to have satisfying noise performances.

2. E-HEMT design and fabrication

The conduction band structure of a planar-doped HEMT is shown in Fig. 1, where n_d is the concentration of the planar doping and $\Delta E_F = qV_G$, V_G is the voltage drop across the gate Schottky junction. As can be seen in Fig. 1, Poisson's equation can be solved to obtain the threshold voltage[3]:

$$V_T = \Phi_m - \frac{\Delta E_c}{q} + \frac{E_{F0}}{q} - \frac{qn_d(d-d_i)}{\varepsilon_2}, \quad (1)$$

where ε_2 is the dielectric constant of the InAlAs layer.

The derivation process is based on the hypothesis that the 2DEG fully concentrates on the interface between InAlAs and InGaAs layer. However, the hypothesis is not exact, the error of which can be corrected in the charge control equation[4].

As can be inferred from Eq. (1), three parameters can be adjusted to obtain an enhancement working mode: (1) Φ_m (the barrier height of the schottky junction): A high barrier height metal/InAlAs system is preferred. According to Table 1[5], Pt/InAlAs system has a relatively high barrier height and

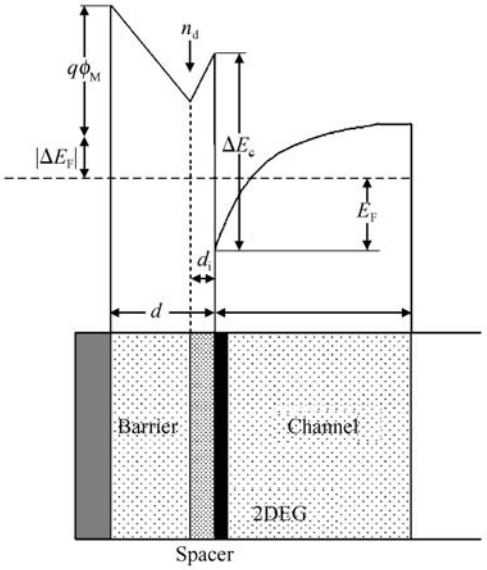

Fig. 1. Band structure of a planar-doped HEMT.

Table 1. Schottky barrier heights of InAIAs/metal contacts.

Material	Pt	Pd	Cr	Ti	Al
Barrier height (eV)	0.82	0.73	0.60	0.59	0.67

† Corresponding author. Email: ddrr@semi.ac.cn
Received 8 September 2008, revised manuscript received 23 October 2008

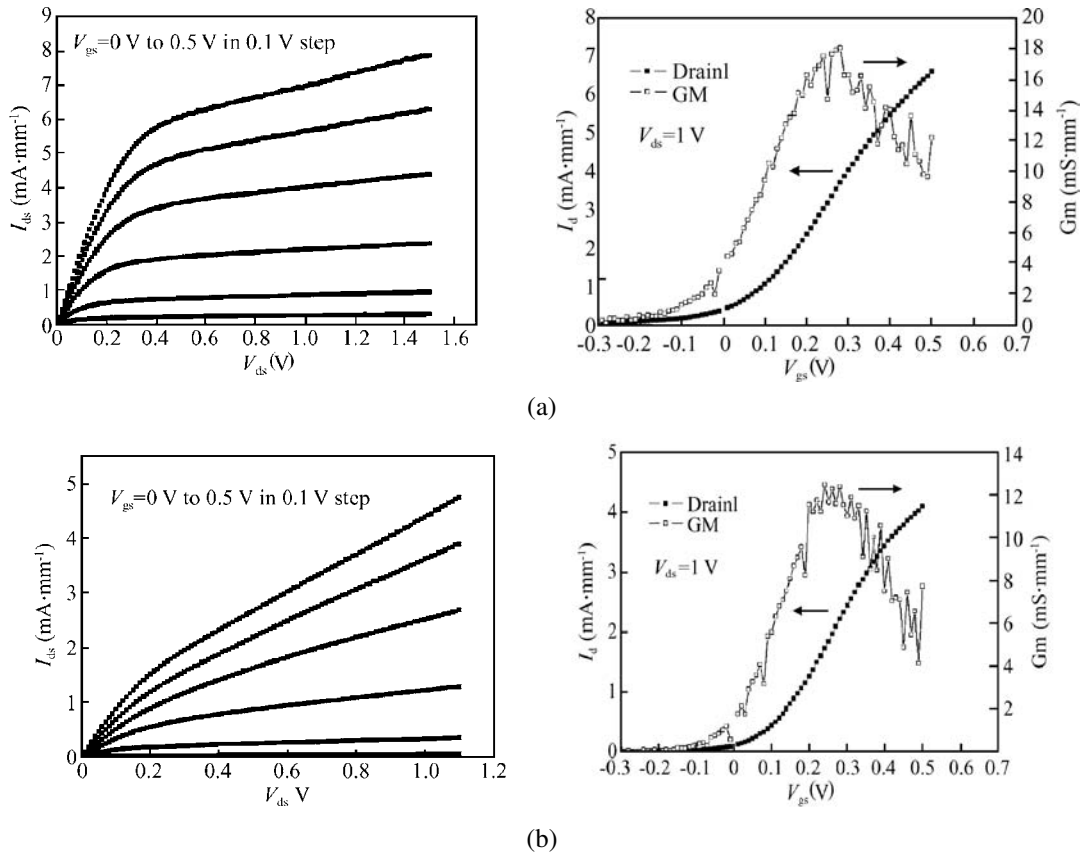

Fig. 2. (a) DC performance of the proposed HEMT(barrier layer = 7 nm); (b) DC performance of the proposed HEMT(barrier layer = 6 nm).

a regular rectifying property. (2) $d - d_i$ (the thickness of the InAlAs barrier layer): A reasonable small value is preferred. (3) n_d (the doping concentration): A reasonable low value is preferred. InAlAs/InGaAs/InP HEMT structures with different thicknesses of barrier layer are grown on InP substrates by molecular beam epitaxy for the experiment. The heterostructure on InP substrates consists of a 250 nm $In_{0.52}Al_{0.48}As$ buffer, a 15 nm $In_{0.53}Ga_{0.47}As$ channel, a 3 nm $In_{0.52}Al_{0.48}As$ spacer, Si atomic planar doping with a concentration of 2×10^{12} cm^{-2}, an InAlAs barrier layer, a 2 nm AlAs etch stop layer, and a 50 nm n$^+$-InGaAs cap layer doped to 1×10^{19} cm^{-3}.

For the device fabrication, isolation is achieved by mesa etching in a vitriol/hydrogen peroxide solution. Alloyed Ni/Ge/Au (10/50/80 nm) ohmic contacts are then formed. After that the gate recess etching is performed using succinic acid /ammonia/hydrogen peroxide solution. The etching rate for $In_{0.53}Ga_{0.47}As$ is more than 1000 times of that for AlAs[6]. So this etching process is of good controllability. Finally, Pt/Ti/Pt/Au (5/15/10/100 nm) is evaporated for the gate metallization. The gate width of all the devices is 1×40 μm.

The DC performance of the HEMT with a barrier-layer thickness of 7 nm is illustrated in Fig. 2(a) and the DC performance of the HEMT with a barrier-layer thickness of 6 nm is illustrated in Fig. 2(b). Figure 2 shows that the working mode of HEMT changes from depletion-mode to enhancement-mode when the barrier-layer thickness is changed from 7 to 6 nm. Figure 2 also shows the transconductance suppression which characterizes the saturation of the 2DEG. With the aid of Fig. 1 again, a voltage V_C can be obtained as shown in Eq. (2)[3]. When $V_G > V_C$, the electron Fermi level nearly touches the conduction-band minimum in the InAlAs layer and the transfer of electrons into the V-shaped quantum well in this layer becomes dominant, sharply reducing the device transconductance.

$$V_C = \Phi_m + \frac{an_{s0}}{q} - \frac{\Delta E_c}{q} + \frac{E_{F0}}{q} - \frac{qn_d(d-d_i)}{\varepsilon_2} + \frac{qn_{s0}d}{\varepsilon_2}, \quad (2)$$

where n_{s0} is the saturation sheet density of the 2DEG.

For the E-HEMT shown in Fig. 2(b), enhancement-mode characteristics of V_T of 10 mV with I_d of 4.5 μA and the gate leaking current of 0.5 μA are realized, while V_{ds} is 1 V.

Compared with the conventional methods which control the thickness of the barrier layer either by the wet etching or by the gate annealing, the reliability of our method is improved.

3. Inverter and VCO design

The conventional DCFL configurations and the full enhancement-mode HEMT logic configurations are shown in Fig. 3.

In order to avoid the expensive process to fabricate a metal-film resistor in MMIC, a diode-connected load is always used and operates as a small-signal resistor. Both the diode-connected D-HEMT load (D-load) and the diode-connected E-HEMT load (E-load) have an equivalent small-signal resistance of $1/g_m$. But in a DCFL circuit, an equivalent DC resistance is always necessary to be considered. The $I-V$ character

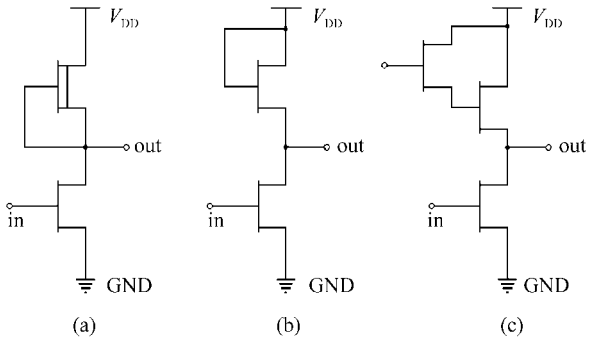

Fig. 3. Circuit configuration of (a, b) DCFL and (c) full enhancement-mode HEMT logic.

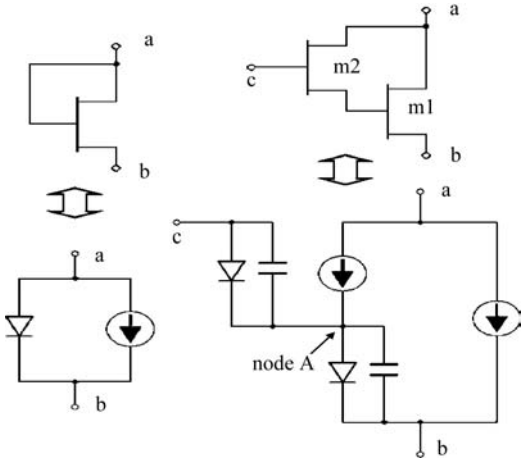

Fig. 4. Equivalent circuit for the E-load and the complex load.

of a D-load using Curtice–Quadratic[7] model is

$$I_{ds} = \beta V_T^2(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}). \quad (3)$$

The I–V character of an E-load is

$$I_{ds} = \beta(V_{ds} - V_T)^2(1 + \lambda V_{ds}) \tanh(\alpha V_{ds}). \quad (4)$$

From Eqs.(3) and (4), we can conclude that the equivalent DC resistance of D-load is increasing with the rising of the voltage through it, where E-load the opposite. So D-load always provides a larger DC equivalent resistance. When the diode-connected load is introduced to the inverter circuit, the D-load one provides a larger output swing than the E-load one does, hence the noise margin of both the high voltage level and the low voltage level can be better.

As mentioned above, the current in an E-load is increasing rapidly when the voltage is rising, the reason of which can be easily explained using the equivalent circuit. The schematic of the E-load and the complex load used in the full enhancement-mode HEMT logic gate is shown in Fig. 4. With the gate and the drain being short connected, the equivalent circuit can be constructed in which a Schottky diode is connected in shunt with a controlled source. So when the Schottky diode is positive onset, the total current will still be increasing even when the channel current reaches the maximum value.

For the complex load, a possible range of reference voltage is given by[2]

$$2V_T + V_{OH} < V_{ref} < V_{OL} + 2V_B, \quad (5)$$

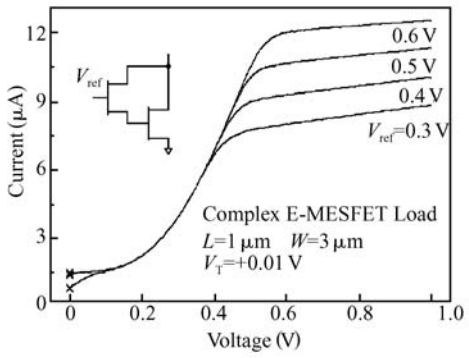

Fig. 5. DC character of the complex load.

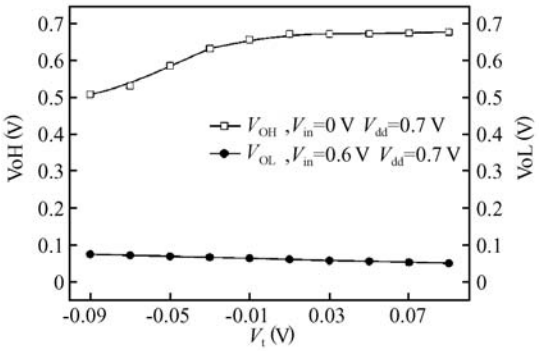

Fig. 6. Relation between noise margin and threshold.

where V_B ($\approx$ 0.6–0.7 V) is the voltage drop across an open Schottky diode, V_T is the threshold voltage of the E-HEMT, V_{OH} is the high output voltage, and V_{OL} is the low output voltage.

As can be inferred from Eq. (5), for a right V_{ref}, it is obvious that the two Schottky diodes in series cannot be turned on simultaneously even when the output is low; the total current flowing in the complex load will nearly maintain the maximum value of I_{ds}. The DC character of the complex load is shown in Fig. 5. Compared with the DCFL configuration using E-load, with the lower current at the low output logic level, the noise margin of the full enhancement-mode HEMT logic gate is definitely improved.

Furthermore, as the output voltage is changed from low to high, since V_{gs} through gate-source capacitance do not have a sudden change, it causes an increase in the voltage at node A above the value of V_{DD} (the bootstrap effect). As a result, the gate-source voltage of the E-HEMT m1 is higher than the DC value, the larger charge current bring on a shorter rise time.

In addition, in a D-load inverter, the output voltage always increases with the threshold, which depraves the noise margin of the low voltage. But for a full enhancement-mode HEMT logic, the noise margin is mainly determined by the ratio of the load transistor's W/L to the driving transistor's. The equivalent resistance of both the driving transistor and the complex load increases with the threshold, which makes the noise margin of the inverter relatively insensitive to the varying of the threshold, especially in the region where V_T is positive (Fig. 6).

When the inverter is used to construct a ring oscillator, the low-frequency gain of the inverter must satisfy the Barkhausen's law, which is always more strict than the self-

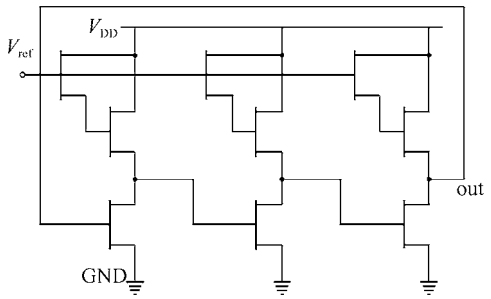

Fig. 7. A 3-stage ring oscillator circuit.

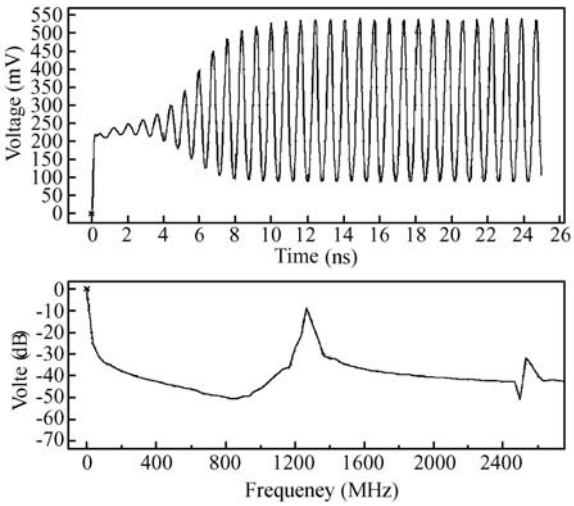

Fig. 8. Simulated waveform and the spectrum of the oscillator.

restoring character ($A_0 > 1$ in transition region, $A_0 < 1$ in stable region). For an N-stage ring oscillator, according to the Barkhausen's law, the loop should induce an AC phase shift of 180 °, supposing the stages are just identical and the phase shift induced by a single stage should be 180 °/N. Assuming there is only one pole in a single stage, the oscillating frequency should be

$$\omega_{\rm osc} = \tan(\frac{180^\circ}{N})\omega_0, \tag{6}$$

where ω_0 is the 3 dB band width. According to the Barkhausen's law we also have

$$A_0 \geqslant \sqrt{1+\left(\frac{\omega_{\rm osc}}{\omega_0}\right)^2}, \tag{7}$$

where A_0 is the DC gain of a single stage. So the minimum A_0 is decreasing when N is growing bigger. In order to make a 3-stage oscillator, we have $A_0 \geqslant 2$[8].

If m1 and m2 are identical in Fig. 4, we can infer that the small-signal equivalent resistance of a complex load should approximately equal $2/g_{\rm m}$, which is twice of an E-load one and good enough for making the single stage to satisfy the Barkhausen's law.

The topology of a 3-stage ring oscillator is shown in Fig. 7. The signal will feed back from the output of the third inverter to the input of the first inverter.

According to the Leeson model[9] which assumes the oscillator as an LTI system and also the definition of the open-loop quality factor Q of the ring oscillator which is based on a small-signal analysis[10], the phase noise can be expressed as

$$L(\Delta\omega) = 10\lg\left[\frac{4NFkRT}{V_{\rm osc}^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right], \tag{8}$$

where $V_{\rm osc}$ is the swing of the oscillator output, and R is the total load impedance. So increasing the output swing is an effective method to reduce the phase noise. As mentioned above, for a fixed load, the swing of the oscillator is mainly determined by the ratio of the load transistor's W/L to the driving transistor's, but not by $V_{\rm T}$. So $V_{\rm T}$ has little influence on the phase noise.

According to the Hajimiri model[11] based on an LTV analysis method, in an single-ended ring oscillator, the phase noise has no relation to the stage number; the phase noise can be minimized by improving the switching speed of the inverter, the symmetry in the layout design and the consistency of the process.

As proved in the analysis above, the choice of $V_{\rm ref}$ directly affects the value of small signal equivalent resistance of a complex load $R_{\rm D}$. At the same time, the choice of $V_{\rm ref}$ has indirect influence on the value of $g_{\rm m}$ by altering the DC operation point. Considering $A_0 \approx g_{\rm m}R_{\rm D} \geqslant 2$, the valid range of $V_{\rm ref}$ is not so wide.

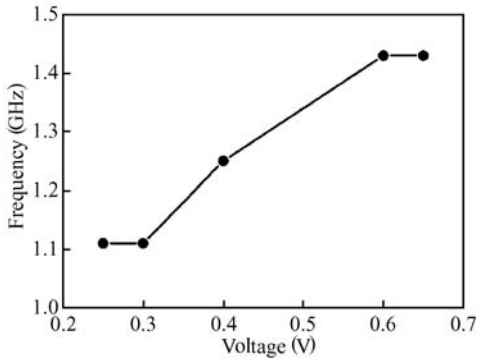

Fig. 9. Tuning characteristic of the VCO.

4. Simulation results

A Curtice cubic MESFET model with a symmetric capacitance hypothesis[12], whose parameters are extracted from an E-HEMT we fabricated, is used for the simulation: the gate width is 10 μm for the drive transistors and 3 μm for the transistors in the complex load, $V_{\rm DD}$ is 0.75 V. Three inverter stages are identical and assumed to have the same parasitic capacitance at the output nodes.

Using the parameters above, Figure 8 shows the simulated output waveform under a 0.45 V reference voltage and its spectrum. With adjustable $V_{\rm ref}$, the tuning characteristic of the VCO is shown in Fig. 9.

By the simulation of harmonic balance, it can be found that the phase noise is insensitive to the varying of the threshold when $V_{\rm T} > 0$ (Fig. 10). So the proposed circuit configuration does not require a large positive threshold.

Through the simulation, the fact that the E-HEMT fabricated by us can be used in the ring oscillator is proved.

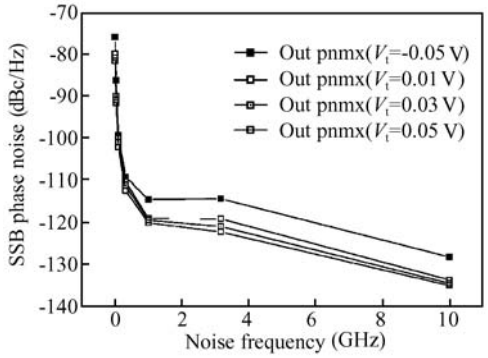

Fig. 10. Single-side-band phase noise under different threshold.

5. Conclusions

We have designed a voltage-controlled oscillator (VCO) based on a full enhancement-mode HEMT logic. As the reference voltage in the complex load directly serves as the control signal, compared with the traditional voltage-controlled ring oscillator, the complexity of circuit is simplified. Moreover, due to that the full enhancement-mode HEMT logic is introduced to the circuit, the process complexity decreases; also since that the AlAs stop layer technology is used in device fabrications, the controllability is improved. Finally the yield of the whole chip will be better for a large scale production.

References

[1] Kim S, Adesida I. 0.15-μm-gate InAlAs/InGaAs/InP E-HEMTs utilizing Ir/Ti/Pt/Au gate structure. IEEE Electron Device Lett, 2006, 27(11): 873

[2] Bushehri E, Thiede A, Bratov V, et al. Design and evaluation of a novel enhancement mode FET logic gate configuration in AlGaAs/GaAs/AlGaAs quantum well HEMT technology. IEE Proc Circuits, Devices and Systems, 1997, 144(4): 243

[3] Wang G, Eastman L F. An analytical model for *I–V* and small-signal characteristics of planar-doped HEMT's. IEEE Trans Microw Theory Tech, 1989, 37(9): 1395

[4] Lee K, Shur M S, Drummond T J, et al. Current–voltage and capacitance–voltage characteristics of modulation-doped field-effect transistors. IEEE Trans Electron Devices, 1983, 30(3): 207

[5] Harada N, Kuroda S, Katakami T, et al. Pt-based gate enhancement-mode InAlAs/InGaAs HEMTs for large-scale integration. Third International Conference on Indium Phosphide and Related Materials, 1991, 8–11: 377

[6] Broekaert T P E, Fonstad C G. AlAs etch stop layers for InGaAlAs/InP heterostructure devices and circuits. IEEE Trans Electron Devices, 1992, 39(3): 533

[7] Curtice W R. A MESFET model for use in the design of GaAs integrated circuits. IEEE Trans Microw Theory Tech, 1980, 28(5): 448

[8] Razavi B. Design of analog CMOS integrated circuit. New York: McGraw Hill, 2001

[9] Leeson D B. A simple model of feedback oscillator noises spectrum. Proc IEEE, 1966, 54(2): 329

[10] Razavi B. A study of phase noise in CMOS oscillators. IEEE J Solid-State Circuits, 1996, 31(3): 331

[11] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2): 179

[12] Statz H, Newman P, Smith I W, et al. GaAs FET device and circuit simulation in SPICE. IEEE Trans Electron Devices, 1987, 34(2): 160