System on chip thermal vacuum sensor based on standard CMOS process*

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Abstract: An on-chip microelectromechanical system was fabricated in a 0.5 μm standard CMOS process for gas pressure detection. The sensor was based on a micro-hotplate (MHP) and had been integrated with a rail to rail operational amplifier and an 8-bit successive approximation register (SAR) A/D converter. A tungsten resistor was manufactured on the MHP as the sensing element, and the sacrificial layer of the sensor was made from polysilicon and etched by surface-micromachining technology. The operational amplifier was configured to make the sensor operate in constant current mode. A digital bit stream was provided as the system output. The measurement results demonstrate that the gas pressure sensitive range of the vacuum sensor extends from 1 to 10^5 Pa. In the gas pressure range from 1 to 100 Pa, the sensitivity of the sensor is 0.23 mV/ Pa, the linearity is 4.95%, and the hysteresis is 8.69%. The operational amplifier can drive 200 Ω resistors distortionlessly, and the SAR A/D converter achieves a resolution of 7.4 bit with 100 kHz sample rate. The performance of the operational amplifier and the SAR A/D converter meets the requirements of the sensor system.

Key words: micro-hotplate; thermal vacuum sensor; monolithic; operational amplifier; SAR ADC
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1. Introduction

Thermal vacuum sensors are widely used in the fields of metal-smelting, food processing, thin film preparation and electronic packaging to detect gas pressure from 10^{-1} to 10^5 Pa. The monolithically integrated sensor system with embedded interface circuits has attracted more attention due to the advantages of high precision, fast response speed, small size, low power consumption, strong anti-interference ability and reduced assembly and packaging cost[1−3]. Many researches on the integrated thermal vacuum sensor system have been performed. Among them, Haberli fabricated a CMOS thermal pressure sensor system integrating a biasing circuit and a readout circuit[4]; Klaassen reported a vacuum sensor with an area of a single crystal silicon membrane suspended by silicon dioxide beams, which was integrated with a two-stage operational amplifier and a digital to analog converter (DAC) to form a constant temperature control system[5].

In this paper, a thermal vacuum sensor system integrating a rail to rail operational amplifier and a SAR A/D converter in the same substrate is designed. The CMOS compatible sensor is based on MHP and surface-micromachining technology. The sacrificial layer is manufactured from polysilicon and etched in post-IC process. A tungsten resistor is designed as the sensing element. The operational amplifier is configured to make the sensor work in constant current mode. Then the voltage signal is converted into a digital bit stream by the SAR A/D converter.

2. Sensing element design

The MHP has been extensively adopted in thermal vacuum sensors due to the benefits of fast response time, high thermal efficiency and easily integrated with standard CMOS process. In this work, an MHP with the area of 40 × 40 μm^2 is supported by four cantilever beams of 30 μm length and 15 μm width. The heater and thermometer on the MHP is made from a tungsten resistor of 0.8 μm width that is entwined in an s-shape to obtain a uniform temperature distribution. The tungsten resistor is about 230 Ω at room temperature and has a high temperature coefficient of 0.0015 Ω / °C. The tungsten layer is an interface layer between the first metal layer and the second metal layer in the CMOS process but is specially designed as a resistor here in order to make use of its high temperature coefficient and good thermal stability. The sacrificial layer is made from the second polysilicon layer, which is 0.34 μm thick and determines the upper limit of the gas pressure measurement range. The top view and the cross-section view of the MHP are shown in Fig. 1.

The ambient gas pressure variation changes the gas thermal conductivity, and the heating power consumed by the MHP in gas conduction varies. The temperature of the MHP working in constant current mode varies correspondingly, which leads to the alteration of the tungsten resistor. So the gas pressure can be measured by detecting the voltage across the tungsten resistor.

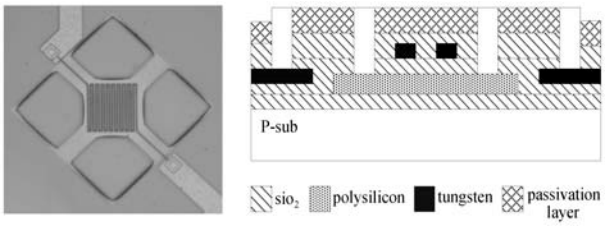

Fig. 1. Structure and cross-section view of the MHP.

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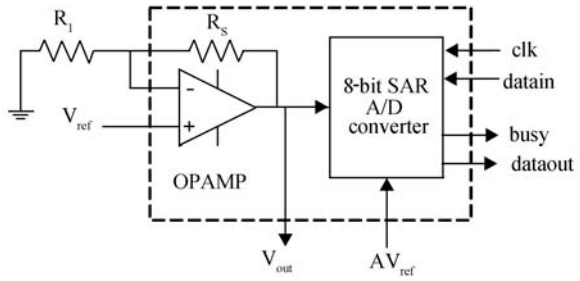

Fig. 2. Block schematic diagram of the vacuum sensor system.

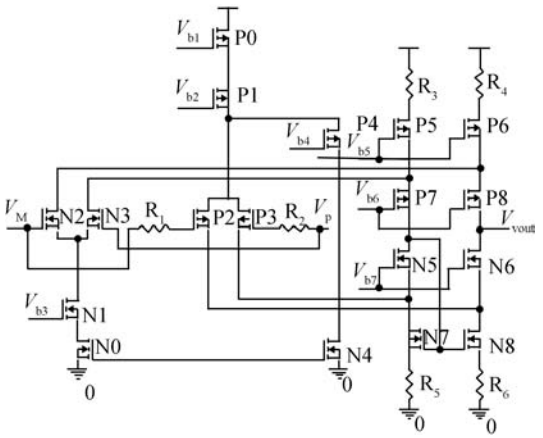

Fig. 3. Rail to rail input stage of the operational amplifier.

3. System design

The block schematic diagram of the vacuum sensor system is shown in Fig. 2. A robust digital bit stream is exported, which represents the ambient gas pressure and can transmit in a noisy environment without any loss in the resolution. The non-inverting input terminal of the operational amplifier connects to 1.25 V DC reference voltage, while the inverting input terminal links to two resistors in series connection. The resistor R_1 is set to generate 7 mA current in the branch of R_1 and R_s to make the sensor work in constant current mode.

The sensor system requires a rail to rail operational amplifier. The output current of the operational amplifier needs to be greater than 10 mA to drive 200 Ω resistor distortionlessly. The required performance of the SAR A/D converter is as follows: (1) The supply is 5 V. (2) The resolution is 8 bit. (3) The input voltage range is 2–5 V. (4) The sampling frequency is 100 kHz. (5) Low power consumption.

3.1. Operational amplifier design

The operational amplifier is designed with rail to rail input and output ranges. The input stage employs a couple of complementary differential pairs to achieve a rail to rail common mode voltage range. To obtain an optimal frequency compensation and avoid distortion, the constant G_m input stage is preferred[6, 7]. It is known that the transconductance is proportional to the current when the transistor works in weak inversion region. The sum of the tail currents of n-pair and p-pair is kept constant to make the combined transconductance stable. The input stage circuit is shown in Fig. 3. The variation of G_m is controlled within 10%, as shown in Fig. 4.

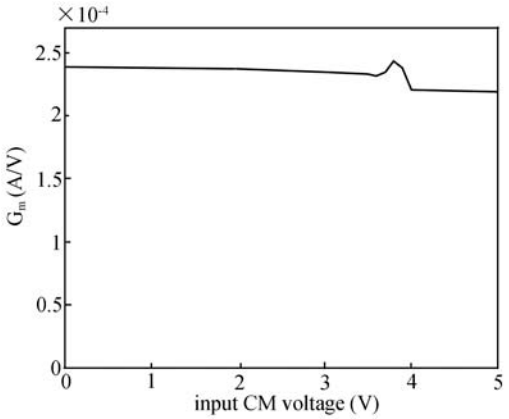

Fig. 4. G_m variation with the input voltage.

Table 1. Performance of the class AB operational amplifier.

Feature	Performance
Supply	5 V
Process	0.5 μm CMOS
Open-loop gain	132 dB
Phase margin	66 °
GBW	3.5 MHz
SR	2.5 V/μs
Input transconductance	Constant (ΔG_{mmax} = 10%)
Input stage swing	rail to rail
Output stage swing	0.2 V to V_{dd} − 0.2 V
CMRR	107 dB @ 1 kHz
PSRR	97 dB @ 1 kHz
THD	–81 dB@ (0.9 Vpp, 1 kHz)

A complementary class AB controlled common source output stage was realized for low quiescent power consumption[8]. The performance of class AB operational amplifier is summarized in Table 1.

3.2. SAR A/D converter design

SAR A/D converter has the advantage of lower power and smaller area[9] over other converters. The output has only a clock period delay relative to the input signal. The power consumption is not a fixed value but decreases with the slowdown of the sampling frequency. This is beneficial to the application where the data need not be acquired continuously. So, SAR A/D converter is an attractive choice for this sensor system.

The SAR A/D converter comprises four main sections: sampling/holding circuit, successive approximation register circuit, D/A converter and logic control circuit. The diagram of SAR A/D converter is shown in Fig. 5. The precision of the comparator determines the resolution of the ADC. The offset cancellation technique based on output offset storage was adopted in the design of the comparator[10]. The SAR A/D converter works in three phases. First, the A/D converter works in the sampling phase. The switch S4 connects to V_{out}, and the switchs S1, S2, S3 are on. The output signal of the operational amplifier, V_{out}, is sampled and stored on the capacitor C_1. The two input terminals of the preamplifier connect to V_{out} simultaneously, and the offset voltage of the preamplifier is stored on the capacitor C_2 and C_3. After three clock periods for the

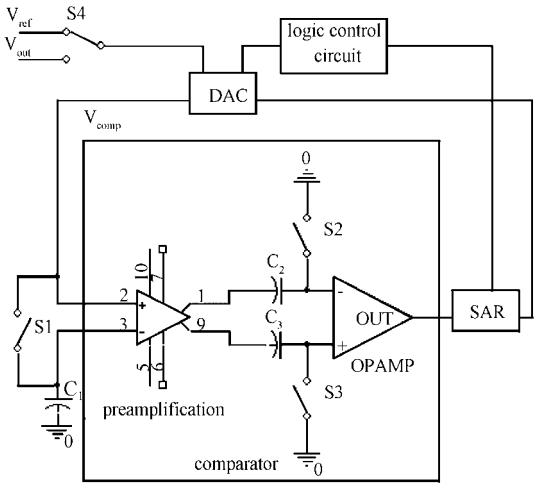

Fig. 5. Diagram of SAR A/D converter.

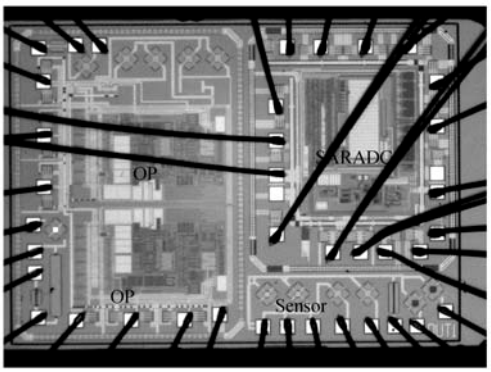

Fig. 6. System on chip thermal vacuum sensor.

holding phase, the switch S4 connects to $V_{\rm ref}$, and the switch S1, S2, S3 are off. The A/D converter begins to work in the successive comparison phase. The logic control circuit generates the initial digital codes which are converted into an analog voltage to compare with $V_{\rm out}$. The SAR circuit computes next digital codes according to the result of the comparator until all the 8 bit digital output codes are completed. To decrease the power consumption, the comparator enters the low power mode after a conversion. When next conversion begins, the comparator returns the work mode.

Charge scaling DAC was adopted in the SAR A/D converter. The precision of the DAC depends on the noise and the mismatch between the capacitors in the array. Thermal noise is the main random process error source[11]. The edge effect and the fluctuation of oxide thickness and dielectric constant are two major factors contributing to the mismatch. The capacitors were manufactured by the parallel of unit capacitors and arranged in common-centroid floorplan to minimize the ratio error and the gradient error. The upper plates of the capacitors were connected together as the common terminal to weaken the effects of parasitic capacitance in the input terminal of the comparator. A guard ring around the capacitor array was applied to isolate the capacitor array from the peripheral switch circuits. The smaller capacitors were placed near their corresponding switch circuits to decrease the interconnect capacitance. The capacitors in the DAC were fabricated with the gate polysilicon layer and the second polysilicon layer.

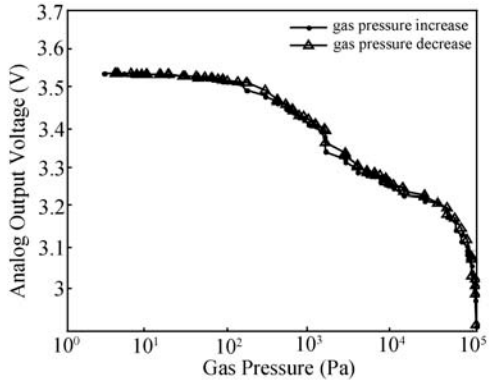

Fig. 7. Measurement results of output voltage versus gas pressure.

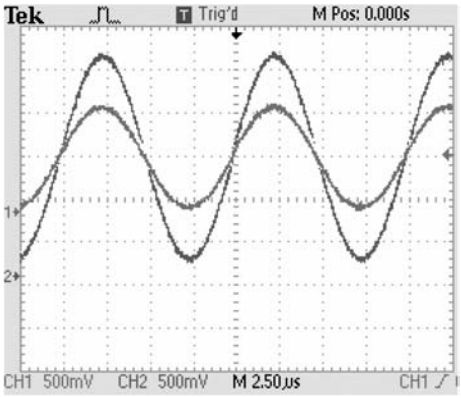

Fig. 8. Measurement results of the operational amplifier.

4. Measurements and results

The vacuum sensor system was fabricated by post-IC process. First, the sensor system was manufactured in a standard 0.5 μm CMOS process. Then the sacrificial layer was etched in a tetramethyl ammonium hydroxide (TMAH) solution to free the MHP from the silicon substrate. To prevent the bare silicon surface from being etched, an additional aluminum layer was deposited in the backside of the die. The system on chip thermal vacuum sensor is shown in Fig. 6.

The sensor test system includes a vacuum chamber, a mechanical pump and a diffusion pump. The packaged sensor chip was fixed on the work platform in the vacuum chamber. The gas pressure in the vacuum chamber was controlled by the mechanical pump and the diffusion pump to change from 1to 10^5 Pa. The output voltage of the operational amplifier versus the gas pressure is shown in Fig. 7. The higher the gas pressure is, the lower the temperature is in the MHP. So, the thermal resistor on the MHP reduces, which leads to the decrease of the output voltage. As shown in Fig .7, the sensitivity of the sensor is 0.23 mV/Pa, the linearity is 4.95%, and the hysteresis is 8.69% in the gas pressure range from 1 to 100 Pa.

The operational amplifier and the SAR A/D converter are packaged by individual pads and can be tested respectively.

4.1. Operational amplifier test

The operational amplifier was configured into a noninverting proportional amplifier circuit to test its drive capability. The closed loop gain is 2, and the connected resistors are

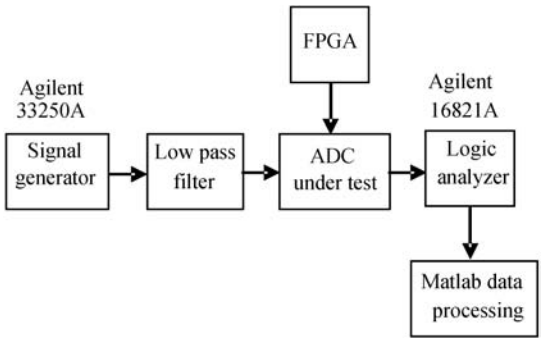

Fig. 9. Block diagram of the ADC test system.

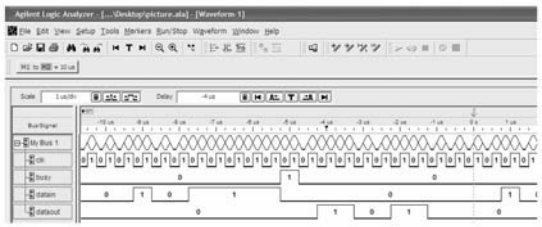

Fig. 10. Measured timing sequence diagram of the SAR ADC.

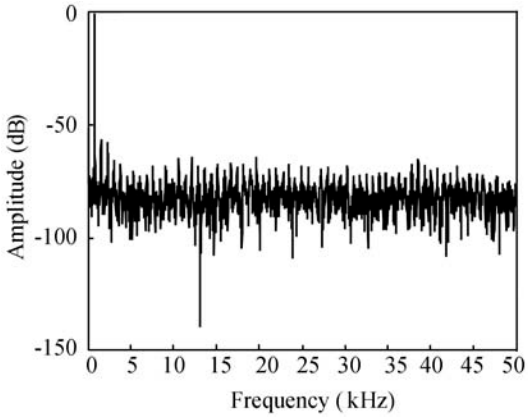

Fig. 11. Frequency spectrum of the SAR ADC.

200 Ω. As shown in Fig. 8, the input sinusoidal signal with the frequency of 100 kHz is amplified distortionlessly.

4.2. SAR A/D converter test

The test system of the SAR A/D converter is shown in Fig. 9. The signal generator provided the sinusoidal signal. A low pass filter was inserted between the signal generator and the ADC under test to eliminate the interference of FPGA (field programmable gate array) to the system. The FPGA generated the clk and the datain signal, and the busy and the dout signal of the ADC were collected by the logic analyzer. Then the data were sent to Matlab program to calculate the parameters such as SNR (signal-to-noise ratio), DNL (differential non-linearity) and INL (integral non-linearity)[12]. The timing sequence diagram is shown in Fig. 10. The clock frequency is 2 MHz. The datain is an enable signal, and the rising edge of datain means that the input signal will be sampled. After the high level of the busy signal, the digital signal corresponding to the analog input voltage begins to export. The dout is the serial data output signal, first the higher bits, then the lower bits.

An integer number of signal periods are sampled for the spectrum analysis. Based on the coherent sampling principle, the formula

$$M/N = F_{\text{in}}/F_{\text{s}}$$

needs to be satisfied, where M is the number of signal periods, N is the number of samples, F_{in} is the signal frequency, and F_{s} is the sampling frequency. In this test, F_{s} is 100 kHz, and F_{in} is 757 Hz. 31 signal periods are sampled to obtain 4096 data for fast Fourier transform (FFT). The FFT frequency spectrum is shown in Fig. 11. The significant bit is 7.4, which meets the design requirement.

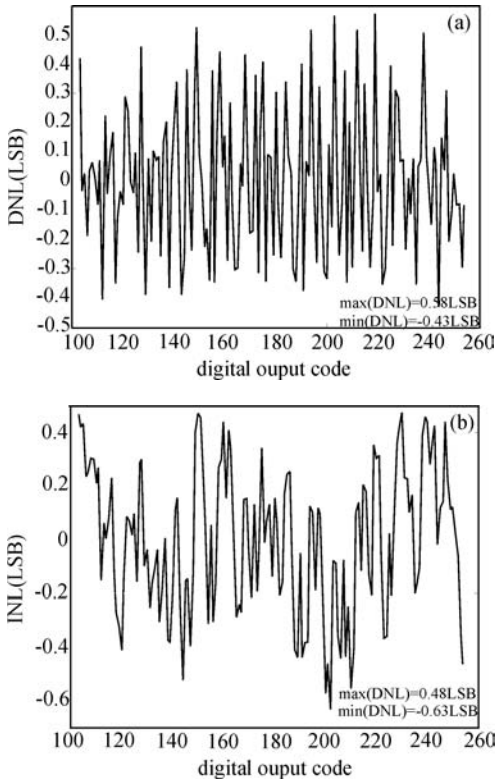

Fig. 12. Measured linearity of the SAR ADC: (a) DNL characteristic; (b) INL characteristic.

Histogram test[13] was used to determine the linearity (DNL and INL) of the A/D converter. Like FFT test, an integer number of periods are sampled. To attain a high confidence measurement, a quite large data length is required. Owing to the limit of the logic analyzer, 49152 data were sampled. The measurement results of DNL and INL are shown in Fig. 12. Because the output signal of the operational amplifier is greater than 2 V, only the signal between 2 and 5 V is processed by the A/D converter for simpler circuit and less layout area. The maximum of DNL and INL are 0.58 LSB (least significant bit) and 0.63 LSB respectively, which are higher than the designed 0.5 LSB. There are two reasons for the higher DNL and INL: one is the less samples due to the capability of the logic analyzer, and the other is the effects of the capacitor mismatch in the DAC circuit.

5. Conclusions

A fully integrated vacuum sensor system with a rail to rail operational amplifier and an 8-bit successive approximation register A/D converter is proposed. The sensor system

was based on the MHP and was fabricated in a standard 0.5 μm CMOS process on the same substrate. The tungsten resistor was designed as thermal sensing element and entwined in s-shaped to obtain uniform temperature distribution. The sacrificial layer was realized by polysilicon, which was etched in post-IC process using surface-micromachining technology. The operational amplifier was configured to make the sensor work in constant current mode. The output voltage of the operational amplifier can be controlled by adjusting the resistor off the chip. A robust digital signal was provided as system output, which was representative of the absolute gas pressure and was immune to the noise. The gas pressure sensitivity range of the sensor extends from 1 to 10^5 Pa. In the gas pressure range from 1 to 100 Pa, the sensitivity of the sensor is 0.23 mV/Pa, the linearity is 4.95%, and the hysteresis is 8.69%.The operational amplifier can drive 200 Ω resistors distortionlessly. The SAR A/D converter achieves a resolution of 7.4 bits with 100 kHz sampling frequency. The measurement results demonstrate that the performance of the operational amplifier and the SAR A/D converter meets the requirements of the sensor system.

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