A 434/868 MHz CMOS low-IF receiver with I/Q imbalance calibration for SRDs application

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Abstract: A receiver for SRDs implemented by the 0.35 μm CMOS process is presented. The receiver, together with the ADC, power amplifier (PA), frequency synthesizer and digital baseband has been integrated into a single chip solution. Low cost and low power requirements are met by optimizing the receiver architecture and circuit topology. A simple mixed-signal mode I/Q imbalance calibration circuit is proposed to enhance the IRR (image rejection ratio) so as to raise the BER. From a single 3 V power supply, the receiver consumes 5.9 mA. The measurement result shows that the receiver achieves reference sensitivity of –60 dBm and a control gain of 60 dB. The S_{11} reaches –20 dB at 433 MHz and –10 dB at 868 MHz without off-chip impedance match network. The die area is only 2 mm^2 including the bias circuit.

Key words: short range device; low-power; low-cost; receiver; I/Q imbalance calibration
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1. Introduction

Wireless communication has grown rapidly. Bluetooth, wireless LAN (WLAN) and ultra wideband (UWB) are known for their high data rate communication for the short range. However, they are complex, power consuming and expensive. Consequently, it is inappropriate for some simple short range devices (SRDs) applications such as telemetry and wireless remote keyless entry. Most of these applications only require relatively low data rare from 0.3 to 128 kb/s and a bit-error rate of 1%[1]. In addition, they share the common requirement of a low-cost, low-power, and small form-factor transceiver.

This paper focuses on the implementation of a low-cost low-power receiver. Design considerations including operating frequency, modulation scheme, and system and circuit topology are taken to meet the cost and power requirements. The system architecture and circuit topology are discussed in detail.

It is generally known that the higher the operating frequency, the more power is required to achieve the desired performance. However, considering the antenna size and channel selectivity, it is hard to lower the frequencies below 300 MHz. As a result, an SRD band at 433 and 868 MHz is used as a compromise.

For the sake of power consumption and complexity, amplitude shift keying (ASK), frequency shift keying (BFSK) and Gauss frequency shift keying (GFSK) are selected as modulation schemes for SRD applications though they are not the most specially efficient nor do they have the lowest SNR requirements[2].

Obviously, GaAs or bipolar technology has demonstrated its excellent performance in low-noise, high-gain, and high-output power. However, from the standpoint of low cost, high integration and good compatibility with digital baseband, CMOS is more attractive. Many research studies have demonstrated that the CMOS submicron process can realize reasonable performance in RF circuits[3, 4].

The low-cost receiver calls for minimization of the number of discrete external components. The use of the on-chip inductor is avoided as well, because it will take up large die area so as to raise the cost. Thus the above considerations affect the receiver architecture as well as circuit topology.

In this paper, a receiver that uses single-conversion low-IF architecture with a wideband low noise amplifier (LNA) and mixed-signal mode imbalance calibration is presented. It is implemented in the CMOS 0.35 μm process.

2. System level design considerations

Zero-IF[3] and low-IF[4, 5] are preferred over the superheterodyne architecture because the latter has the drawbacks of external component indispensable, high complexity, cost and power consumption. The zero-IF receiver down-converts the radio frequency directly to zero frequency. Consequently, it is not suitable for SDRs applications which operate at a narrow band because of its DC offset and flicker noise problems . The low-IF receiver does not suffer from the problem of DC-offset and flicker noise because it down-converts the RF frequency to intermediate frequency (IF). Figure 1 shows the block diagram of the proposed receiver that employs the low-IF architecture. The received RF signal is amplified by the first single-ended LNA and then is converted from single-ended to differential. Following SDC, there is the second-stage variable-gain amplifier to enlarge the dynamic range. The quadrature mixer down-converts the amplified signal with an on-chip clock to IF. The output frequency of PLL is 1.736 GHz. A digital signal can select 434 or 868 MHz clock to feed into the receiver by using

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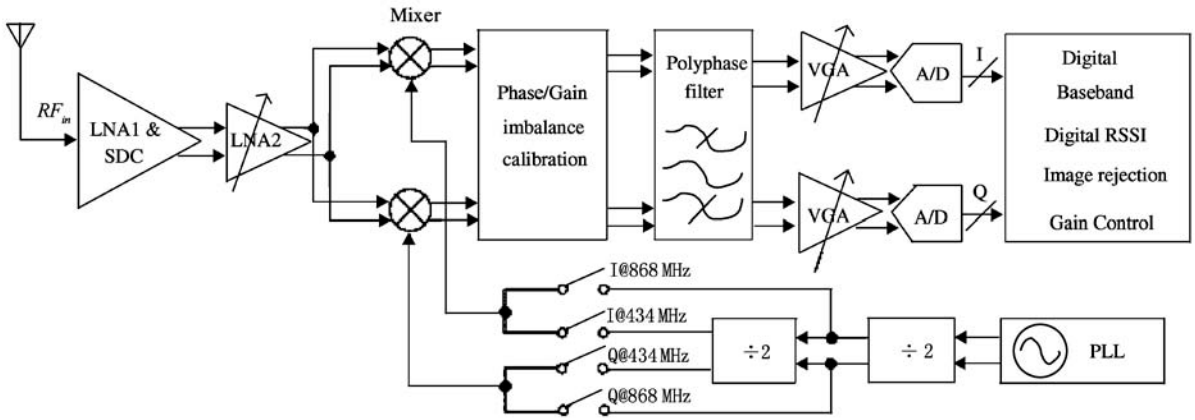

Fig. 1. Receiver block diagram.

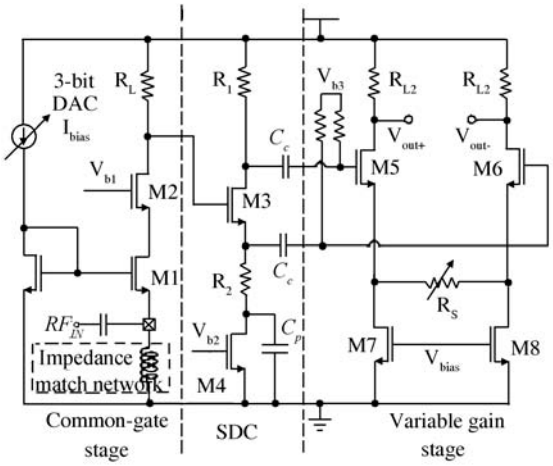

Fig. 2. Circuit of the wideband LNA.

two dividers. An IF-frequency of 300 kHz was selected based on a careful trade off among $1/f$ noise, LO phase noise, chip area and power consumption[5]. A polyphase filter is adopted to deal with the image problem inherent to the low-IF receiver[6]. Due to the reason that the amount of the image rejection is limited by gain and phase mismatches, an image and phase calibration block following the quadrature mixer is introduced. During calibration, I/Q imbalance is detected digitally and corrected in the analog domain. The calibrated signal is then filtered by four order Butterworth polyphase filter. Following that, VGA is adopted to keep almost constant signal level at the ADC input.

3. Circuit implementations

3.1. Two stage wideband variable gain LNA without off-chip match network

Figure 2 depicts the schematic of the wideband LNA. The signal level received by the receiver is always affected by the ambient circumstance. According to the Friss equation[7], LNA locating at the first stage of the receiver needs to provide minimum noise figure and adequate large gain when the received signal level is low for the overall noise performance of the receiver. However, an excessively large gain may overload the mixer and compromise the dynamic range. Consequently, a two-stage variable-gain LNA is adopted to realize the trade offs between noise figure and linearity.

Since the resistance looking into the source terminal is $1/g_{\mathrm{m}}$, a proper selection of device size and bias current can provide the desired 50 Ω resistance[8]. The transconductance is given by

$$g_{\mathrm{m}} = \sqrt{\mu_{\mathrm{n}} C_{\mathrm{ox}}\ (W/L)\, I}, \tag{1}$$

where W, L is the width and length of the transistor, respectively, and I is the bias current. By choosing the proper input transistor and bias current, the dual band match at 434 and 868 MHz can be achieved simultaneously without the help of off-chip matching network. In order to stabilize the impedance against variations in process, temperature, voltage (PVT) variations, the bias current is controlled by a 3-bit DAC. The cascade transistor is added to increase the output impedance and achieve high reverse isolation.

In a common gate amplifier, the load can be an inductor, resistor, and MOSFET. However, in order to reduce cost, inductor is not used for SRDs. MOSFET is noisier and more nonlinear than a poly resistor. Hence, the poly resistor is selected as the load.

The noise figure of a common gate amplifier with load resistor is

$$\begin{aligned} \mathrm{NF} &= 1 + \frac{\overline{V_{\mathrm{n,o}}^2}}{A_{\mathrm{V}}^2}\frac{1}{4kTR_{\mathrm{s}}} = 1 + \frac{(4kT\gamma g_{\mathrm{m}})R_{\mathrm{L}}^2 + 4kTR_{\mathrm{L}}}{(g_{\mathrm{m}}R_{\mathrm{L}})^2}\frac{1}{4kTR_{\mathrm{s}}} \\ &= 1 + \frac{\gamma}{g_{\mathrm{m}}R_{\mathrm{s}}} + \frac{1}{g_{\mathrm{m}}^2 R_{\mathrm{L}}R_{\mathrm{s}}}. \end{aligned} \tag{2}$$

If the input impedance is matched, then

$$\begin{aligned} \mathrm{NF} &= 1 + \gamma + \frac{1}{g_{\mathrm{m}}R_{\mathrm{L}}} \\ &= 1 + \gamma + \frac{1}{A}, \end{aligned} \tag{3}$$

where γ is the excess channel thermal noise coefficient, and A is the voltage gain. From the last term of Eq. (3), it is obvious that the noise figure is reverse to the gain. As a result, the first

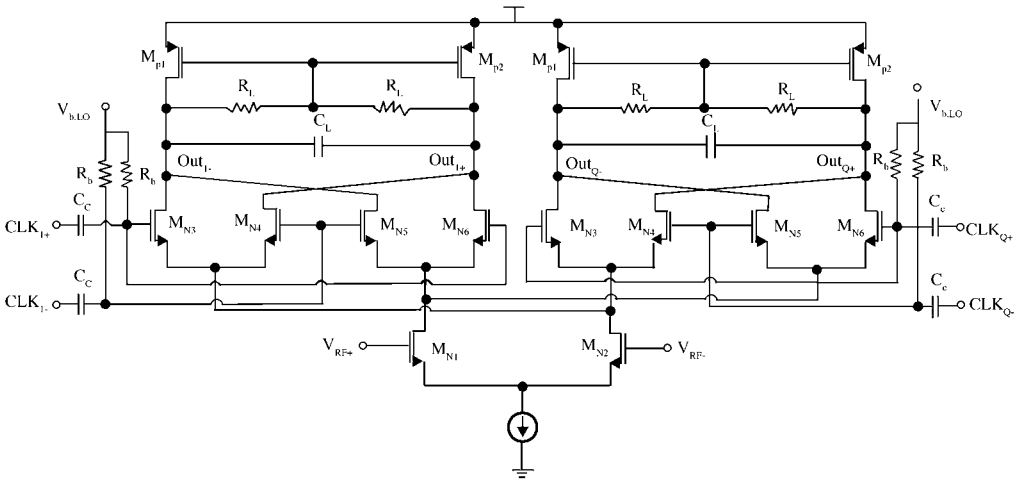

Fig. 3. Schematic of quadrature down-converter.

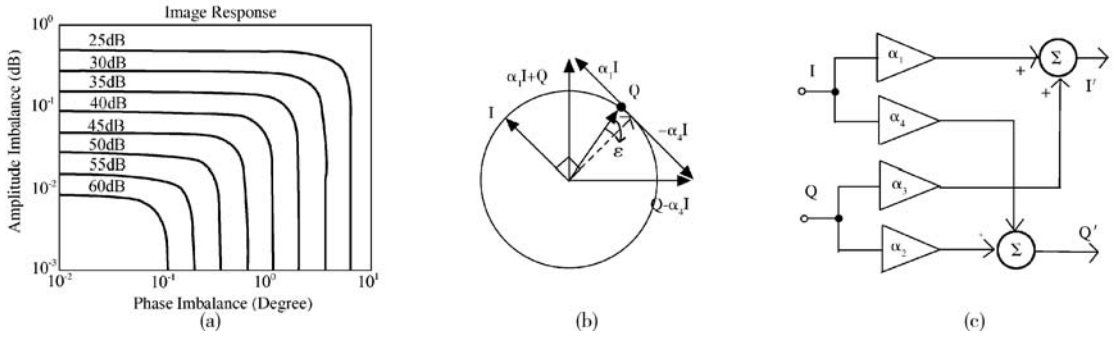

Fig. 4. Phase imbalance calibration structure: (a) Image responses versus amplitude and phase imbalance; (b) Special condition: β_1 and α_2 equals to one; (c) Practical implementation.

stage is designed with a fixed gain that is as large as possible. An off-chip grounded inductor also carriers the bias current.

To make the following circuit differential so as to reduce the common mode noise and clock feed-through to the LNA input, the circuits following the first-stage are implemented full differentially. As a result, a signal-ended to differential-ended converter (SDC) is inserted between the first stage and the second variable gain stage. It is a common-source amplifier with source degeneration to produce the differential output which can give higher linearity with low biasing current. The output of SDC is AC-coupled to the second stage of variable-gain LNA, which consists of a degenerate differential pair with resistive load. Degeneration improves the linearity of the amplifier and the resistor load alleviates the nonlinearity because of the MOSFET. The differential gain of this stage is given by

$$\text{Gain} = R_{\text{L2}}/R_{\text{S2}}, \tag{4}$$

where R_{S2} denotes half of the degeneration resistance. Therefore, the gain can be varied either by using a variable degeneration resistance or load resistance. However, it is preferably implemented using a variable degeneration resistor while maintaining a constant load resistor. Otherwise, the dominant pole at the output nodes is not constant and thus the bandwidth is independent on the gain. The programmable degeneration impedance results in a gain distribution ranging from 2 to 10 dB in 4 dB steps. The smaller the degenerated resistance, the higher the gain and the worse the linearity. However, as the increased gain is required only when the input signal swings are low, this decreased linearity has a negligible influence on the overall linearity performance. Polysilicon resistors are used so as not to degrade the linearity and noise performance.

3.2. Quadrature downconverter

The output of LNA is AC-coupled to the quadrature down-conversion mixer, shown in Fig. 3. It is based on a double-balanced Gilbert-type architecture with resistive loads that can provide better LO-intermediate (IF) and LO-RF isolations. The switch pairs share the same RF drive stage to reduce mismatches present in the conventional two separate I/Q mixers. Active loads are avoided at the output of the mixer to minimize flicker noise and improve the linearity. A low-pass load formed by the load resistor and the capacitor is used to filter out any undesirable high frequency content in the output signal.

3.3. I/Q mismatch calibration

A complex filter with unsystematic responses towards the positive and negative frequency response is adopted to attenuate the image signal and the folded-back strong interference after down-conversion[9]. However, the phase and amplitude mismatches at the input of the filter will limit the image rejection ratio (IRR) thus degrading the signal-to-noise ratio (SNR) and raising the BER. From Fig. 4(a) we find that IRR is only

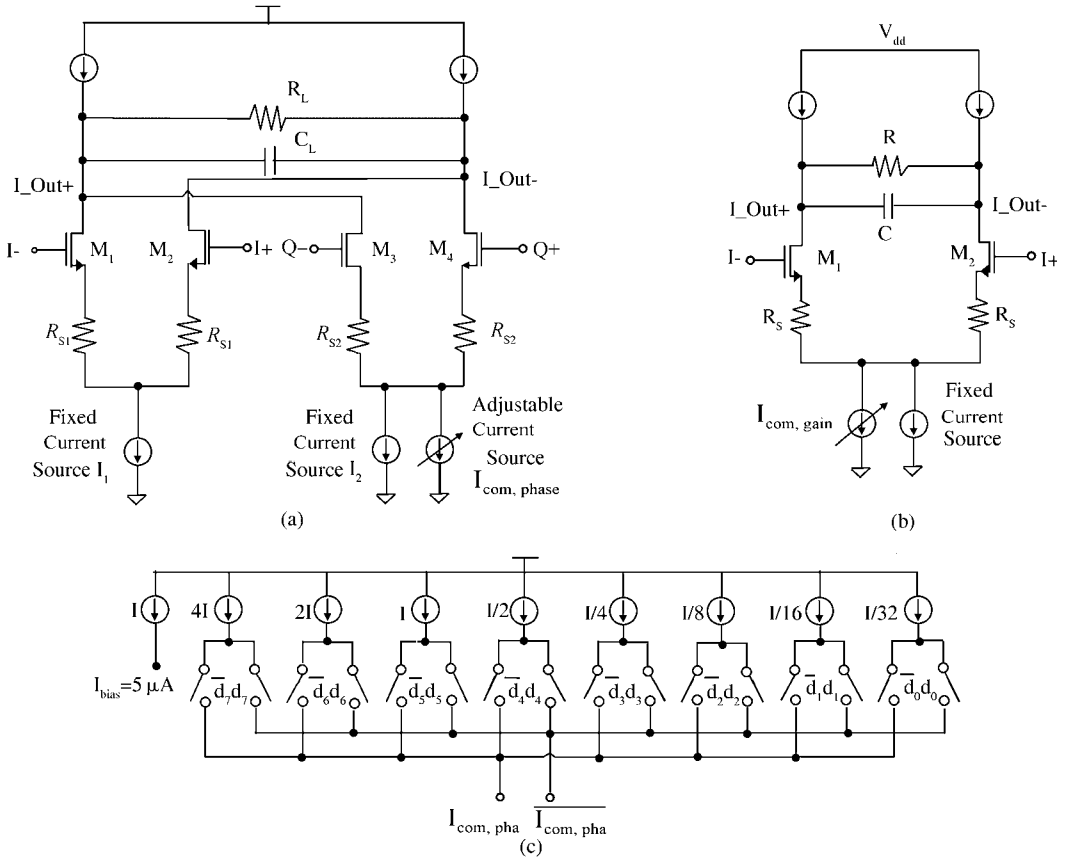

Fig. 5. (a) Schematic of phase imbalance compensation; (b) Schematic of gain imbalance compensation; (c) Current steering 8-bit DAC.

30 dB when the gain imbalance is 0.1 dB and the phase imbalance is 3.4 ° . Therefore, I/Q gain and phase imbalance calibration circuits in front of polyphase filter are exploited.

Without loss of generality, the down-converted signal with phase imbalance can be expressed as

$$I = \cos(\omega_{\mathrm{IF}} t), \quad Q = (1+\delta)\sin(\omega_{\mathrm{LO}} t + \varepsilon), \tag{5}$$

where ε denotes the phase imbalance between the I and Q paths and the amplitude is normalized to one. From Fig. 4 (a) we can find that the new vectors $\alpha_1 I + \alpha_3 Q$ and $\alpha_2 Q - \alpha_4 I$ could be orthogonal through the addition and subtraction of I and Q with proper coefficients. Figure 4(b) is the special case where both α_2 and α_3 are equal to 1. In practice, quadrature compensation is used, as shown in Fig. 4(c). On one hand, it increases the compensation speed and accuracy. On the other hand, it minimizes the systematic mismatches owing to the asymmetric loading of the two mixers.

The operation procedures are outlined as follows. In calibration mode, a signal at the image frequency ($2f_{\mathrm{IF}}$ below the desired channel) is applied at the RF input. Subsequently, the digital received signal strength indicator (RSSI), which is a logarithmic measure of the average voltage amplitude after the digital low-pass filter in the baseband, estimates the average received signal power. For perfect phase and gain match of the I and Q paths, the values in the digital RSSI register are zero. Correspondingly, the I and Q phase and gain difference can be fine-tuned by two 8-bit DACs for minimum RSSI value.

Figure 5(a) depicts the phase calibration circuit realization. For simplicity, only one branch of the circuit is presented and the structure of the other branch is the same. The differential input voltage signal is converted to a differential current through the transconductance of the two input transistors. Addition and subtraction are implemented by adding or subtracting currents. The channel of input transistors is set relatively long to improve matching and to reduce flicker noise. Degeneration architecture is used in order to get good linearity. The adjustable compensated current $I_{\mathrm{com,pha}}$ is mirrored from the 8-bit current mode differential DAC with the most significant bit as the symbol bit, which is shown in Fig. 5(c).

Figure 5(b) depicts the gain imbalance calibration circuit by changing the bias current controlled by 8-bit complementary DAC. The output current is converted from the input voltage with different weight factors. The DAC used in gain imbalance calibration circuit is the same as the one in the phase imbalance calibration circuit to decrease the design complexity. With a 5-μA reference current, the overall current consumed in the calibration circuit is less than 100 μA.

The calibration results of the phase and gain imbalances are shown in Figs. 6(a) and 6(b), respectively. The maximum compensable phase deviation is about ± 6 ° , and the phase mismatch after calibration can be compensated to a level below 0.08 ° . The maximum compensable gain deviation is about ±3 dB, and the gain deviation after calibration will be below 0.024 dB. From the plot in Fig. 4(a), we find that the IRR after calibration can reach 60 dB.

3.4. Polyphase filter

Polyphase filter can be divided into passive polyphase

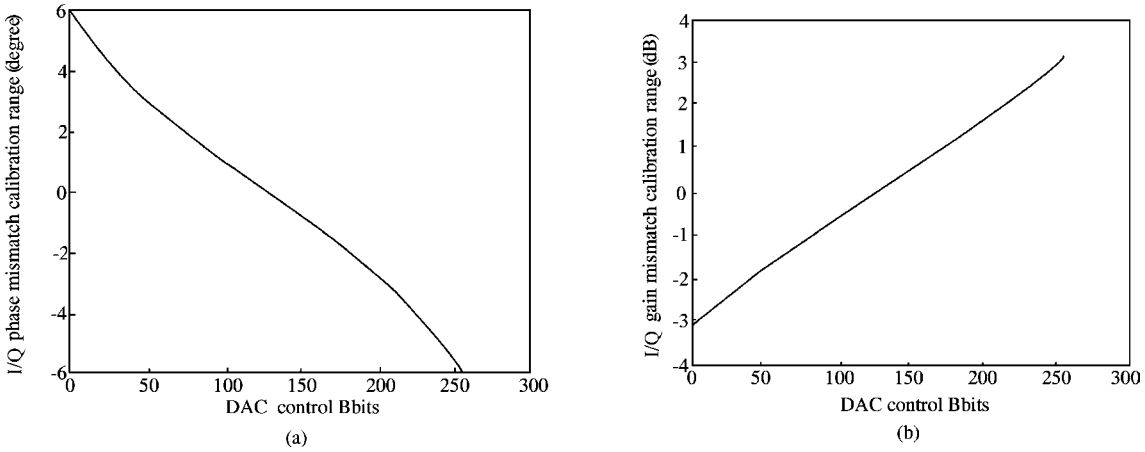

Fig. 6. (a) I/Q phase calibration range; (b) I/Q gain calibration range.

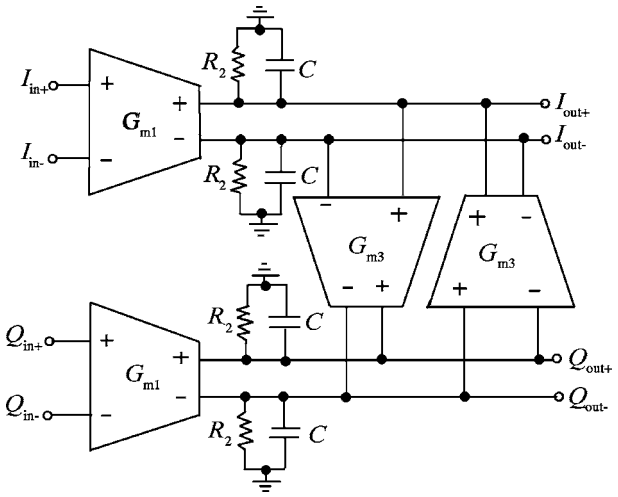

Fig. 7. Block diagram of one stage polyphase filter.

filters and active polyphase filters. As the passive polyphase filter is lossy, the signal-to-noise ratio (SNR) will be degraded when the signal passes through it. Though additional buffer can be used to compensate for the loss, more power is consumed. On the contrary, active polyphase filter have the advantages of low power dissipation, small chip area and high signal gain. Active filter consists of switch capacitor, g_m–C and active RC filters. Since OOK, FSK and GFSK modulation scheme do not place high requirement on in-band linearity, G_m–C filter is used for the sake of power saving though it is less linear than the another two. The Butterworth approximation is preferred because it has a small group delay variation within the passband. System simulation result shows that the four-order polyphase filter is adequate to meet the specification requirement. Figure 7 is the block diagram of one-stage polyphase filter. The transfer function of one-stage complex filter, $H(S)$ can be realized as

$$H(s) = \frac{V_{out(s)}}{V_{in}(s)} = \frac{G_{m1}}{sc + \dfrac{1}{R_2} - jG_{m3}} = \frac{A_V \omega_{LF}}{s + (\omega_{LF} - j\omega_{IF})}, \quad (6)$$

where $A_v = G_{m1}R_2$ is the midband voltage gain, $\omega_{LF} = 1/R_2C$ is the real part of the complex pole, and $\omega_{IF} = G_{m3}/C$ is the image part of the complex pole.

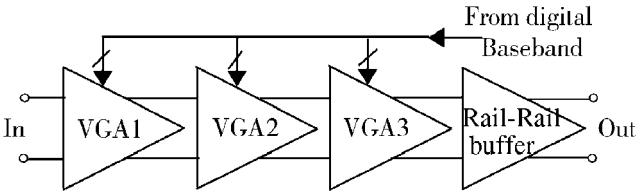

Fig. 8. Block diagram of VGA.

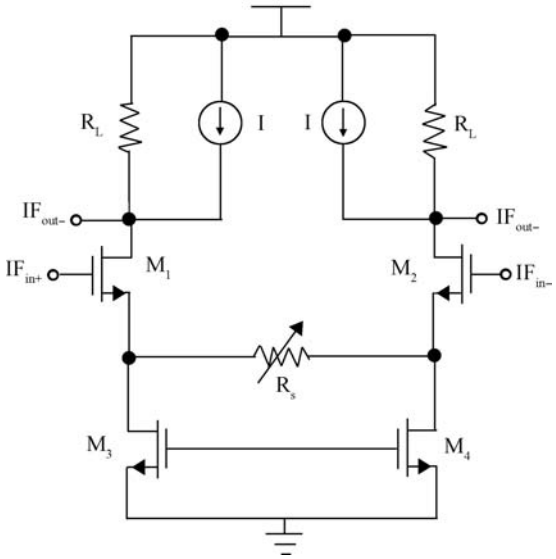

Fig. 9. Schematic of VGA.

3.5. VGA

The block diagram of VGA is shown in Fig. 8. It consists of three variable gain stages and an output rail-to-rail output buffer. The individual amplified range is from 6 to 24 dB, 6 dB per step. This distribution is chosen mainly to enhance the total noise performance of the VGA and enlarge the dynamic range of the receiver. According to the Friss equation, a large gain in the first stage will reduce the noise figure of the whole VGA. As a result, the total gain is set to the largest and decreases from the last stage to the front stage according to the signal level.

The detail schematic of the variable gain stage is outlined in Fig. 9. The voltage gain can be expressed by

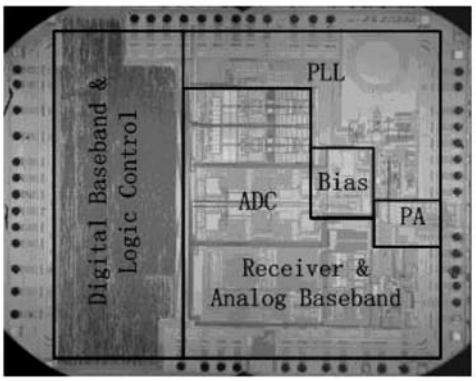

Fig. 10. Die photo.

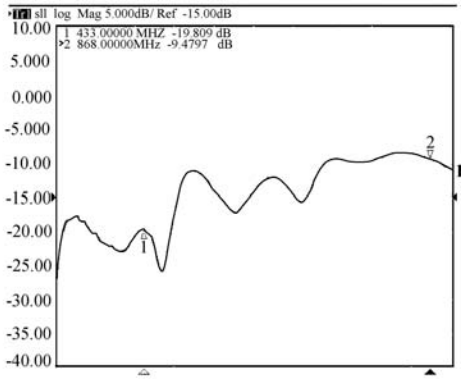

Fig. 11. Measured input returm loss of the receiver.

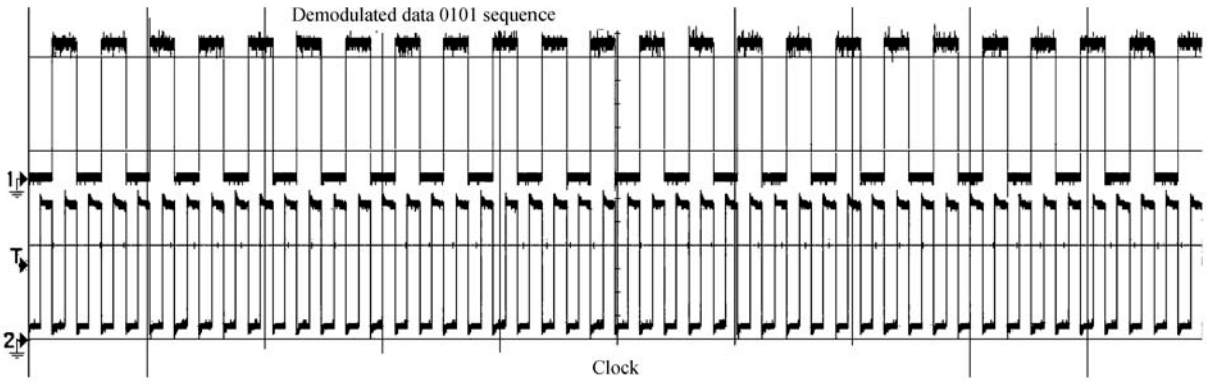

Fig. 12. Demodulated waveform at 4.8 kps data rate.

$$A_{\rm v} = G_{\rm m}R_{\rm L} = \frac{g_{\rm m}}{1 + g_{\rm m}R_{\rm s}}R_{\rm L} = \frac{R_{\rm L}}{R_{\rm s}}, \quad g_{\rm m} \gg 1. \tag{7}$$

By changing the degeneration resistance combined with load resistance, a different gain can be realized. The channel of input transistors is set relatively long to improve matching and to reduce flicker noise. Large resistive load for a fixed current will limit the available headroom. A current source load will degrade linearity and introduce noise. To maintain a compromise among gain, linearity and noise, a parallel combination of current source with resistor is used.

The input sampling capacitor of ADC that usually locates following VGA is always large. In order to enhance the driven ability and enlarge the dynamic range of the input signal, an input buffer using a complementary differential pair to achieve rail-to-rail operation is used. It is a compound structure that consists of NMOS and PMOS differential pairs connected in parallel.

4. Measurement results

This low-IF receiver has been fabricated in the 0.35 μm CMOS technology. Figure 10 shows the die photomicrograph of the integrated transceiver, in which the receiver takes up an area of 2 mm^2.

Figure 11 shows the input return loss (S_{11}) of the receiver sweeping the frequency across the entire band from 300 to 900 MHz. The S_{11} is –19.9 dB at 434 MHz and –9.6 dB at 868 MHz without the introduction of any impedance matching network.

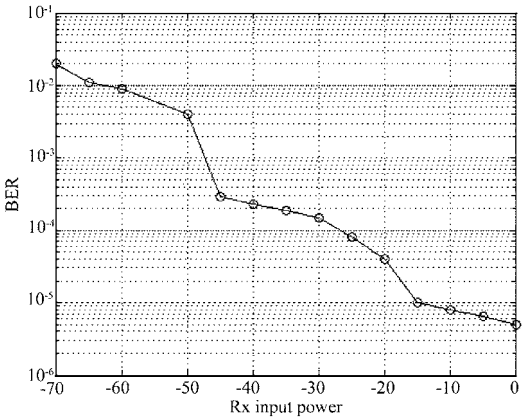

Fig. 13. BER versus input power.

As mentioned in Section 1, the receiver is fully integrated with PLL, PA, and digital baseband. As a result, some performances such as noise figure (NF) and linearity cannot be measured by the pin constraint. However, these performances can be reflected from the demodulated signal and the BER. The measured demodulated output waveform and the clock signal were displayed by the oscilloscope, as shown in Fig. 12. FSK modulated signals of the 433 MHz carrier with 4.8 kbps data rate were generated by signal generator E4438C and then fed into the receiver. It is obvious that the receiver recovers the modulating signal very well. Figure 13 shows the measured receiver bit-error rate (BER) performance versus the input signal power for the 868 MHz band. At 1% BER, it achieves –64 dBm sensitivity at 434 MHz band and the minimum detectable signal is –62 dBm at 868 MHz, which is relative low than the

Table 1. Experimental results and comparisons.

Parameter	Ref. [10]	Ref. [11]	Ref. [12]	This work
Process	0.18 μm CMOS	0.25 μm CMOS	0.18 μm CMOS	0.35 μm CMOS
I/Q imbalance calibration	None	None	None	Mixed-signal mode
Modulation scheme	OOK	FSK/OOK	OOK	FSK/OOK
Input return loss S_{11}	NC	NC	NC	–20 dB@434 MHz –9.6 dB@868 MHz
Sensitivity	–65 to –37 dBm@916.5 MHz	< −100 dBm@912 MHz	< −58 dBm@150 MHz < −35 dBm@433 MHz < −15 dBm@1900 MHz	< −62 dBm@ 434MHz < −60 dBm@4868 MHz
Max input power (Saturation)	NC	> 13 dBm	< −15 dBm@150 MHz < −3 dBm@433 MHz	0 Bm@434 MHz 0 dBm@4868 MHz
P_{dc}	1.5 mA@1.8 V	19.7 mA@2.3–3.6 V	3 mA@0.45 V	5.2 mA@3 V
Chip area	1.82 mm^2	7.2 mm^2(transceiver)	0.09 mm^2	2 mm^2

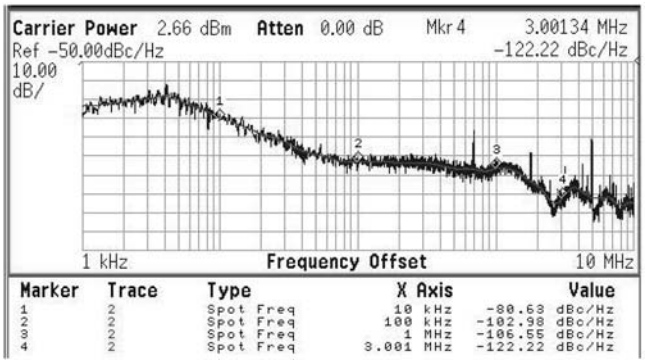

Fig. 14. PLL phase noise at 434.6 MHz.

speciation. The maximum input power is up to 0 dBm at 434 and 868 MHz. The reason for the deterioration of the sensitivity is that the receiver's clock is provided by the on-chip frequency synthesizer whose phase noise is poor and has critical effect on the receiver's sensitivity and the BER. Figure 14 shows the measured PLL phase noise of the 434.6 MHz carrier frequency, which is –103 dBc/Hz at 100 kHz offset and –106 dBc/Hz at 1 MHz. This is quite high. The measured performances are summarized in Table 1 in Section 5.

5. Conclusion

A fully integrated sub-1 GHz ISM-band receiver optimized for low power and low cost mixed-signal mode imbalance calibration circuit has been presented. It is implemented in a 0.35 μm CMOS process. The on chip inductor is not used and very few external components are required. In addition, impedance match network is not needed. In receiver mode, the prototype consumes only 15.6 mW at a 3 V power supply. The receiver performance is summarized in Table 1, and similar works are also listed for comparison.

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