A fast-settling frequency-presetting PLL frequency synthesizer with process variation compensation and spur reduction*

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Abstract: This paper proposes a fast-settling frequency-presetting PLL frequency synthesizer. A mixed-signal VCO and a digital processor are developed to accurately preset the frequency of VCO and greatly reduce the settling time. An auxiliary tuning loop is introduced in order to reduce reference spur caused by leakage current. The digital processor can automatically compensate presetting frequency variation with process and temperature, and control the operation of the auxiliary tuning loop. A 1.2 GHz integer-*N* synthesizer with 1 MHz reference input was implemented in a 0.18 μm process. The measured results demonstrate that the typical settling time of the synthesizer is less than 3 μs, and the phase noise is –108 dBc/Hz@1MHz. The reference spur is –52 dBc.

Key words: fast-settling; frequency synthesizer; process variation compensation; spur reduction
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1. Introduction

Fast frequency switching of frequency synthesizers is one of the challenges in modern wireless communications. How fast the communication channels can be switched and how fast the system can be turned on/off depend on the lock-in time. In order to realize the fast settling process of the PLL frequency synthesizer, dynamic loop bandwidth methods were proposed[1,2]. However the methods do not avoid the design tradeoff between the lock-in time and the phase noise or reference spurs. Fractional-*N* PLL frequency synthesizers were also proposed[3], but the additional fractional spurs and high-frequency quantization noise limit the increase of loop bandwidth, hence the locking speed[4,5]. Recently we reported a direct frequency presetting method to realize a fast-settling PLL frequency synthesizer[6]. The method can directly presets the target frequency with very small initial frequency error so that the synthesizer can speed up the lock-in process and avoid the tradeoff between the lock-in speed and the phase noise/spurs. But in practical application we have to manually adjust the presetting signal to compensate the presetting frequency error that results from the process variation and device parasitic effect. Then for integer-*N* PLL with low reference frequency, the reference spur and its harmonics are located at low offset frequencies. Therefore the reference spur should be low enough to ensure a clean spectrum.

This paper presents a fast-settling frequency-presetting PLL frequency synthesizer with process variation compensation and spurs reduction circuits. We develop a mixed-signal ring-type voltage controlled oscillator (VCO). The oscillation frequency of VCO can be preset with a small initial frequency error by a digital processor. We design an auxiliary tuning loop to compensate the leakage current of charge pump and loop filter in order to reduce reference spur and its harmonics[7]. The digital processor can automatically estimate the presetting frequency error that results from the process variation and device parasitic, and calibrate the relation between the target frequency and presetting signals. It also can control the operation of the auxiliary tuning loop.

2. Design of chip architecture

Figure 1 shows a block diagram of the proposed fast lock-in PLL frequency synthesizer. It has a main phase lock loop and an auxiliary tuning loop. The main phase lock loop consists of six blocks: a phase-frequency detector (PFD), a charge pump (CP), a second order loop filter (LPF), a mixed-signal VCO, a divider, and a digital processor. The digital processor consists of a divide ratio generator, loop controller, frequency sampler, linear interpolation module and presetting signal generator.

The mechanism that the frequency presetting method reduces the lock-in time of the synthesizer significantly is as

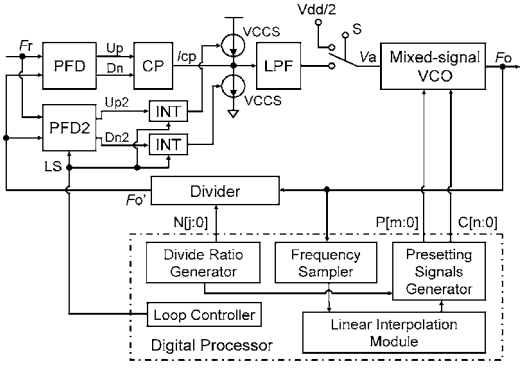

Fig. 1. PLL frequency synthesizer architecture.

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follows. First, the lock-in time of frequency synthesizer is defined as

$$T_{\rm l} = \frac{-\ln\left(\frac{\rm tol}{\Delta f} \times \sqrt{1-\zeta^2}\right)}{\zeta\omega}. \quad (1)$$

The factor tol is the acceptable frequency error, Δf is the initial frequency error, ζ is the damping factor, and ω is the natural frequency of PLL loop. Equation (1) shows that the lock-in time depends on the magnitude of initial frequency error Δf. The frequency presetting method is to preset the frequency of VCO output signal to the target-frequency within a short time by some digital presetting signals, if the presetting-frequency is very close to the target-frequency, Δf can be greatly reduced and the lock-in time will be shortened. Of cause the efficiency of this method depends on the precision of VCO presetting-frequency, so the relation between the output frequency of VCO and the presetting digital signals should be accurately defined. However, in practical application this relation will be different from simulation results due to the process variation, device parasitic effect and temperature. So an automatic calibration process is needed to redefine the relation between output frequency of VCO and the presetting signals, in order to reduce the frequency presetting error caused by the process variation, device parasitic effect and temperature.

The proposed frequency synthesizer can work in two modes: calibration mode and operation mode. When the synthesizer starts up or receives a reset signal, it firstly works in the calibration mode. The digital processor measures the output frequency of VCO and calibrates the relation between the output frequency and the presetting digital signals C and P automatically. After the calibration process is finished, the synthesizer switches to the operation mode. The digital processor outputs the presetting signals C and P to directly preset the frequency of VCO. After the output frequency of VCO is preset with very small initial frequency error, the output voltage $V_{\rm a}$ of LPF precisely tunes the frequency of the VCO. Therefore the synthesizer can settle down in a very short time. Its lock-in time does almost not depend on frequency step, process variation, device parasitic effect and chip temperature.

Another issue in the integer-n PLL frequency synthesizer design is the reference spur caused by leakage current of charge pump and loop filter. The power of the reference spur Pr in the PLL in is approximately given by

$$\Pr = 20\lg\left(\frac{1}{\sqrt{2}}\frac{f_{\rm BW}}{f_{\rm REF}}N\Phi\right) - 20\lg\left(\frac{f_{\rm REF}}{f_{\rm P1}}\right)[\rm dBc], \quad (2)$$

where $f_{\rm BW}$ is the loop bandwidth, $f_{\rm REF}$ is the reference frequency, $f_{\rm P1}$ is the frequency of the pole in the loop filter, N is the division ratio, and Φ is the phase offset due to the leakage current given by

$$\Phi = 2\pi \times \frac{I_{\rm LEAK}}{I_{\rm CP}}[\rm rad], \quad (3)$$

where $I_{\rm LEAK}$ is the leakage current and $I_{\rm CP}$ is the charge pump current. In order to reduce the area of loop filter, small charge pump current (100 μA) is used in the frequency synthesizer design, which makes the reference spur more sensitive to the leakage current. In order to reduce the reference spur, an auxiliary tuning loop is introduced in the proposed frequency synthesizer. The feedback path of auxiliary tuning loop consists of an additional phase-frequency detector (PFD2) with dead zone, two voltage integrators (INT) and two voltage controlled current sources (VCCS). During the settling process of the synthesizer, the auxiliary loop is disabled by the loop controller. The outputs of the two VCCSs are zero. After the synthesizer is locked, the auxiliary loop will be enabled and PFD2 will detect the phase offset between $F_{\rm r}$ and $F_{\rm o}$, caused by leakage current. The output voltage pulses will be integrated by INTs, and the output of INTs will control the VCCSs to compensate the leakage current. The voltage ripple on $V_{\rm a}$ can be reduced, which will decrease the magnitude of reference spur and its harmonics[7].

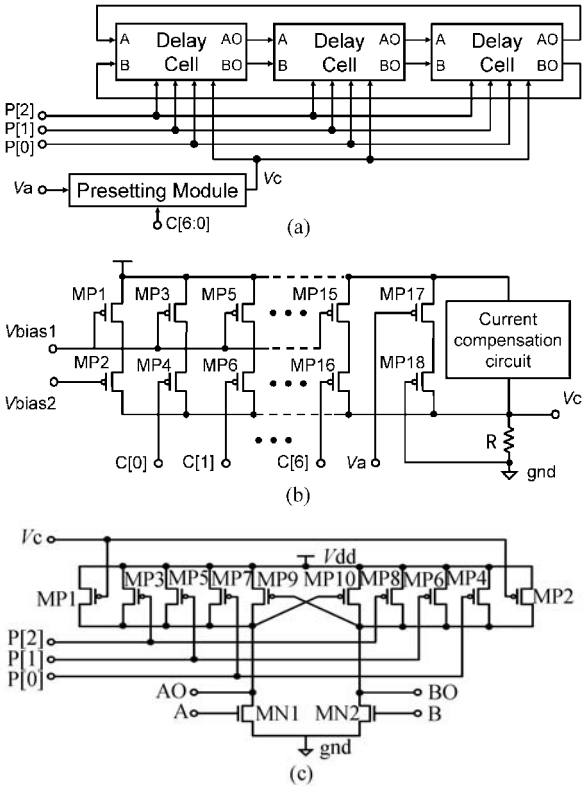

Fig. 2. Mixed-signal VCO with a presetting module: (a) Top architecture; (b) Presetting module; (c) Delay cell.

3. Circuits design and operations

Figure 2 shows the architecture and circuits of proposed mixed-signal ring-type VCO. Figure 2(a) shows the top architecture of the VCO. It consists of three stages of delay cells and a presetting module. The presetting module receives the presetting digital signal C[6:0] and the output signal $V_{\rm a}$ of LPF, and produces a control signal $V_{\rm c}$. On the other hand, the digital signal P[2:0] controls the transition currents in the delay cells and generates four overlapped discrete tuning curves to lower VCO gain $K_{\rm v}$ and to cover the desired frequency range. Smaller $K_{\rm v}$ will benefit to the phase noise performance. The multiple tuning curves can compensate for the variation in the

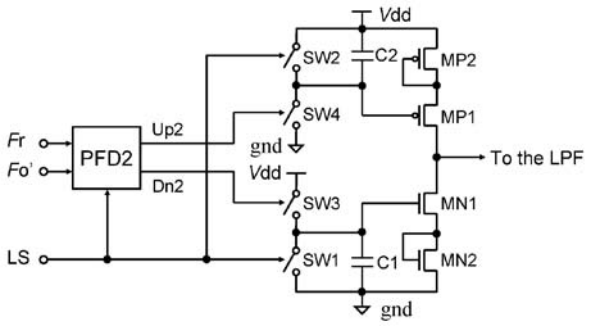

Fig. 3. Feedback path of auxiliary tuning loop.

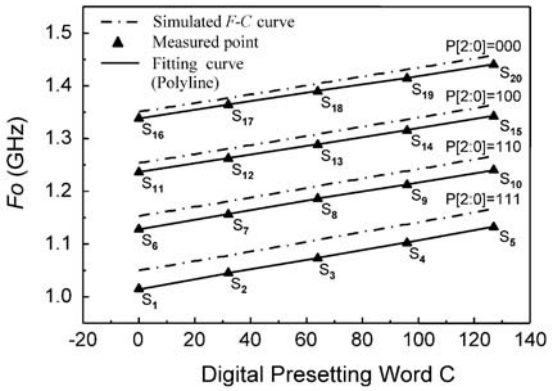

Fig. 4. Output frequency F_o versus presetting signal C[6:0] and P[2:0].

VCO frequency due to process variation.

Figure 2(b) shows the presetting module. It is a mixed-signal circuit. When a digital signal C[6:0] is inputted into the presetting module, the module produces a voltage signal V_c to preset the frequency of VCO with a small initial frequency error. Then the output signal V_a of LPF accurately tunes the frequency of VCO by adjusting the current through MP17. The additional current compensation network circuit is designed to make the presetting frequency to depend linearly on the signal C[6:0]. If the divide ratio N signal of the synthesizer is changed, the presetting signals C[6:0] and P[2:0] can accurately preset the frequency of the VCO. Then the output signal V_a of the LPF precisely tunes the frequency of the VCO within a very short time.

Figure 2(c) shows the delay cell in the VCO. It is a differential inverter with parallel active loads. Transistors MP9 and MP10 are added to the delay cell to constitute a CMOS latch, which will increase the speed of transition between V_{dd} and ground. The signal V_c tunes the oscillation frequency by adjusting the transition currents of MP1 and MP2. Additional current sources MP3–MP8 are controlled by digital signals P[2:0] in order to generate the multiple tuning curves.

Figure 3 shows the feedback path of auxiliary tuning loop. The PFD2 is a phase-frequency detector with dead zone. When the synthesizer is locked, the PFD2 will not affect the main phase lock loop if there is no leakage current in CP and LPF. The INTs are implemented with switches and capacitors. The VCCSs are implemented with transistors: MP1, MP2, MN1 and MN2. During the lock-in process, the signal LS is high. Outputs of PFD2 are zeros, and switches SW1 and SW2 are turned on. Voltages across the capacitors C_1 and C_2

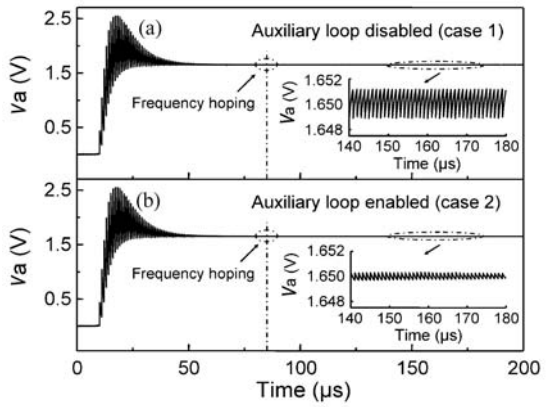

Fig. 5. Transient voltage of V_a: (a) Auxiliary loop disabled; (b) Auxiliary loop enabled.

are zeros, so the transistors MP1 and MN1 are shut down. There is no compensation current flow into or out of the LPF. After the synthesizer settles down, the signal LS will be low. If there is leakage current in CP and LPF, one output of PFD2 (Up2 or Dn2) will generate voltage pulses. Switches SW1 and SW2 will be turned off and the output voltage of PFD2 will be integrated into C_1 and C_2 by switching SW3 or SW4. One of the VCCSs will be turned on, and the current will flow into or out of the LPF to compensate the leakage current in CP and LPF.

Figure 4 shows the dependence of the VCO presetting frequency on the presetting signals C[6:0] and P[2:0] at $V_a = V_{dd}/2$. The simulated result shows good linear relation between the presetting frequency and the signal C under different P signals. The initial frequency error is less than ±0.5 MHz. But, the measured result shows that if the calibration process was not carried out, the dependence of the VCO presetting frequency on signal C deviated from the simulation result due to process variation and device parasitic effect. So the processor can not preset the VCO with very small initial frequency error. In practical application, the digital processor can automatically calibrate the relation between the presetting frequency and the signals C and P in the calibration working mode by the following algorithm. First the main phase lock loop is opened by the switch S and the input of VCO is biased by $V_{dd}/2$. Then the dependence of the VCO presetting frequency on the signal C under different P signals is automatically measured by the frequency sampler at n sampling points S_i ($i = 1,\ldots,n$). Next the linear interpolation module uses the measured data to form multiple fitting curves. Figure 4 also shows this calibrated dependence of the VCO presetting frequency on signal C under different P signals. After the calibration process is finished, the main phase lock loop is closed. Thus the synthesizer switches to the operation mode and the processor can accurately preset the VCO frequency according to the fitting curves.

4. Simulation results

We simulated the transient voltage of node V_a (in Fig. 1) in two cases: the auxiliary loop is disabled (case 1) and the auxiliary loop is enabled after the synthesizer settles down

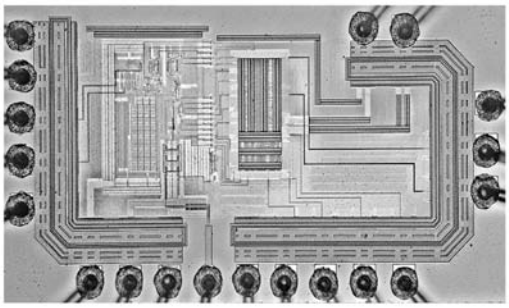

Fig. 6. Chip micrograph.

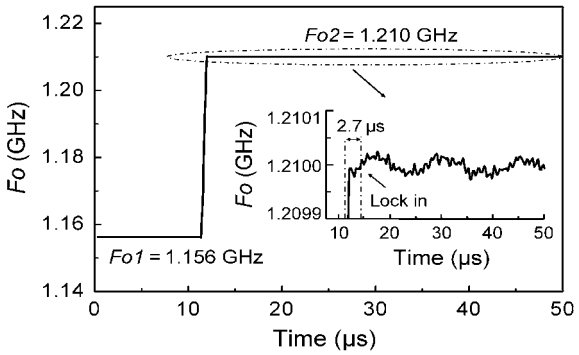

Fig. 7. Frequency hopping characteristic.

(case 2). In simulations, a 10 nA leakage current is added to the LPF during the normal operation. Figures 5(a) and 5(b) show the simulated voltages of V_a in case 1 and case 2 respectively. A frequency hoping happened at 85 μs. The voltage of V_a shows no variation, which means the synthesizer settled in a very short time. The voltage ripple in V_a is reduced by the auxiliary loop (case 2), and became much less than that in case 1. It indicates that the auxiliary loop can significantly reduce reference spur at the output of frequency synthesizer.

5. Experimental results

The proposed synthesizer was implemented in 1P6M, 0.18 μm CMOS process with 3.3 and 1.8 V power supply. The die micrograph of proposed frequency synthesizer is presented in Fig. 6. The chip core area is 0.32 mm^2. The test chip consumes current of 23 mA that includes large buffer of VCO output for measurement. The measured output frequency of VCO ranges from 1.01 to 1.44 GHz. After the synthesizer was automatically calibrated, many frequency hopping operations between two any frequencies F_{o1} and F_{o2} were performed randomly and continuously. The frequency hopping was measured by vector signal analyzer. Figure 7 shows a typical frequency hopping characteristic of the synthesizer. The dependence of the frequency on time shows that the frequency hopped rapidly from 1.156 to 1.210 GHz at 12 μs. The lock-in time is less than 3 μs, which is much shorter than that of a conventional synthesizer.

Figure 8 shows the measured spectrum of output signal at the frequency of 1.21 GHz. Figure 8(a) shows the spectrum when the auxiliary tuning loop is disabled. The reference spur is –42.38 dBc. Figure 8(b) shows the spectrum when the auxiliary tuning loop is enabled, the reference spur reduces to −52.1 dBc.

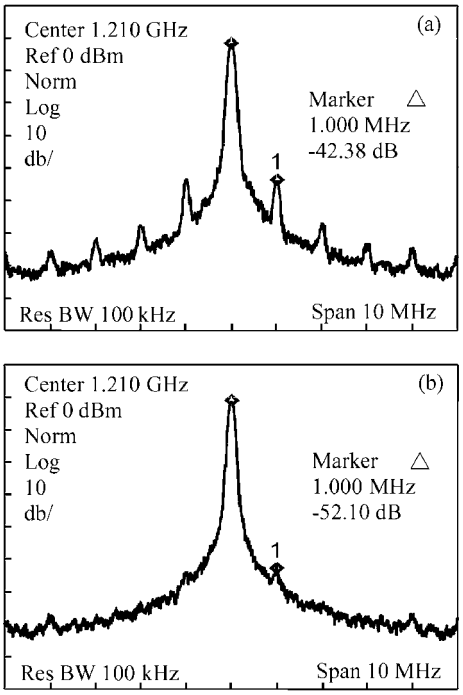

Fig. 8. Spectrum of output signal: (a) Auxiliary loop disabled; (b) Auxiliary loop enabled.

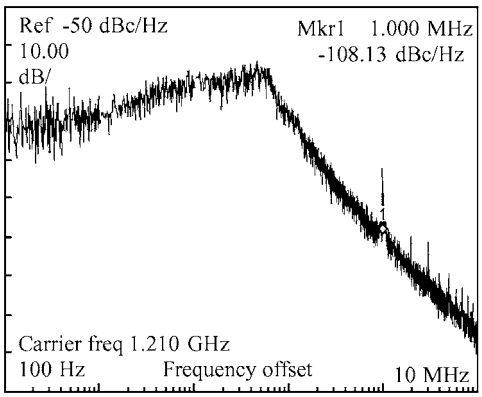

Fig. 9. Phase noise of output signal.

Figure 9 shows the measured phase noise of output signal, when two loops are working. The phase noise is −108 dBc/Hz at 1 MHz offset from center-frequency. The measured performances are summarized and compared to other reported designs in Table 1.

6. Conclusion

We proposed a fast lock-in PLL frequency synthesizer with process variation auto-compensation and spurs reduction circuits. The compensation algorithm calibrates the presetting frequency error caused by process variation and temperature, which improves the efficiency of frequency presetting method and greatly speeds up the lock-in process of the synthesizer. The auxiliary tuning loop of PLL reduces the reference spur caused by leakage current. We implemented the synthesizer in a 0.18 μm CMOS process. The measured results showed that the frequency synthesizer has fast lock-in speed and small reference spur. It avoids the tradeoff between the lock-in speed and the phase noise/spurs.

Table 1. Performance summary and comparison.

Parameter	Ref. [1]	Ref. [5]	This work
Fast settling method	Dynamic loop bandwidth	Wide-bandwidth fractional-*N*	Frequency presetting with calibration
Process	0.6 μm CMOS	0.18 μm CMOS	0.18 μm CMOS
Chip core area (mm^2)	0.11	4.8	0.32
Supply voltage (V)	3	1.8	3.3/1.8
Frequency range (GHz)	0.08–0.25	2.4–2.5	0.99–1.45
Loop bandwidth (kHz)	—	> 730	< 100
VCO type	Ring	LC	Ring
VCO gain (MHz/V)	100	60	25
Lock-in time	30 cycles (dependent on frequency step)	35 μs (independent on frequency step)	3 μs (independent on frequency step)
Spur @1 MHz (dBc)	—	–47	–52
Phase noise	2.544 ps (RMS)	−101 dBc/Hz @ 100 kHz −124 dBc/Hz @ 3 MHz	−79 dBc/Hz @ 100 kHz −108 dBc/Hz @ 1 MHz

References

[1] Lee J, Kim B. A low noise fast-lock phase-locked loop with adaptive bandwidth control. IEEE J Solid-States Circuits, 2000, 35: 1137

[2] Yang C Y, Liu S I. Fast settling frequency synthesizer with a discriminator-aided phase detector. IEEE J Solid-States Circuits, 2000, 35: 1445

[3] Riley T A D, Copeland M A, Kwasniewski T A. Delta-Sigma modulation in fractional-*N* frequency synthesis. IEEE J Solid-States Circuits, 1993, 28: 553

[4] Rhee W, Song B, Ali A. A 1.1 GHz CMOS fractional-*N* frequency synthesizer with 3-b third order $\Delta\Sigma$ modulator. IEEE J Solid-State Circuits, 2000, 35: 1453

[5] Swaminathan A, Wang K J, Galton I. A wide-bandwidth 2.4 GHz ISM band fractional-*N* PLL with adaptive phase noise cancellation. IEEE J Solid-State Circuits, 2007, 42: 2639

[6] Kuang X F, Wu N J. A fast-settling monolithic PLL frequency synthesizer with direct frequency presetting. ISSCC Digest of Technical papers, 2006: 204

[7] Wang H, Shou G, Wu N. An adaptive frequency synthesizer architecture reducing reference sidebands. IEEE International Symposium on Circuits and Systems, May 2006: 3081