Active layer self-protection process for organic field-effect transistors*

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Abstract: To isolate the active layer from air, double organic layer organic field-effect transistors have been fabricated, based on a two-step vacuum-deposition process. Pentacene acted as the active layer, and subsequently, CuPc was deposited above the pentacene and served as a protecting layer for the active layer. Due to the same electrical characteristics but different morphologies, the bilayer structure was effective in decreasing the contamination of impurities and gas, and then improved the device stability in air.

Key words: OFET; pentacene; CuPc; stability
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1. Introduction

Organic field-effect transistors (OFETs), due to their low-cost, flexibility, and large-area application advantages, have great potential as switching devices for active-matrix OLED displays, low-end smart cards and identification tags[1–4]. Over the last ten years, significant progress has been made on OFET performance and their mobilities have been comparable to or even greater than those of amorphous silicon (0.1–1 $cm^2/(V{\cdot}s)$) with the use of common organic semiconductors, such as pentacene, CuPc, and poly(3-hexylthiophene)[5, 6]. In spite of many remarkable advantages, organic field-effect transistors are currently subject to some major defects. For example, because organic materials are sensitive to oxygen and moisture, OFETs show little performance stability under ambient conditions[7]. The oxygen and moisture molecules can diffuse into organic grain boundaries, causing either trapping or doping of charge carriers[8]. If the active organic molecules could be isolated from ambient conditions, the transistors' stability would be clearly improved. In this paper, we report a simple process to protect the active layer organic molecules from the impurities contaminating the organic semiconductor. The active layer is formed into a double layer with pentacene and CuPc. Pentacene serves as the active layer, with CuPc covering it. The second organic material, CuPc, can not only function as the active layer but protect the pentacene from contamination by gas and metal particles.

2. Experiment

Figure 1 shows a schematic diagram of the bilayer OFET. We fabricated the bilayer OFET on a highly doped n^+-Si wafer which was prepared with a 300 nm thermally grown oxide layer. The wafer worked as a gate electrode, and the oxide layer acted as a gate insulator. The surface of the substrate was ultrasonically cleaned in acetone, alcohol and deionized water. Then pentacene and CuPc were vacuum-deposited on the substrate with an optimizing thickness of 35 nm and 25 nm in sequence. During this two-step vacuum-deposition process, after the pentacene was deposited, the CuPc was immediately deposited above the pentacene to form a protecting layer. Then the active layer was kept from exposure in to air. The pentacene and CuPc deposition was carried out with a deposition rate of 0.2 Å/s at a base pressure of 10^{-6} torr. Pentacene and CuPc were purchased from Sigma-Aldrich Trading Corporation with double purification. The last step was to form 50 nm thick gold source and drain electrodes on the CuPc film by e-beam deposition through a metal shadow mask. The channel length and width of the top electrode were fixed at 60 μm and 500 μm, respectively. To distinguish the action of the CuPc protecting layer, we also fabricated common pentacene based OFETs without a CuPc layer. The morphological and electrical measurements were performed by atomic force microscopy (AFM) and a Keithley 4200 scs, respectively.

3. Results and discussion

It is well known that the organic film morphology intensively influences the transistor's electric performance. The

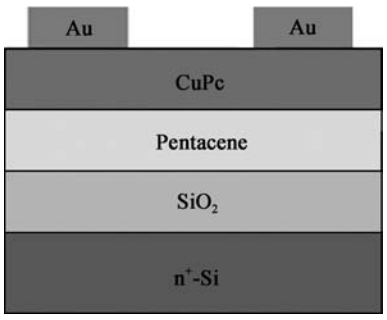

Fig. 1. Schematic diagram of the top-contact bilayer OFET.

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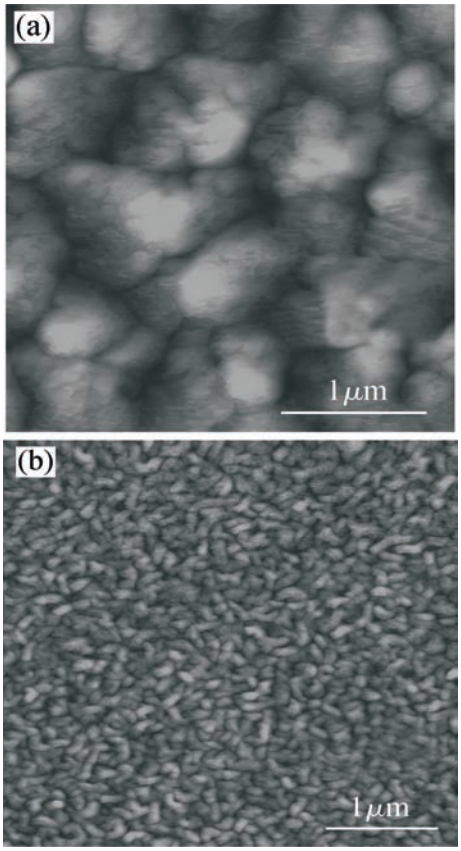

Fig. 2. AFM images of (a) pentacene and (b) CuPc.

morphologies of the pentacene and CuPc films were characterized by AFM. As shown in Fig. 2(a), the pentacene is very flat, with an average roughness ~ 4Å, and the grains grow to an even size of about 300 nm in the 1 μm square area. Figure 2(b) shows the AFM image for CuPc. Because of the different morphologies, it helps to form a compact interface between the pentacene and CuPc, which can protect the pentacene from contamination by impurities and gas.

Figure 3 shows the typical drain output and transfer characteristics of the bilayer pentacene OFET. All electrical measurements were carried out in air at room temperature and in darkness to avoid the irradiation of light. The transistors, using gold as drain-source electrodes, exhibit an obvious field effect with operation in a p-type accumulation mode. As can be seen in Fig. 3(a), with the magnitudes of V_{SD} and V_{SG} increasing, a linear current regime was initially observed at low drain voltages ($V_{SD} < V_{SG}$), followed by a saturation regime when the drain voltage exceeded the gate voltage. The source–drain currents in the linear and saturation regimes are characterized by Eqs. (1) and (2), where L and W are the channel length and width, C_i is the capacitance of the insulator per unit area, and $I_{D,sat}$, V_G, and V_T are the saturated drain current, the gate voltage, and the threshold voltage, respectively[9].

$$I_D = \frac{WC_i\mu}{L}\left(V_G - V_T - \frac{V_D}{2}\right)V_D, \quad (1)$$

$$I_D = \frac{W}{2L}\mu_{sat}C_i\,(V_G - V_T)^2\,. \quad (2)$$

The linear behavior of the drain current at low drain voltage values indicated that good Ohmic contact was

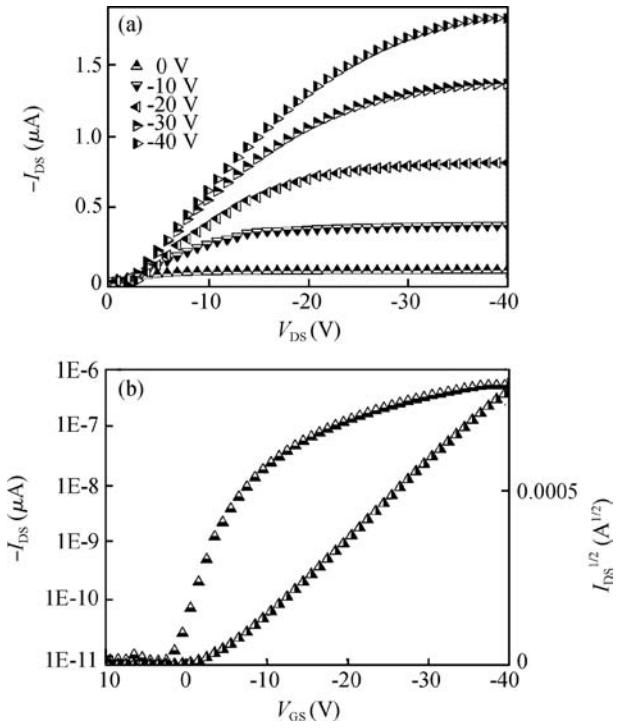

Fig. 3. Drain output and transfer characteristics of the bilayer OFET.

realized between source/drain electrodes and the organic semiconductors[10]. Figure 3(b) shows the dependence of the drain current and the square root of the drain current on the gate voltage at a fixed drain voltage of −30 V. Threshold voltage V_T was determined from the linear regression of the measured data plotted as $\sqrt{I_D}$ versus V_G. The on/off ratio and the subthreshold swing estimated from Fig. 3(b) are about 10^5 and 3.5 V/decade, respectively. We also evaluated the saturation mobility μ_{sat} from the slope of the square root of the drain current plot using Eq. (2). The estimated mobility and the threshold voltage are 0.08 cm^2/(V·s) and −6 V. The mobility is a little lower than some literature reports. We considered the low mobility to be attributed to traps on the dielectric surface. If the substrate surface was treated with OTS or HMDS before the pentacene was deposited, the hole-carrier mobility would obviously increase[11]. In addition, the inserted CuPc layer between the pentacene and gold electrodes added to the total thickness between the dielectric surface and the Au electrodes, which lengthened the carrier transport length, resulting in a higher resistance. This contributes to the lower drain current of the devices[12].

Figure 4 shows the drain output and transfer characteristics of the bilayer pentacene-based OFET 3 months later. The devices were stored in a silicon slice carrier, and then placed in a metal cabinet without further protection. It was found that the magnitude of the on-state drain current and on/off ratio had not changed significantly. As shown in Fig. 4, the maximum saturation drain current was about 2.4 μA, which was a little lower than 3 months previously, and the on/off ratio was still approximately 10^5. This indicated that the stability of the bilayer OFET was good. However, by comparing Fig. 3(b) with Fig. 4(b), we also found that the subthreshold swing obviously increased (from 3.5 to 5 V/decade). Simultaneously,

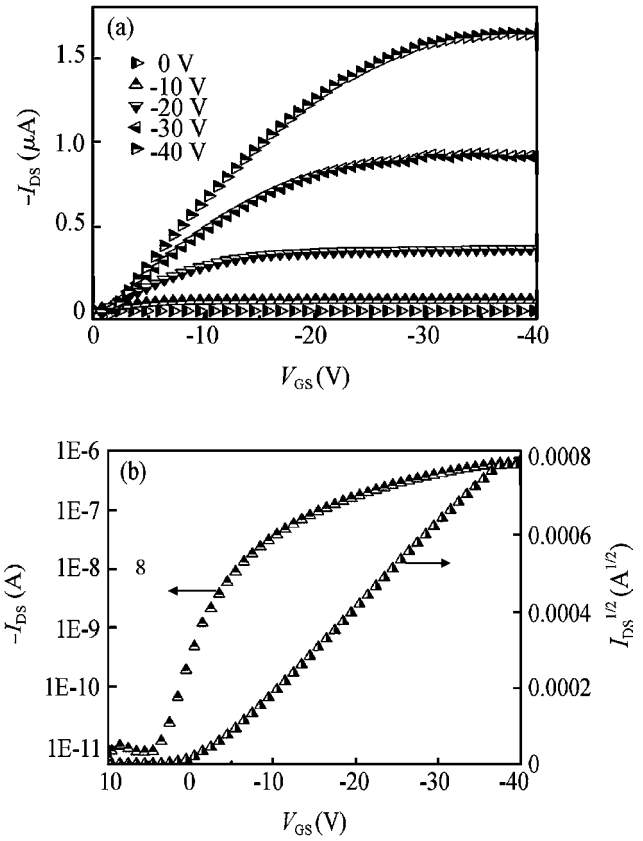

Fig. 4. Drain output and transfer characteristics of the bilayer OFET after 3 months in a continuous air environment.

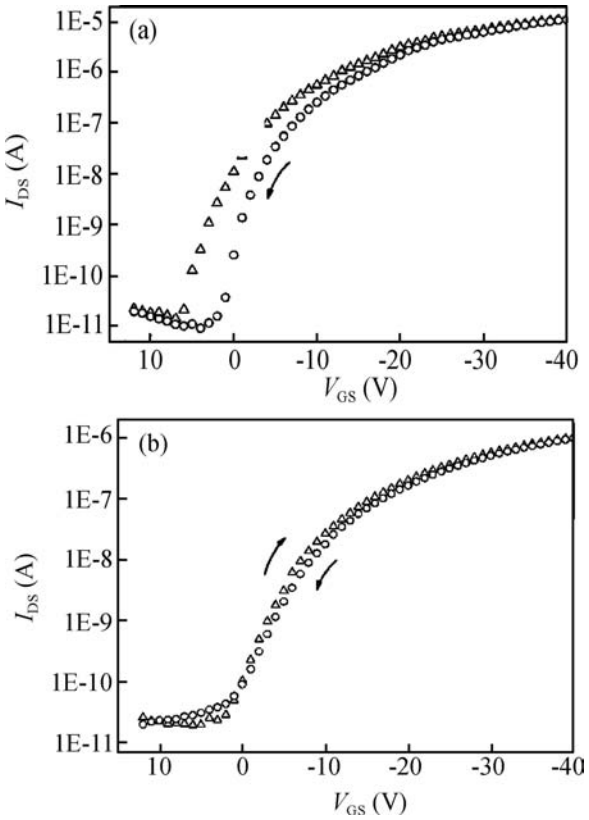

Fig. 5. Transfer characteristics of pentacene-based OFETs (a) without and (b) with the CuPc protecting layer in air after a period of 3 months.

the threshold voltage also decreased from –6 to –5 V. This implied that the 25 nm thick CuPc could not completely protect the pentacene from the influence of oxygen and vapour in the air[13].

To verify the action of the CuPc layer, we made a comparison between the bilayer active layer pentacene-based OFET and common pentacene-based OFET without the CuPc protecting layer. Figure 5 shows the transfer characteristics of these two pentacene based OFETs in air 3 months later. Judging by the transfer characteristics, the OFET without the CuPc layer shows a clear hysteresis phenomenon, seen in Fig. 5(a), while the bilayer OFET suffered less hysteresis under ambient conditions after the same 3 month period. The hysteresis indicates that the traps increased in the device channel. The traps in the channel generally resulted from oxygen and moisture doping, impurity contamination, or even reflection of the electrode metal from the organic molecule[8, 14]. Figure 5(b) indicates the CuPc protecting layer alleviated the occurrence of traps in the pentacene film. Of course, to further improve the device stability, the fabrication process and the selection of protecting materials need further study.

4. Conclusion

We presented a simple method to improve OFET stability. The device channel was fashioned into a bilayer with pentacene acting as the active layer and CuPc serving as the protecting layer. With this geometry, the vital component of the device, that is, the organic semiconductor layer, was protected as soon as it was deposited without exposure in air. CuPc has similar electric characteristics but different grain size. This allowed the CuPc to fill the vacant spaces in the pentacene, and then form a compact interface between it and the pentacene, which helped to restrict the contamination of the pentacene by impurities and gas. The similar electric characteristics of the two organic layers prevented the CuPc from weakening the performance of the integrated device. Also, by employing this bilayer structure, the device stability in air was distinctly improved.

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