Degradation of ultra-thin gate oxide LDD NMOSFET under GIDL stress*

Hu Shigang(胡仕刚)†, Hao Yue(郝跃), Cao Yanrong(曹艳荣), Ma Xiaohua(马晓华), Wu Xiaofeng(吴笑峰), Chen Chi(陈炽), and Zhou Qingjun(周清军)

(Key Laboratory of Wide Band-Gap Semiconductor Materials and Devices, School of Microelectronics, Xidian University, Xi'an 710071, China)

Abstract: The degradation of device under GIDL (gate-induced drain leakage current) stress has been studied using LDD NMOSFETs with 1.4 nm gate oxides. Experimental result shows that the degradation of device parameters depends more strongly on V_d than on V_g. The characteristics of the GIDL current are used to analyze the damage generated during the stress. It is clearly found that the change of GIDL current before and after stress can be divided into two stages. The trapping of holes in the oxide is dominant in the first stage, but that of electrons in the oxide is dominant in the second stage. It is due to the common effects of edge direct tunneling and band-to-band tunneling. SILC（stress induced leakage current）in the NMOSFET decreases with increasing stress time under GIDL stress. The degradation characteristic of SILC also shows saturating time dependence. SILC is strongly dependent on the measured gate voltage. The higher the measured gate voltage, the less serious the degradation of the gate current. A likely mechanism is presented to explain the origin of SILC during GIDL stress.

Key words: GIDL; interface traps; direct tunneling; SILC
DOI: 10.1088/1674-4926/30/4/044004 **PACC:** 7340G; 7320; 7340Q

1. Introduction

The off-state drain leakage is one of the big issues for aggressively shrunk MOSFETs. Gate-induced drain leakage current (GIDL) is a major source of off-state drain leakage current[1]. For a fresh MOSFET, GIDL is attributed to band-to-band tunneling process at Si/SiO_2 interface due to the gate-induced high field at the deep-depleted gate-to-drain overlap region. It is one of the major issues for retention time degradation in dynamic random access memories (DRAM's)[2–6]. Reducing the size of a DRAM cell usually causes an increase of the electric field under the gate which makes the cell transistor more susceptible to GIDL. The GIDL current itself involves hot-hole effects which can introduce holes trapping in gate oxides and result in device instabilities. However, the location of these trapped holes which affect the GIDL current mostly is still uncertain[7, 8]. With the scaling down of the thickness of active dielectrics in CMOS, direct-tunneling (DT) gate leakage becomes significant in transistor operation. So the off-state device reliability should be an important issue. Much research has been done on GIDL stress, but no complete agreement has been reached about its degradation mechanism.

Our previous work focused on GIDL current in 90 nm CMOS technology using lightly-doped drain (LDD) NMOSFET and showed that the drain bias V_d has a strong effect on GIDL current as compared with the gate bias V_g[8]. The threshold (V_{th}) degradation has also been investigated under GIDL stress in LDD NMOSFET with 1.4 nm thick gate oxide in our work[7]. But these investigations have not dealt with the effect of GIDL stress on the degradation of device deeply and have not given a good analysis on the damage mechanism. It is necessary to perform a further investigation on GIDL stress.

In this paper, we study the off-state instabilities of NMOSFET with 1.4 nm gate oxides under GIDL stress. The degradation of device parameters is also presented. The effects of GIDL stress on GIDL current and the stress induced leakage current (SILC) is emphasized. The characteristics of the GIDL current are used to analyze the damage generated during the stress. A likely mechanism is presented to explain the origin of SILC during GIDL stress.

2. Devices and experiments

The devices used in this paper are LDD NMOSFETs, fabricated in a standard 90 nm CMOS technology. The LDD NMOSFET is a surface device with N^+ poly-Si gate. The gate oxide thickness (T_{ox}) of the device is 1.4 nm with decoupled-plasma-nitridation (DPN) processing. The NMOSFETs have a channel length (L) of 0.35 μm and a width (W) of 5 μm. The operation voltage is 1.0 V for the MOSFETs. GIDL stress and I–V measurements were made by an Agilent B1500A semiconductor parameter analyzer. The GIDL stress was performed at $V_g < 0$ V and $V_d > 0$ V, while the source and substrate electrodes were grounded. Stress was interrupted at regular intervals and device parameters were measured. GIDL current were periodically monitored by fixing V_d at 1.2 V and sweeping V_g from −1.5 to 0 V. The SILCs were characterized by measuring the I–t (gate current–stress time) and I–V (gate current–gate voltage) characteristics at constant, low, pre-tunneling voltages at regular intervals. All experiments were carried out at room temperature.

* Project supported by the National Natural Science Foundation of China (Nos. 60736033, 60506020).
† Corresponding author. Email: hsg99528@126.com
Received 16 September 2008, revised manuscript received 14 October 2008 © 2009 Chinese Institute of Electronics

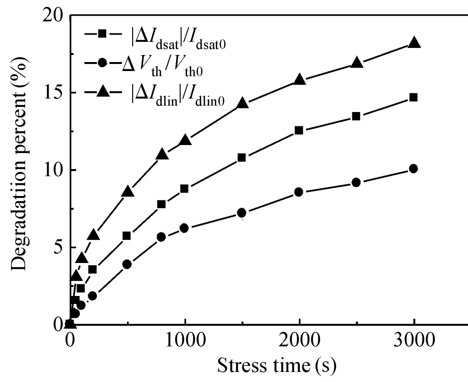

Fig. 1. Time dependence of degradation of device parameters in NMOSFET under GIDL stress.

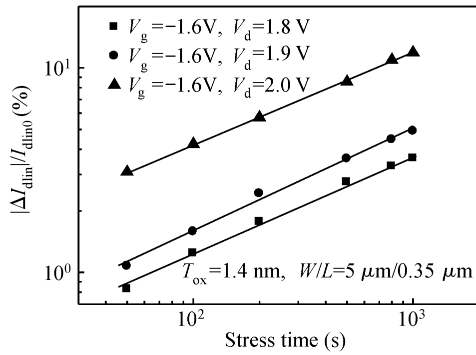

Fig. 2. Time dependence of I_{dlin} degradation in NMOSFETs during GIDL stresses at constant V_g.

Aggressive shrinking of MOSFET causes direct-tunneling (DT) gate leakage to become significant in transistor operation. In this thin gate oxide region, direct tunneling current increases exponentially with oxide thickness decreasing, which is of primary concern for CMOS scaling[9, 10]. The GIDL stress is performed at $V_g < 0$ V and $V_d > 0$ V, a strong vertical field will be generated in the gate/drain overlap region. Edge direct tunneling (EDT) of electron from n^+ polysilicon gate to underlying n-drain extension will play important role during GIDL stress. The degradation of device is due to the common effects of edge direct tunneling and band-to-band tunneling.

3. Results and discussion

First, the degradation of device parameters is studied under GIDL stress in NMOSFETs. Figure 1 shows the time dependence of degradation of device parameters. The degradation of device parameters is very particular. V_{th} in the NMOSFET increases and the other parameters in the NMOSFET decrease with time. The degradation of linear drain current (I_{dlin}) is the most serious, that of saturation drain current (I_{dsat}) is the second. GIDL stress not only depends on the gate voltage V_g, but also the drain voltage V_d. It is necessary to investigate the different influences of V_g and V_d on the degradation of device. The I_{dlin} degradation has been studied under different GIDL stress conditions. The I_{dlin} degradation during GIDL stresses at constant V_g increases with increasing V_d as shown in Fig. 2, that at constant V_d increases with increasing V_g as shown in Fig. 3, and that at constant drain–gate voltage V_{dg}

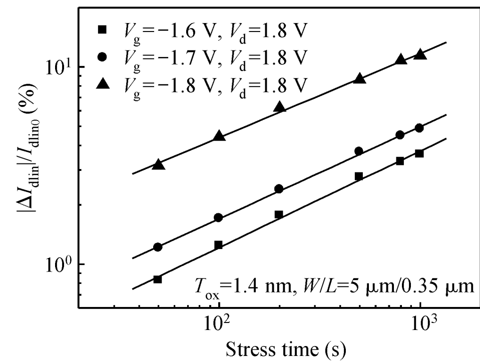

Fig. 3. Time dependence of I_{dlini} degradation in NMOSFETs during GIDL stresses at constant V_d.

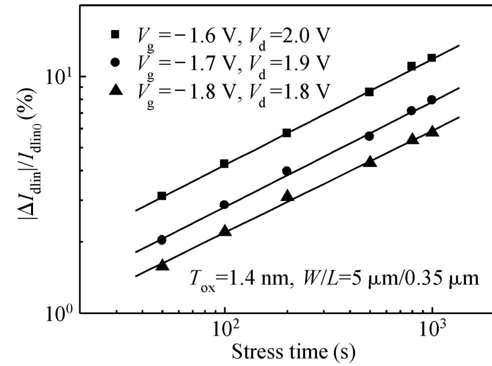

Fig. 4. Time dependence of I_{dlin} degradation in NMOSFETs during GIDL stresses at constant V_{dg}.

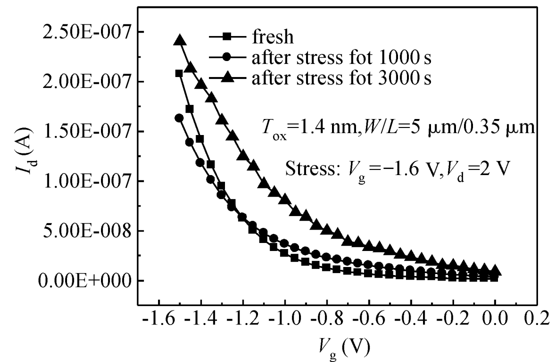

Fig. 5. GIDL current evolution before and after GIDL stress.

($V_{dg} = V_d - V_g$) increases with increasing V_d as shown in Fig. 4. It is evident that the degradation of device depends more strongly on V_d than on V_g.

Second, the damage is investigated through the analysis of GIDL current. Because the GIDL current is very sensitive to the trapped charge and the interface traps at the interface in the gate–to-LDD region. For NMOSFETs, all the interface traps become neutral at high V_{dg}, thus only the oxide trapped charges affect the GIDL current[11]. But at low V_{dg}, interface traps alter the GIDL current by introducing a trap-assisted leakage component[12]. GIDL current was periodically monitored at each stress condition. From GIDL current evolution before and after GIDL stress as shown in Fig. 5, it is found that the change of GIDL current can be divided into two stages. In the first stage, the GIDL current increases at low V_{dg}, which indicates that interface traps generated during GIDL stress

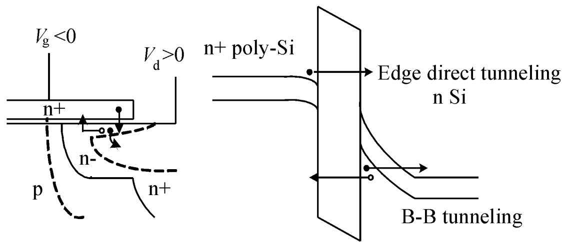

Fig. 6. Device cross section and band diagram at the gate-to-drain overlap region under GIDL stress (• indicates electron, ◦ indicates hole).

which assists in band-to-band tunneling. Meanwhile, GIDL current decreases at high V_{dg}, which gives the evidence that the holes are trapped in the oxide during GIDL stress. These trapped holes at the interface depress energy band bending of Si at interface in the gate-to-LDD region. As a result, the electron tunneling length from valence band to conductance band becomes longer and the GIDL current decreases. In the second stage, the GIDL current continues to increase at low V_{dg}, which indicates that interface traps still generated during GIDL stress. Meanwhile, GIDL current increases at high V_{dg}, which shows that the electrons are trapped in the oxide during GIDL stress. These trapped electrons at the interface make the electron tunneling length from valence band to conductance band become shorter, so the GIDL current increases. From the above analysis, it can be concluded that it is inaccurate to argue that GIDL stress only to introduce holes trapping in gate oxides. Although the GIDL current itself involves hot-hole effects which can introduce holes trapping in gate oxides and result in device instabilities, there must be some other mechanism playing an important role during GIDL stress.

Figure 6 shows device cross section and band diagram at the gate-to-drain overlap region under GIDL stress. Band-to-band tunneling happens in the deep-depletion region of drain underneath the gate-to-drain overlap; among all the holes created from the band-to-band tunneling, most of them flow into the substrate due to the lateral field, while just a fraction of the holes are injected into the gate oxide with the aid of the vertical field. These trapped holes cause GIDL current at high V_{dg} to decrease in the early stage of GIDL stress as shown in Fig. 5. But for thin gate oxide thicknesses, electrons tunneling from the gate can not be neglected. Those trapped holes created from band-to-band tunneling can be neutralized rapidly by a subsequent electron injection into the same region. The decreased GIDL current at the high V_{dg} can be quickly recovered by the subsequent injection of electrons, and even increases beyond the original value. This results in an increase of GIDL current at the high V_{dg} in the last stage of GIDL stress as shown in Fig. 5. In a word, electrons from the gate and holes created from the band-to-band tunneling are probably injected into the gate/drain overlap region of the gate under GIDL stress. The trapping of holes in the oxide is dominant in the first stage, but that of electrons in the oxide is dominant in the second stage. The change of GIDL current under GIDL stress is due to the common effects of edge direct tunneling and band-to-band tunneling.

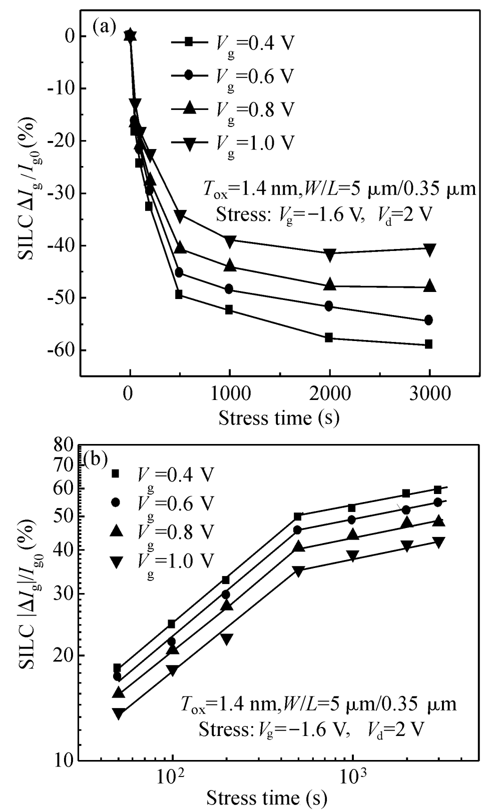

Fig. 7. Time evolution of SILC at different measured gate voltages under GIDL stress in NMOSFET: (a) Linear–linear scale; (b) log–log scale.

In order to further investigate the effect of GIDL stress on the damage of device, SILC is also been monitored during stress. We suppose $(I_g - I_{g0})/I_{g0}$ as the SILC, where I_g is the gate leakage current measured from the interruption of stresses, and I_{g0} is the initial gate leakage current. Figure 6 shows the time evolution of SILC measured at different positive gate voltage under GIDL stress in LDD NMOSFET. SILC in the NMOSFET decreases with increasing stress time and also gets saturated after a long stress time as shown in Fig. 7(a). SILC is strongly dependent on the measured gate voltage. The higher the measured gate voltage, the less serious the degradation of the gate current. The time evolution of SILC in the log–log scale under GIDL stress in NMOSFET is drawn in Fig. 7(b). The degradation slope of SILC becomes smaller with increasing stress time. The SILC degradation shows the saturating time dependence. Figure 8 shows the gate current as a function of the gate voltage before and after GIDL stress for 1.4 nm-thick gate oxide. It is also clearly found that the SILC decreases with the stress time.

Figure 6 also shows two likely origins of the gate current under GIDL stress: electrons tunneling through the oxide to the drain due to edge direct tunneling and holes injection created from the band-to-band tunneling over the oxide to the gate. In the early stage of GIDL stress, a fraction of the holes created from the band-to-band tunneling inject into the gate oxide. Some neutral traps are generated by the hole injection. Meanwhile, these holes can also be trapped by the

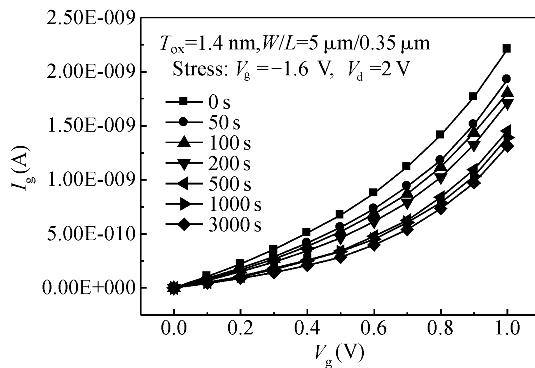

Fig. 8. Time evolution of SILC under GIDL stress in NMOSFET.

neutral traps. The SILC is measured at constant, low, positive voltages after GIDL stress. During the measurement of SILC, electrons can emit from the inverted channel. These electrons can be neutralized by the holes trapped into the neutral traps. At the same time, some of the electrons also can be trapped by the neutral traps and prevent electrons emitting from the inverted channel. So SILC decreases with stress time in the first state. In the last stage of GIDL stress, electrons tunneling from the gate are dominant. Some electrons can be trapped in the oxide finally and become oxide trapped negative charges. During the measurement of SILC, the oxide trapped negative charges can prevent electrons tunneling through the oxide by enhancing the barrier height and lowering the electric field in the oxide. So SILC also decreases with stress time in the last state. In the first state, electrons from the inverted channel not only can be neutralized but also can be trapped. Therefore, the degradation of SILC is more serious. When the measured gate voltage is higher, electrons from inverted channel can emit toward the gate more easily. Then the higher the measured gate voltage, the less serious the degradation of the gate current.

4. Conclusion

In summary, the degradation of devices has been investigated in detail under GIDL stress in this paper. Firstly, the degradation of device parameters is presented. Experimental result shows that the degradation of device parameters depends more strongly on V_d than on V_g. We mainly focus on the effects of GIDL stress on GIDL current and SILC. The damage is investigated through the analysis of GIDL current. From GIDL current evolution before and after GIDL stress, it is found that the change of GIDL current can be divided into two stages. The trapping of holes in the oxide is dominant in the first stage, but that of electrons in the oxide is dominant in the second stage. This is due to the common effects of edge direct tunneling and band-to-band tunneling. SILC in the nMOSFET decreases with increasing stress time under GIDL stress. The degradation characteristic of SILC shows the saturating time dependence. SILC is strongly dependent on the measured gate voltage. The higher the measured gate voltage, the less serious the degradation of the gate current. A likely mechanism is presented to explain the origin of SILC during GIDL stress.

References

[1] Yang K N, Huang H T, Chen M J, et al. Characterization and modeling of edge direct tunneling (EDT) leakage in ultrathin gate oxide MOSFETs. IEEE Trans Electron Devices, 2001, 48(6): 1159

[2] Yoshida E, Tanaka T. A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory. IEEE Trans Electron Devices, 2006, 53(4): 1159

[3] Semenov O, Pradzynski A, Sachdev M. Impact of gate induced drain leakage on overall leakage of submicrometer CMOS VLSI circuits. IEEE Trans Semicond Manuf, 2002, 15(1): 9

[4] Chang M, Lin J, Shih S N, et al. Impact of gate-induced drain leakage on retention time distribution of 256 Mbit DRAM with negative wordline bias. IEEE Trans Electron Devices, 2003, 50(4): 1036

[5] Kim I, Choi S, Choi J, et al. Real impact of dynamic operation stress during burn-in on DRAM retention time. IEEE Trans Electron Devices, 2004, 51(4): 603

[6] Park K H, Han K R, Kim Y M, et al. Simulation study of high-performance modified saddle MOSFET for sub-50-nm DRAM cell transistors. IEEE Electron Device Lett, 2006, 27(9): 759

[7] Chen H F, Hao Y, Ma X H, et al. Characteristic s of degradation under GIDL stress in ultrathin gate oxide LDD nMOSFET's. Acta Physica Sinica, 2007, 56(3): 1662 (in Chinese)

[8] Chen H F, Hao Y, Ma X H, et al. Investigation of the characteristics of GIDL current in 90 nm CMOS technology. Chin Phys Soc, 2006, 15(3): 645

[9] Choi C H, Nam K Y, Yu Z, et al. Impact of gate direct tunneling current on circuit performance: a simulation study. IEEE Trans Electron Devices, 2001, 48(12): 2823

[10] Yeo Y C, Lu Q, Lee W C, et al. Direct tunneling gate leakage current in transistors with ultrathin silicon nitride gate dielectric. IEEE Electron Device Lett, 2000, 21(11): 540

[11] Lo G Q, Kwong D L. Roles of electron trapping and interface state generation on gate-induced drain leakage current in p-MOSFETs. IEEE Electron Device Lett, 1991, 12(12): 1745

[12] Cheng K, Lyding C Y. Corrections to "An analytical model to project MOS transistor lifetime improvement by deuterium passivation of interface traps". IEEE Electron Device Lett, 2003, 24(11): 1745