An RF power amplifier with inter-metal-shuffled capacitor for inter-stage matching in a digital CMOS process

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Abstract: One challenge of the implementation of fully-integrated RF power amplifiers into a deep submicro digital CMOS process is that no capacitor is available, especially no high density capacitor. To address this problem, a two-stage class-AB power amplifier with inter-stage matching realized by an inter-metal coupling capacitor is designed in a 180-nm digital CMOS process. This paper compares three structures of inter-metal coupling capacitors with metal-insulator-metal (MIM) capacitor regarding their capacitor density. Detailed simulations are carried out for the leakage, the voltage dependency, the temperature dependency, and the quality factor between an inter-metal shuffled (IMS) capacitor and an MIM capacitor. Finally, an IMS capacitor is chosen to perform the inter-stage matching. The techniques are validated via the design and implement of a two-stage class-AB RF power amplifier for an UHF RFID application. The PA occupies $370 \times 200\ \mu m^2$ without pads in the 180-nm digital CMOS process and outputs 21.1 dBm with 40% drain efficiency and 28.1 dB power gain at 915 MHz from a single 3.3 V power supply.

Key words: power amplifiers; radio frequency amplifiers; UHF amplifiers; RFID; digital CMOS process
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1. Introduction

SOC solutions of wireless devices are attractive owing to a higher benefit from scaled CMOS technology. Nowadays, the multi-chip in a package solution is also popular but generally undesirable in terms of cost, form factor, and power consumption. As CMOS technology is scaled down to deep submicro minimum feature sizes, CMOS technology shows its ability to compete with other expensive technologies at radio frequency. However, the scaling trend also causes many challenges in the realization of a fully-integrated CMOS RF power amplifier (PA). One of them, in particular, is how to realize a high density capacitor for the PA inter-stage matching when more metal layers are used in a digital CMOS process.

Besides a special process high density capacitor[1, 2], one special paper tried a fractal capacitor[3], but this capacitor is quite complicated to generate and handle. Several papers have tried to construct novel interconnection based capacitors, which used coupling effects between metal layers to realize the capacitor, such as a metal sandwich capacitor, a pillar capacitor, a ring capacitor, and an inter-metal shuffled (IMS) capacitor[4]. An IMS capacitor shows the best performance for the capacitor density. For a five-layer metal of a standard 180 nm digital CMOS process, 0.7 fF/μm^2 capacitor density is gained with an IMS capacitor compared to 1 fF/μm^2 for the metal–insulator–metal (MIM), which needs additional layers and operations during manufactory, and, besides, these layers are not provided in a digital process. As the process advances into the deep sub-micro range, more metal layers will be implemented. A high density capacitor of interconnection will be used in a digital process to accelerate RF block shrinkage and integration with other parts.

In this paper, interconnection based capacitors are introduced. Comparisons between an interconnection based capacitor and a standard MIM capacitor, which were provided by a foundry, are shown. A class-AB power amplifier with an IMS capacitor is also designed.

2. Interconnection based capacitors

According to the electric field direction between two nodes, three types of interconnection based capacitors are introduced. There are vertical electric field capacitors (VEFC), lateral electric field capacitors (LEFC) and radiative electric field capacitors (REFC).

Detailed structures of each type will be illustrated with diagrams. In all the figures, the grey and black color stands for two nodes of each capacitor. Using layout and post layout simulations, we give a performance summary.

2.1. VEFC

The VEFC derives its name from the different nodes, which are placed up and down, thus, making the electric field line also go upward or downward.

In a VEFC, the most conventional capacitor is a multi-plate parallel plate capacitor called metal sandwich capacitor, as shown in Fig. 1, which makes an odd number of plates connected together to stand for one node and an even number of plates for another node. Although it is easy to construct and model, the capacitor density of this type is influenced only by parameters of the oxide layer between adjacent metal plates. Because the oxide layer changed little during process generations, the metal sandwich capacitor density does not scale up withshrinking technology.Theconventional typeis not suitable

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Fig. 1. Metal sandwich capacitor.

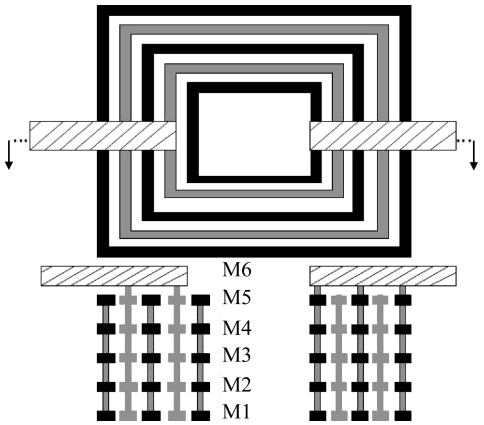

Fig. 2. Ring capacitor.

for deep submicro technology.

2.2. LEFC

The LEFC has different nodes placed side by side, which causes the electric field lines follow a lateral direction.

In an LEFC, a ring capacitor is most frequently used. Several concentric rectangular rings, which are formed with vertical connected metal lines and vias, construct the capacitor in a way of forming adjacent rings with minimum space. In Fig. 2, M1–M5 along with VIA1–VIA4 form the rings and two M6 lines connect different nodes of the capacitor. Again, the adjacent plates stand for different nodes. Connecting M1–M5 all around the same vertical node will increase the capacitor density by 20%[4], ideally compared with only doing so with M6 contact. Rather than having enclosed rings, we can have alternating stripes of metal to derive the inter-metal finger capacitor in Fig. 3.

2.3. Radiative electric field capacitor (REFC)

The basic rule to construct an REFC capacitor is to place one node around the other node. In this case, more electric lines emitted from one node will end at another node than in other cases, which will enhance the capacitor density.

In REFC, the IMS capacitor in Fig. 4 has a better trade-off between the capacitor density and the realization difficulty than the previous two types. Besides, the IMS capacitor density will scale up easily and effectively with the technology scaling down. A new technology will make stripes in Fig. 4,

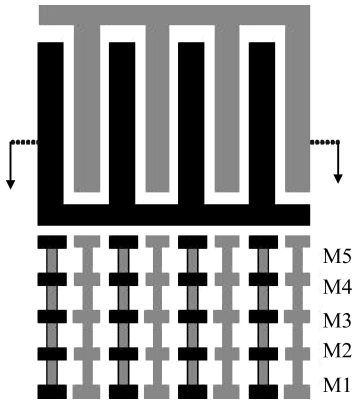

Fig. 3. Inter-metal finger capacitor.

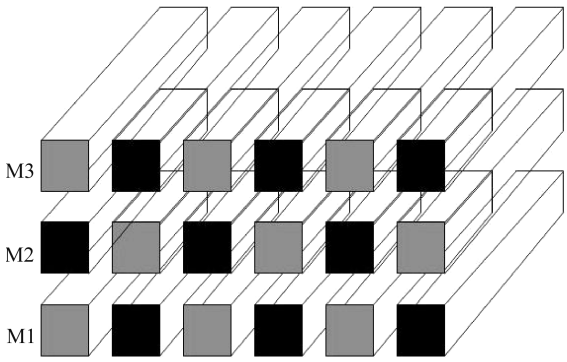

Fig. 4. Inter-metal shuffled capacitor.

Table 1. Capacitor density summary of three types of capacitors and a standard MIM capacitor.

Capacitor type	Hand calculated (fF/μm^2)	Post layout extracted (fF/μm^2)
Metal sandwich	0.23	0.21
Ring	0.65	0.59
Finger	0.41	0.33
IMS	0.71	0.70
Standard MIM	0.96	1.05

which are closer in the lateral direction. For the vertical direction, more metal layers will be used and the capacitor density will be higher.

2.4. Comparison of capacitors

Table 1 gives the capacitor density of several typical interconnection based capacitors. For comparison, the capacitor density of a standard MIM capacitor is listed.

As shown in Table 1, the ring capacitor and the IMS capacitor have a better capacitor density. Considering the scaling trend, more metal layers will be used. The IMS capacitor will be improved if two-dimension electric fields are used. Besides, the IMS capacitor will be denser than the standard MIM capacitor in a more advanced process. So, the IMS capacitor is chosen to be compared with the MIM capacitor regarding its current leakage, the temperature and voltage dependence, the quality factor, and the parasitic capacitance.

Figure 5 shows that the IMS capacitor has a lower leakage current than the MIM capacitor because the silicon dioxide in the IMS capacitor has a better isolation than the silicon

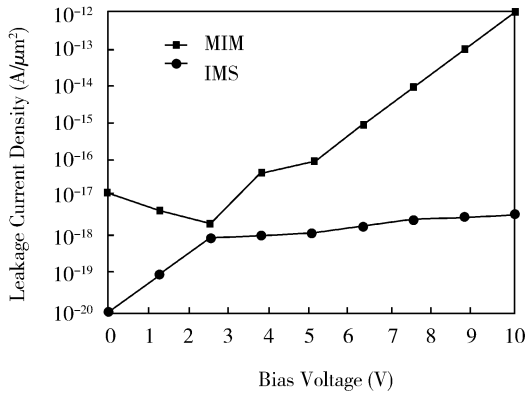

Fig. 5. Leakage current density versus voltage for an IMS and an MIM capacitor.

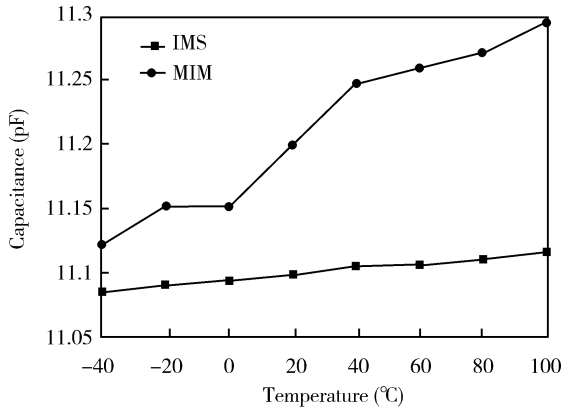

Fig. 6. Capacitance versus temperature for IMS and MIM.

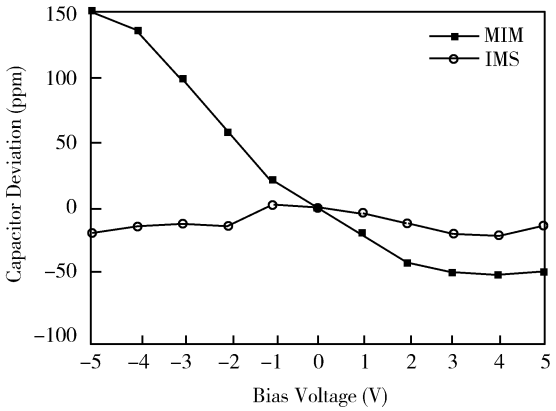

Fig. 7. Capacitance deviation versus bias voltage for the IMS and the MIM.

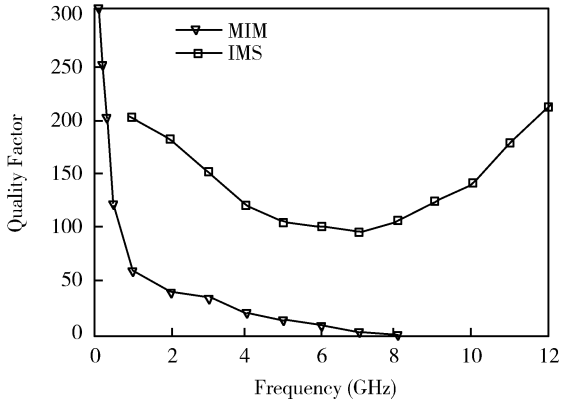

Fig. 8. Quality versus frequency for IMS and MIM.

nitride in the MIM capacitor. Besides, the dielectric constant of the former is 6–8, while for the latter it is 4.5, and both plates of the MIM structure are closer than for the IMS type. When biasing IMS and MIM capacitors at a voltage lower than 2 V at 25 °C, the leakage current density of the IMS is less than 4×10^{-19} A/μm^2, which is at least eight times lower than that of the MIM. When the high bias voltage increases to 10 V, the leakage of the MIM rises exponentially, while that of the IMS stays below 4×10^{-18} A/μm^2. As for the leakage performance, the IMS structure is superior to the MIM type.

The IMS capacitors show a lower voltage and temperature dependency than the MIM capacitors in Figs. 6 and 7. As shown in Fig. 6, the temperature coefficient is about 100 ppm/°C for the MIM capacitor, while it is 22.5 × 100 ppm/°C for the IMS capacitor. As shown in Fig. 7, the capacitance deviation of the IMS is much lower than that of the MIM. Varying the bias voltage from –5 to 5 V, the deviation of the IMS is within 25 ppm, whereas it is 150 ppm for the MIM type. So, the IMS capacitor has a better linearity than the MIM capacitor.

Figure 8 compares the quality factor at different frequencies of IMS and MIM capacitors. The results show that the IMS capacitor has a quality factor of more than 100 up to a frequency of 10 GHz, whereas the Q value of an MIM capacitor drops to less than 40 at 2 GHz and approaches zero at 8 GHz because of the self resonance. The quality factor of the IMS capacitor is affected by the layout style, the structure, and the metal layers used in the design. Reducing the capacitor unit will reduce the series resistor and increases the resonance frequency. The upper metal layer has a lower capacitance effect with the substrate, so a high quality factor can be achieved at higher frequencies. Placing the IMS capacitor in a full layout with a proper area and with proper shielding will allow for a higher resonance frequency.

Although the MIM shows a better performance with regard to capacitor density, process variation, parasitic capacitance, and matching[5], the IMS is a better choice with respect to cost, temperature coefficient, voltage coefficient, leakage, and quality factor at high frequencies and self-resonant frequencies. As for the inter-stage matching capacitor in an RF power amplifier realized in a 180-nm digital CMOS process with no MIM mask layer, the IMS capacitor is a good candidate to replace the MIM capacitor.

3. Class AB RF power amplifier with IMS capacitor

The prototype power amplifier in Fig. 9 is a two-stage configuration with an inter-stage matching capacitor, C_INTER, realized with an IMS capacitor. We use a standard 180-nm CMOS process for the PA design. Thick-oxide devices, commonly used for the pad design in a 180-nm process, are used as cascode devices, MOSFET2 and MOSFET3, to enhance the drain-source breakdown voltage. The common source transistors are thin-oxide devices, which are used to maximize G_m, to minimize the transistors area, and the parasitic parameter. A drain voltage (V_DC) of 3.3 V is used for

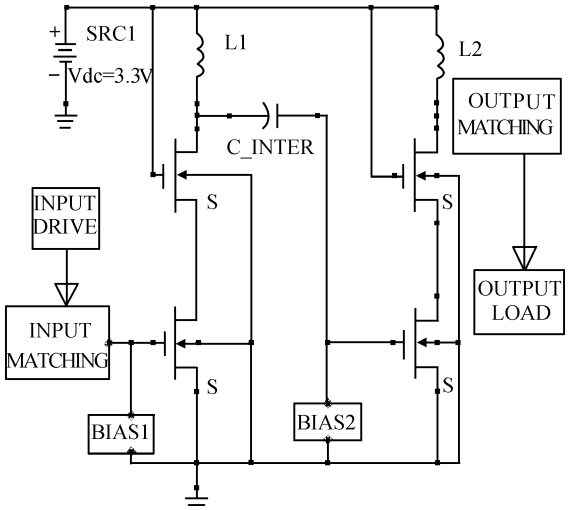

Fig. 9. Schematic of the two-stage class-AB power amplifier.

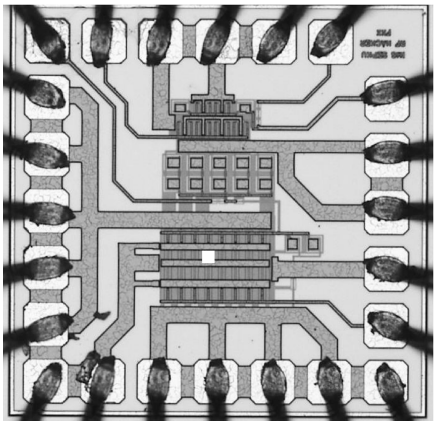

Fig. 10. Die photo of the two-stage power amplifier.

both stages. The driver stage transistor is designed with a total gate width of 128 μm (MOSFET1) while the output-stage transistors have a size of 1024 μm (MOSFET4).

The matching networks and the two RF chokes are designed to be external. Load-pull and source-pull simulations are performed to find out the optimum matching impedance. As for the output impedance matching, the network is to transfer a 50 Ω load to a 23 + j15 Ω load, which is the optimum impedance for an output stage at a 22.1 dBm power output having a 1 dB compression point. At the same time, the input matching network is to transfer a 50 Ω source impedance to the conjugate of the input impedance of the drive stage and most of the power delivered is absorbed by the gate of MOSFET1. RF chokes L1 and L2 are placed externally to achieve a lower resistance and to make them adjustable.

C_INTER is the only capacitor realized on the chip. To match the output impedance of the drive stage to the input impedance of the output stage, L1 and C_INTER form an LC network. Here, C_INTER is an IMS capacitor used to replace the commonly used MIM capacitor, which needs an additional mask.

4. Result and discussion

The total die area without pads is $370 \times 200\ \mu m^2$, where the 8 pF IMS capacitor occupies $70 \times 200\ \mu m^2$ and acts as an inter-stage matching capacitor. Figure 10 shows a die photo of the proposed power amplifier.

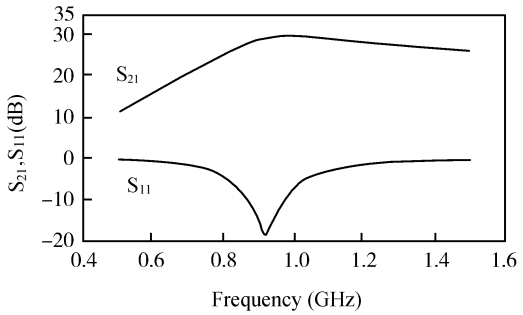

Fig. 11. S_{11} and S_{21} of the power amplifier.

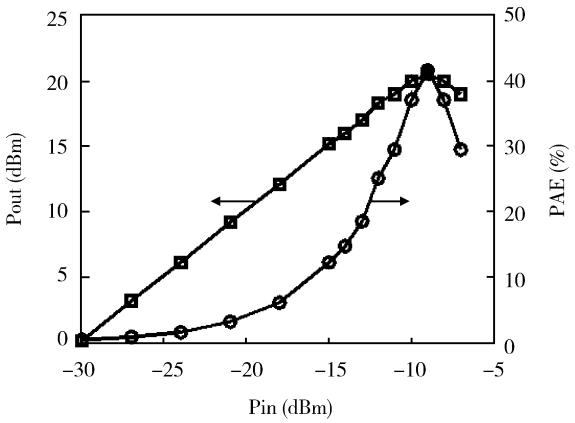

Fig. 12. Output power and PAE.

Figure 11 shows the S parameter measurements of the designed class AB RF power amplifier with an N5230A network analyzer. The small signal gain is 31 dB, while the input S_{11} is lower than –15 dB in the band from 902 to 928 MHz, which is the US ISM band for a UHF RFID application. The power gain of DUT reduces to 28.1 dB because of the class-AB operation.

A difference in the S_{11} parameter of 8 dB has been observed between simulated and measured results. The main cause is that the parasitic parameter affects the input impedance. Besides, simulation models of external components used for input matching are not so accurate. All these could be optimized by fine tuning steps and by the setup of a new simulation model according to the test results.

A 3.5 dB drop in the small signal gain is observed after the first measurement. This comes from the inaccurate inter-stage matching function. This could be optimized by tuning the choke of the driver to some degree. After tuning, S_{11} is improved by 2 dB.

Figure 12 shows the output power and the power added efficiency (PAE) measurement results. The output power shows a 1 dB compression point at 21.1 dBm with a power gain of 28.1 dB, which is less than the small signal gain of 2.9 dB. The maximum PAE is 40%,when compressed.

5. Conclusion

Different types of inter-metal capacitors are compared. An IMS capacitor is chosen to realize the inter-stage matching

capacitor of the power amplifier. To demonstrate if the IMS capacitor is suitable to replace the commonly used MIM capacitor, a two-stage class-AB power amplifier for a 900-MHz RFID application is designed and implemented in a 180-nm digital CMOS process. It has an output power of 21.1 dBm with a power gain of 28.1 dB and a 40% drain efficiency from a single 3.3 V power supply. The measurement results show that the IMS capacitor is a good candidate for deep submicro radio frequency applications and will show a higher potential as the technology is scaling down.

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