Annealing behavior of radiation damage in JFET-input operational amplifiers

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Abstract: The elevated and room temperature annealing behavior of radiation damage in JFET-input operational amplifiers (op-amps) were investigated. High- and low-dose-rate irradiation results show that one of the JFET-input op-amps studied in this paper exhibits enhanced low-dose-rate sensitivity and the other shows time-dependent effect. The offset voltage of both op-amps increases during long-term annealing at room temperature. However, the offset voltage decreases at elevated temperature. The dramatic difference in annealing behavior at room and elevated temperatures indicates the migration behavior of radiation-induced species at elevated and room temperatures. This provides useful information to understand the degradation and annealing mechanisms in JFET-input op-amps under total ionizing radiation. Moreover, the annealing of oxide trapped charges should be taken into consideration, when using elevated temperature methods to evaluate low-dose-rate damage.

Key words: JFET-input operational amplifiers; dose rate; radiation damage; annealing behavior
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1. Introduction

Junction field effect transistors (JFETs) have high impedance, low input offset voltage parameters, such as offset voltage and offset current, and other advantages; so, they typically act as the input stage of operational amplifiers (op-amps). JFET-input op-amps are known to be fairly immune with regard to the total dose of radiation exposure. However, JFET-input op-amps were found to be sensitive to the dose rates, especially low dose rates[1,2]. That is to say, JFET-input op-amps may exhibit more degradation in a low-dose-rate environment, called enhanced low-dose-rate sensitivity (ELDRS). Enhanced damage under low-dose-rate radiation includes two types of degradation mechanisms. One is "true" degradation enhancement occurring at low-dose-rate irradiation. The enhanced damage cannot be estimated after high-dose-rate irradiation followed by long-term annealing at room temperature. The other is "untrue" damage enhancement, called time-dependent-effect (TDE). The only difference between ELDRS and TDE is whether the damage induced by a high or low dose rate can be eliminated by room-temperature annealing.

Because of the damage induced by low dose rates, the application of JFET-input op-amps is limited to environments with dose rates of about 10^{-2}–10^{-4} rad(Si)/s. However, the accelerated testing dose rates are usually 50–300 rad(Si)/s in the laboratory. The radiation damage induced under laboratory dose rates is not conservative for JFET-input op-amps. Thus, doing all studies under these lab conditions can lead to reliability problems for JFET-input op-amps operating at low-dose-rate environment. Thus, developing a suitable accelerated evaluation method for JFET op-amps becomes necessary. However, a good accelerated evaluation method must be based on clear damage mechanisms of JFET-input op-amps. Therefore, this paper provides useful information on the damage and the annealing mechanisms by comparing the annealing behavior of JFET-input op-amps at elevated and room temperatures.

2. Experiments and methods

2.1. Samples and measurement

The experimental samples are pJFET (p-channel JFET)-input op-amps, LF353 and TL062, which are shown in Table 1 in detail. The schematic structure of the p-JFETs is shown in Fig. 1. Irradiation was performed at 50 rad(Si)/s and 13 mrad(Si)/s. The bias board was placed in a lead/aluminum (Pb/Al) container that was made according to the military standard (MIL–STD).

The static parameters of the op-amps were measured before and after irradiation by a Tektronix 577 curve tracer. These parameters included the input offset voltage, the bias current and the common-mode rejection ratio (CMRR). The input offset voltage was found to be sensitive to the total dose.

2.2. Experimental methods

The methods used in our experiments include room-temperature annealing and MOS accelerated test methods. During room-temperature annealing, JFET-input op-amps

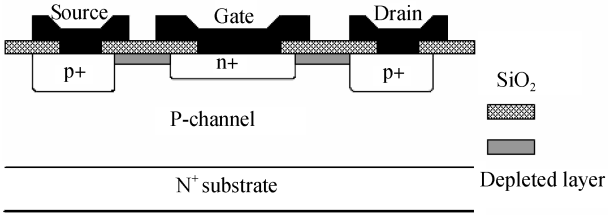

Fig. 1. Schematic illustration of the p-channel JFET and the radiation-induced inversion layer.

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Table 1. Summary of the devices being tested.

Op-amps	Code	Input stage	Description	Manufacturer
LF353	52A402M	pJFET	Dual op-amp	Texas Instruments
TL062	27C3Y9M	pJFET	Dual op-amp	Texas Instruments

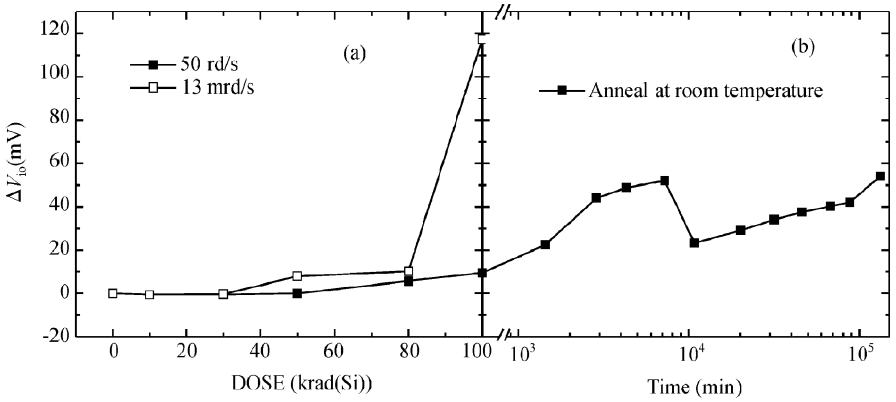

Fig. 2. ΔV_{io} versus (a) total dose and (b) room-temperature annealing time for LF353.

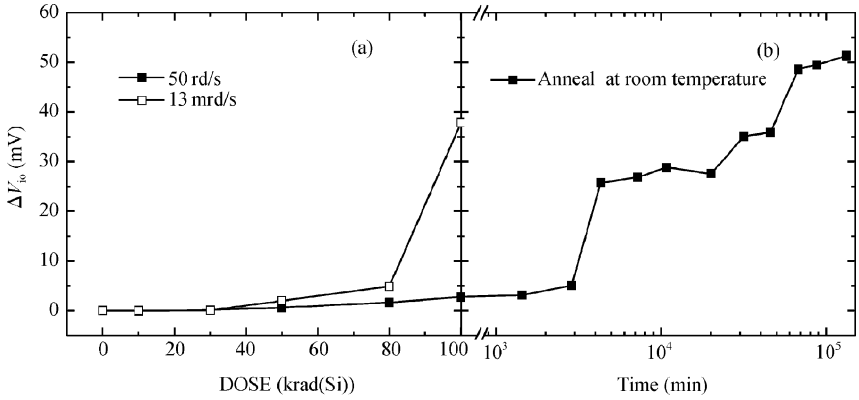

Fig. 3. ΔV_{io} versus (a) total dose and (b) room-temperature annealing time for TL062.

irradiated at a high dose rate were kept at room temperature for almost three months to observe the annealing behavior. The annealing time was the same as that needed at 13 mrad(Si)/s, and the biasing conditions during annealing were the same with irradiation. Due to the parasitic MOSFET in JFET structures, a MOS accelerated annealing testing method, which has been proposed in MIL-STD-883G, TM1019.7, was used to evaluate the damage of the JFET-input op-amps. The method used in our experiments consisted of three steps. First, the experimental samples were irradiated with a total dose of 100 krad(Si) at a relatively high dose rate of 50 rad(Si)/s. Second, they were annealed at room temperature for 24 h, and, finally, annealed at 100 °C for 168 h after an additional exposure to half the total dose.

3. Results

3.1. Annealing at room temperature

Figures 2 and 3 illustrate the change in input offset voltage (ΔV_{io}) of LF353 and TL062 as a function of the accumulated total dose and the room-temperature annealing time, respectively. From Figs. 2(a) and 3(a), we can see that ΔV_{io} only slightly increases at a high dose rate, while a sharp increase occurs when the samples are irradiated at a low dose with a total dose larger than 80 krad(Si). From these figures, we can also see that the ΔV_{io} value of LF353 is three times larger than ΔV_{io} of TL062 when irradiated with 100 krad(Si) at a low dose rate. This shows that LF353 is more sensitive to low dose rates. It can be concluded from the radiation responses that both JFET-input op-amps exhibit more damage at low dose rates, and the damage of LF353 is greater than that of TL062 under low-dose-rate irradiation.

Furthermore, there are differences in the annealing response for LF353 and TL062, as shown in Figs. 2(b) and 3(b). As for LF353, ΔV_{io} is not always increasing, and there is a decrease in the middle of the annealing time. Finally, ΔV_{io} still could not reach the level obtained at low dose rate. However, ΔV_{io} always keeps increasing for TL062, and the final damage level is greater than in the low-dose-rate case. Although there are several differences in the annealing responses, ΔV_{io} always keeps increasing during room-temperature annealing for both op-amps. This is different from the high-temperature annealing response that will be discussed below. We can obtain that LF353 exhibits ELDRS effect, while TL062 shows TDE from the experimental results above. The room-temperature annealing trend is towards to more damage, and ΔV_{io} always keeps

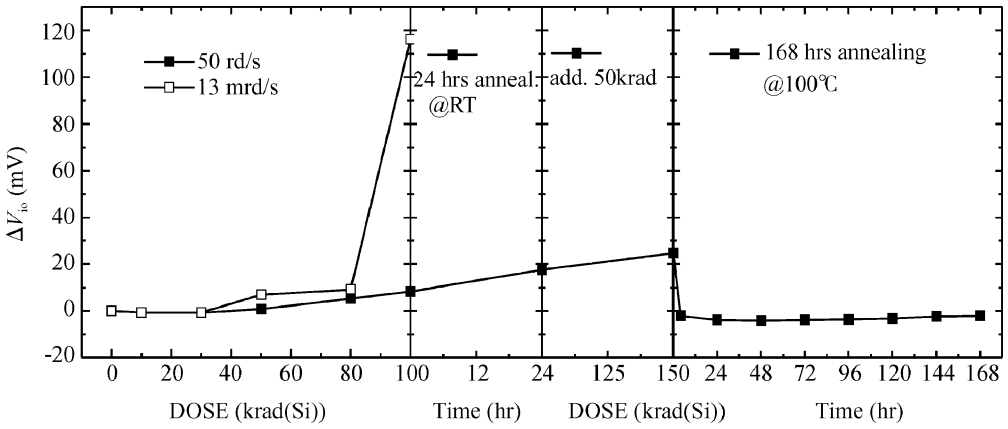

Fig. 4. MOS accelerated annealing testing results of LF353.

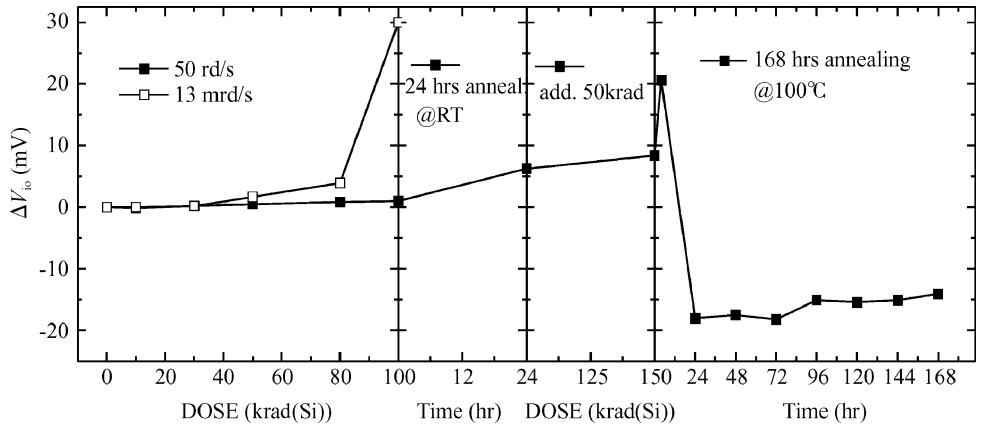

Fig. 5. MOS accelerated annealing testing results of TL062.

positively increasing.

3.2. MOS accelerated annealing

According to the accelerated annealing test method mentioned in section 2.2, Figures 4 and 5 illustrate the radiation and annealing response of LF353 and TL062. It can be seen from these figures that more damage is caused by low-dose-rate irradiation than by a high dose rate, which is consistent with the above results. Furthermore, after annealing at room-temperature and an additional 50 krad(Si) exposure, ΔV_{io} of both op-amps slightly increases.

However, after annealing at 100 °C for 168 h, the behavior of LF353 and TL062 is different. As for LF353, V_{io} initially drops within the first 24 hours and stays almost constant afterwards. The final V_{io} is much less than that at low dose rate. However, for TL062 op-amps, V_{io} increases at the beginning of the annealing process, and then decreases. The final value of V_{io} is closer to the damage level under low-dose-rate irradiation but does not reach it, comparing with that of LF 353 op-amps. Moreover, the behavior of V_{io} is consistent with that of the LF353 op-amps, i.e., V_{io} almost keeps unchanged after 24 h. Therefore, severe changes of V_{io} occur in the initial 24 hours of the 168 hours elevated annealing procedure. From the MOS accelerated annealing test results in Fig. 5, we can conclude that the method is a proper way to evaluate the low-dose-rate damage of JFET-input op-amps, which show time-dependent effect.

4. Discussion

The offset voltage (V_{io}) shows the unmatched level of dual junction field effect transistors in op-amps. Because the characteristics of dual JFETs in op-amps could not be made precisely controlled during the fabrication process, V_{io} cannot be avoided. When fabricating JFETs, the thick LOCOS silicon-dioxide usually acts as a spacer layer. Like the isolation oxide layer in discrete bipolar transistors, the electric field in the thick spacer oxide of the gate-source/drain regions in JFET is very weak[2]. When this type of device is exposed to radiation, electron-hole pairs are produced in the spacer oxide layer. After the initial recombination[3], electrons and holes will migrate in opposite directions under the influence of the weak electric field. Due to the slower mobility[4], holes may be trapped by the defects near or at the Si/SiO_2 interface. This can form oxide trapped charges and interface trapped charges, respectively[5]. Both of them can cause the p-type silicon to deplete or even to invert[6], as shown in Fig. 1. The depleted layer can decrease the effective thickness of the carrier channels in JFETs. Therefore, the *I–V* curves of JFETs would change after irradiation, suggesting a shift of V_{GS}. The offset voltage can be expressed as

$$V_{io} = V_{GS1} - V_{GS2}, \tag{1}$$

where V_{GS1} and V_{GS2} are the gate-to-source voltages of $JFET_1$ and $JFET_2$ in op-amps, respectively. Due to the differences in dual JFETs, the shift of V_{GS} induced by irradiation would be

different. V_{io} represents the relative changes of V_{GS1} and V_{GS2} caused by irradiation. According to Eq. (1), V_{io} can be written as[2]

$$\Delta V_{io} = \Delta V_{GS1} - \Delta V_{GS2}. \quad (2)$$

As discussed above, ΔV_{io} indicates a difference in trapped charge (more net trapped charge) between the dual JFETs in op-amps. When more net trapped charge is induced by irradiation, ΔV_{io} would increase. An increase or decrease of ΔV_{io} only indicates which JFET has more trapped charges. The enhanced low-dose-rate damage can be interpreted as a migration of holes and electrons. During high-dose-rate irradiation, a large amount of holes would be trapped in the thick spacer oxide, forming a relatively strong space field. This electric field could apparently retard the transport of holes. However, the space field will be weaker in the low-dose-rate case. More holes and H^+-ions would migrate to the Si/SiO_2 interface, where they may be trapped[5]. Therefore, both V_{GS1} and V_{GS2} will have more shifts. Due to the different characteristics of dual JFETs in op-amps, more charges would be trapped in a JFET at low dose rates[7], causing a larger V_{io}. An increase of V_{io}, as shown in Figs. 2(a) and 3(a), suggests that more net charges would be trapped in $JFET_1$.

The annealing performance of JFETs can be attributed to the temperature-sensitive migration behavior of holes. During room-temperature annealing, a larger ΔV_{io} in Figs. 2(b) and 3(b) suggests more net trapped charges in $JFET_1$. The decline in Fig. 2(b) may imply that the net trapped charges become fewer in $JFET_1$ than in $JFET_2$. Although the interface trapped charges would increase in during the drop, the annealing rate of oxide trapped charges would be greater than the generation rate of interface trapped charges. As a result, there will be fewer net charges between $JFET_1$ and $JFET_2$. This decline of ΔV_{io} can also indicate that oxide trapped charges in the JFETs in the LF353 op-amps are easier to anneal than those in TL062 op-amps, showing a lower activation energy in the spacer oxide in LF353 op-amps. Thus, radiation damage in the dual JFETs of the LF353 is easier to recover. This may induce a lower damage difference between the dual JFETs, showing a decrease in ΔV_{io}. Although oxide trapped charges are difficult to reduce for the JFETs in TL062, the generated interface trapped charges are more than the annealed oxide trapped charges. There could be more net trapped charges between the dual JFETs in TL062. And this can result in a gradual increase in V_{io}. The positive trend for room-temperature annealing, as shown in Figs. 2(b) and 3(b), tells us that the generation rate of interface trapped charges in $JFET_1$ is greater than that in $JFET_2$.

Unlike for room-temperature annealing, a decrease of ΔV_{io} is observed in Figs. 4 and 5 at elevated temperatures. This indicates more net trapped charges in $JFET_2$ but not in $JFET_1$. At elevated temperatures, radiation-induced mobile species, such as holes and H^+, have a higher diffusivity. This allows these species to migrate to the Si/SiO_2 interface region in a short time and be trapped there. It is known that the annealing temperature of interface trapped charges is more than 100 °C, while oxide trapped charges would anneal at room temperature[4]. Therefore, the generation rate of interface trapped charges of $JFET_2$ is greater than that of $JFET_1$ at elevated temperatures. This can induced more net tapped charges in $JFET_2$, causing V_{io} to become negative. The increase in V_{io} of TL062 shows that more net trapped charges would be trapped in $JFET_1$ at the beginning of the annealing process. There is no increase in LF353 at elevated temperature. This should be related to the easier annealing in $JFET_1$ of LF353, as discussed for room-temperature annealing. Due to the easier annealing in JFETs of LF353, the V_{io} value of TL062 after elevated temperature annealing is greater than V_{io} for LF353. The oxide trapped charges also anneal faster while more interface trapped charges are formed[7]. So, JFETs in op-amps would recover to some extent, reducing the level mismatch between dual JFETs. As a result, V_{io} after MOS elevated temperature annealing is much less than after room-temperature annealing for both op-amps. Although net trapped charges can be caused in a short time at elevated temperature, the annealing of oxide trapped charges should be considered when using the MOS accelerated testing method to evaluate the radiation damage at low dose rate. Therefore, a margin factor might be needed. For example in the TL062 evaluation, the factor is about 2. Furthermore, lateral or substrate PNP transistors are also used in the input stages in JFET-input op-amps. Their radiation and annealing response should also be taken into account. This needs further investigation.

5. Conclusions

The experimental results presented in this paper show that JFET-input op-amps exhibit an enhanced low-dose-rate sensitivity and a time-dependent effect (TDE). This may result from more net trapped charges in the spacer oxide under low-dose-rate irradiation, suggesting a more pronounced level mismatch in the two JFET transistors of the input stage of the op-amps.

The different behavior at elevated and room temperature demonstrates a different migration behavior of radiation-induced holes in the spacer oxide. There are more net trapped charges in $JFET_1$ after annealing at room temperature, showing a larger offset voltage after irradiation. However, more net trapped charges are trapped in $JFET_2$, as seen from the negative offset voltage when annealed at elevated temperature.

The MOS accelerated annealing test method should be suitable for op-amps, which exhibit TDE. Due to the annealing of oxide trapped charges at elevated temperature, a margin factor of about 2 should be taken into consideration for TDE op-amps. Meanwhile, for the lateral or substrate PNP transistors used in the circuitry the annealing of the oxide trapped charges should be taken into consideration.

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