A new level-shifting structure with multiply metal rings by divided RESURF technique*

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Abstract: A new structure of a lateral n-MOST and a new level-shifting structure with multiply metal rings (MMRs) by divided RESURF technique have been proposed. The device and electrical performances of the structure are analyzed and simulated by MEDICI. In comparison to the level-shifting structure with multiply floating field plates (MFFPs) used before, the structure stated here improves the reliability and diminishes the voltage difference between the voltage of the power supply of the high-side gate driver and the voltage of the output terminal of the level-shifting structure, which is also that of the input terminal of the high-side gate driver. The maximal voltage difference of the level-shifting structure in this paper is 30% lower than that used before. Therefore, good voltage isolation and current isolation are obtained. The structure can be used in the level-shifting circuit of various applications.

Key words: level-shifting; divided RESURF; multiple metal rings

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1. Introduction

A typical connection of the high voltage integrated circuit (HVIC) and the MOST half bridge is shown in Fig. 1. The high-side and low-side gate drivers supply the gate drive signals for M1 and M2. The HVM1 and HVM2 have the function of level-shifting and transmitting the drive signal from the control logic which is biased to the ground to the floating high-side gate driver which is biased to the terminal O. HVM1 transmits the on signal of the high-side gate driver, and HVM2 transmits the off signal. The level-shifting function is provided by utilizing HVM1, HVM2, R1 and R2.

There are two points to be considered in the level-shifting structure: (1) voltage isolation: the high voltage interconnections, H1 and H2, should be isolated to the high voltage junction terminal (HVJT) of the high-side gate driver and the drift region of HVM1 and HVM2; (2) current isolation: the currents from HVM1 to R1 and from HVM2 to R2 should be limited in the corresponding devices.

In the conventional level-shifting structure shown in Fig. 2(a), the high-voltage inter-connections are crossing over the HVJT of the high-side gate driver and the drift regions of HVM1 and HVM2. At these portions, electric shielding is required to avoid lowering of the breakdown voltage affected by the electric potential of the high voltage interconnections. Conventional shielding techniques forced HVICs to have increasing cost and process difficulties[1−7]. What is worse still, the maximum breakdown voltage is restricted by local high field and durability of the dielectric layer.

The above difficulty is solved by the self-shielding technique shown in Fig. 2(b)[8, 9]. In this technique, such problem could be ignored, because the high voltage interconnections are not crossing over any voltage sustaining region. However, there is a problem in this structure due to the existence of parasitic resistance which can cause undesirable leakage current parallel to the resistors of level-shifting structure, R1 and R2. As the parasitic resistance is unavoidable in the structure, it must be controlled to substantially high value for suppressing the power dissipation of self-shielding level-shifting circuit, so a large area of the self-shielding region is essentially needed[10].

In order to improve the abilities of current isolation of the level-shifting structure, the level-shifting technique called divided RESURF structure has been proposed in Ref. [10], shown in Fig. 2(c). In this structure, the simple pn junction isolation is used between the HVJT of the high-side gate driver and the high voltage n-MOSTs, HVM1 and HVM2. The H1 and H2 run over only a depleted p-sub region, so there is no need to reduce the electric field at the overlapping region. Thus, basically, there is no limit of level-shifting voltage in this structure. Furthermore, there is little leakage current due to pn

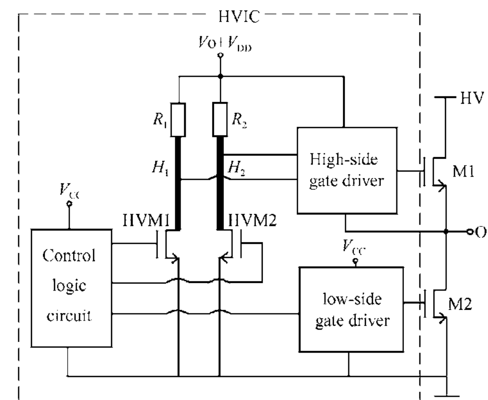

Fig. 1. Typical connection of HVIC.

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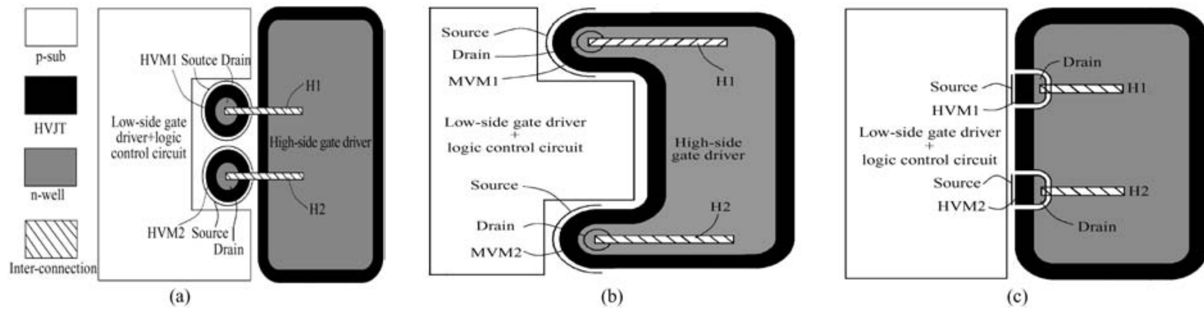


Fig. 2. Top view of HVIC: (a) Conventional structure; (b) Self-shielding structure; (c) Divided RESURF structure.

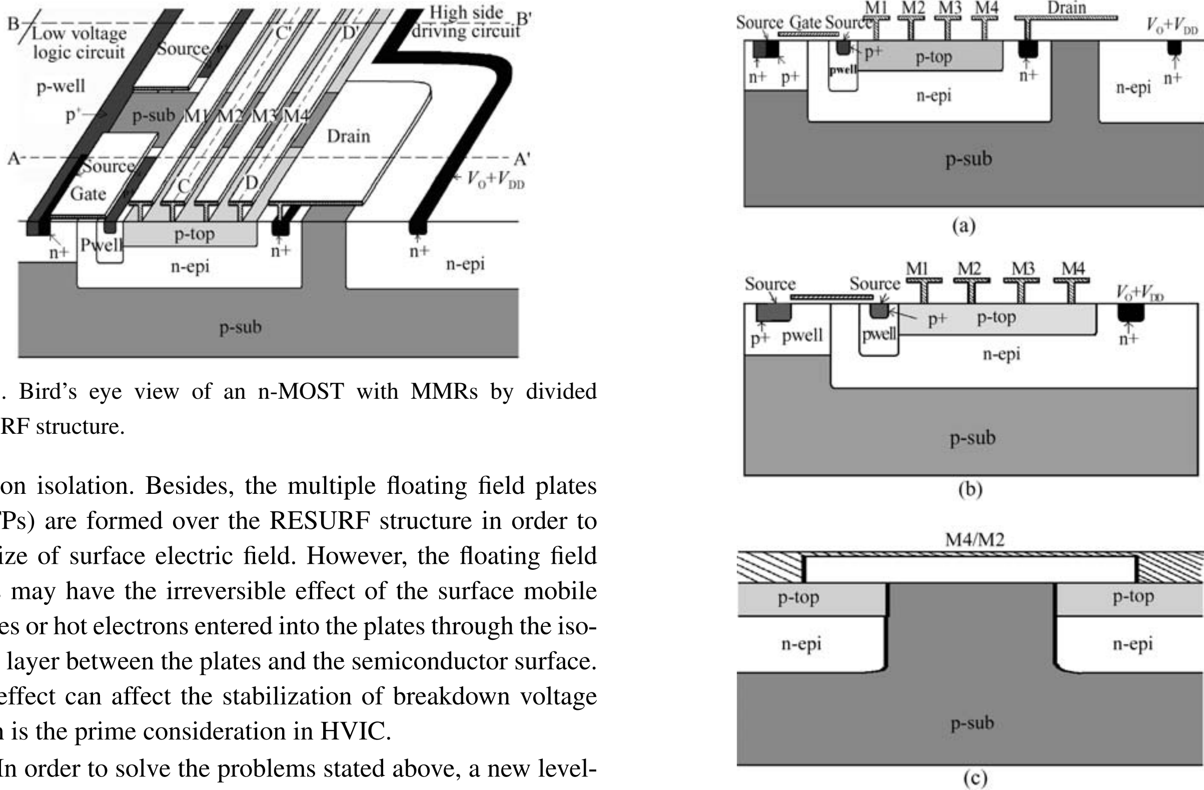


Fig. 3. Bird's eye view of an n-MOST with MMRs by divided RESURF structure.

Fig. 4. Cross-sections along the dashed lines in Fig. 3: (a) Cross-section of an n-MOST along the AA′; (b) Cross-section of the HVJT along the BB′; (c) Cross-section along the CC′ and DD′.

junction isolation. Besides, the multiple floating field plates (MFFPs) are formed over the RESURF structure in order to stabilize of surface electric field. However, the floating field plates may have the irreversible effect of the surface mobile charges or hot electrons entered into the plates through the isolation layer between the plates and the semiconductor surface. This effect can affect the stabilization of breakdown voltage which is the prime consideration in HVIC.

In order to solve the problems stated above, a new level-shifting structure with multiple metal rings（MMRs）by divided RESURF technique is proposed in this paper. The new structure should be more reliable and show better electrical performance than that used before.

2. Device structure and characteristics

Figure 3 shows the bird's view of an n-MOST with the divided RESURF structure. There are multiple metal rings which are denoted as M1, M2, M3 and M4 over the double RESURF regions in the voltage sustaining region of the high-side gate driver and the n-MOST. The MMRs act for stabilization of surface electric field. In comparison to the MFFPs, the merit of the voltage sustaining region with MMRs can absorb the surface mobile ionic charges to improve the reliability of the structure[11]. The n-epi region of the n-MOST is isolated from the n-epi region of the HVJT by the p-sub region. The width of the p-sub region between two n-epi regions is determined by the pinch voltage and the punch-through voltage. The surface of the p-sub region between two n-epi regions is covered by metal field plate which is connected with the drain of the n-MOST. The metal field plate extends to the n-epi region of the HVJT for higher punch-through voltage.

The cross-section along the dashed lines AA′ in Fig. 3 is shown in Fig. 4(a), which consists of a high voltage n-MOST and the n-epi region where there is the high-side gate driver. The drift region of the n-MOST is made by MMRs over the double RESURF structure. The cross-section along the dashed lines BB′ in Fig. 3 is shown in Fig. 4(b). There, except for the field plate on the gate oxide directly connected with the source, the structure of the HVJT is the same as that of the n-MOST. The cross-section along the dashed lines CC′ and DD′ in Fig. 3 is shown in Fig. 4(c), where two neighbouring p-top regions are connected with the p-sub region. That structure can suppress the effect of the parasitic n-MOST due to the neighbouring n-epi regions and the corresponding metal rings.

2.1. Static characteristics

In this paper, the breakdown voltage of the n-MOSTs shown in Fig. 4(a) and the HVJT shown in Fig. 4(b) are both

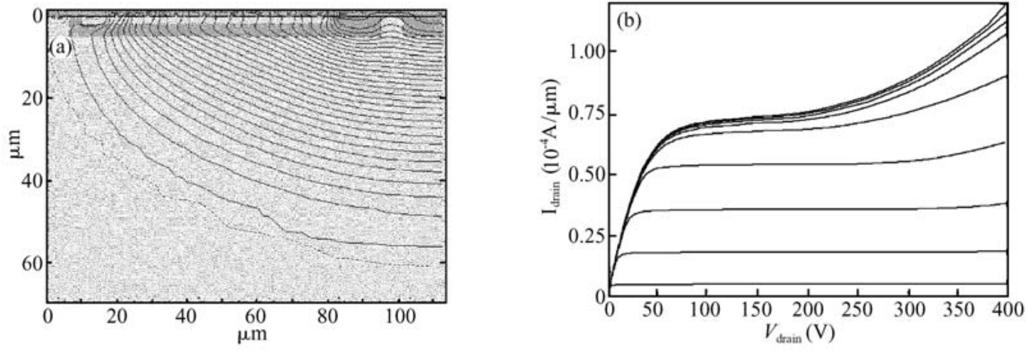


Fig. 5. (a) Potential distribution of n-MOST; (b) Output characteristic of n-MOST.

designed to be 600 V. To obtain high breakdown voltage, we have carried out optimizations for structural parameters as follows: a p-sub region doping of 2×10^{14} cm^{-3}, an n-epi layer doping of 4.2×10^{15} cm^{-3}, an n-epi layer depth of 5 μm, a p-top layer doping of 1.25×10^{16} cm^{-3} and a p-top layer depth of 2 μm. The length of the voltage sustaining region is 70 μm. The gate oxide thickness is 40 nm, the field oxide thickness is 0.85 μm and the oxide thickness between the metal layer and the silicon surface is 0.8 μm.

The punch-through voltage between the drain and the V_O + V_{DD} reaches 100 V for the structure shown in Fig.4 (a) where the width between two neighboring n-epi regions is 10 μm. In Fig. 4(c), the punch-through effects between two neighboring n-epi regions are suppressed by the p-top layer, so the punch-through voltage reaches 50 V that is enough higher than the usual level shifting signal.

With MEDICI simulating, the potential distribution of the n-MOST is shown in Fig. 5(a) when the drain and the V_o + V_{DD} are both biased by 600 V, where the difference between successive contour values is 20 V. Figure 5 (b) shows the output characteristic of the n-MOST.

2.2. Dynamic characteristics

The half bridge output, terminal O, is connected with inductive loading usually, and the level-shifting circuit shown in Fig. 1 has four main working processes in the ideal status: (1) the voltage of terminal O raises rapidly from zero to HV when the HVM1 and HVM2 are both off; where HV is the high voltage main supply; (2) the voltage of terminal O descends rapidly from HV to zero when the HVM1 and HVM2 are both off; (3) the HVM1 is from off to on when the voltage of terminal O equals HV voltage and the HVM2 is off; (4) the HVM2 is from off to on when the voltage of terminal O equals zero and the HVM1 is off. The analysis that follows will be divided into two parts: HVM1 and HVM2 being off and HVM1 or HVM2 being on.

2.2.1. HVM1 and HVM2 being off

There are parasitic capacities in the HVJT of the high-side gate driver and the drift regions of HVM1 and HVM2. The parasitic capacity is made of three parts: (1) C_1 is the depletion capacity constituted by the n-epi region and the p-sub region; (2) C_2 is the depletion capacity constituted by the n-epi region and the p-top region; (3) C_3 is the capacity constituted by the metal rings (MRs) and the silicon surface.

Because of the parasitic capacities stated above, a rapid change of the voltage of terminal O causes a lowering or raising of the voltage of the output of the level-shifting circuit. That is to say, when both n-MOSTs are off, the voltage of the input of the high-side gate driver V_{drain} will be lower or higher than that of the power supply of the high-side gate driver $V_{V_O+V_{DD}}$ which follows the change of the voltage of terminal O. V_{drain} also stands for the voltage of the drain of the n-MOST shown in Fig. 3. This voltage difference is denoted as ΔV and can be expressed as

$$\Delta V = V_{V_O+V_{DD}} - V_{drain}. \quad (1)$$

If the voltage difference ΔV is too large, then the function of the high-side gate driver circuit could be pushed in a non-proper way. So it is important to suppress the ΔV.

Obviously, ΔV in Eq. (1) can be expressed in another way.

$$\Delta V = I_{drain} R. \quad (2)$$

I_{drain} is not only the current of the drain of the n-MOST shown in Fig. 4(a), but also is that of HVM1 or HVM2 shown in Fig. 1. R is the values of R_1 or R_2 shown in Fig. 1. When the change of the voltage of terminal O is very fast and the n-MOSTs are off, I_{drain} is developed by charging and discharging of the parasitic capacities stated above. In the p-sub region, p-top region and MRs, the displacement current is supplied by the source, and the displacement current in the n-epi region is supplied by the drain. The latter current is I_{drain} and decides the value of ΔV. In the structure of this paper, a way is developed for the electron current to flow away from the drain to the MRs, and can suppress effectively the value of ΔV.

When the $V_{V_O+V_{DD}}$ is increasing at first, if the hole current for charging C_2 and C_3 in the p-top region is large enough, the potential of the p-top region is able to be 0.7 V higher than the n-epi region somewhere, the parasitical diode is on. Then, the electrons in the n-epi region flow into the p-top region, and then into MR by the electric field. But a few holes go into the n-epi region because there is large parallel electric field toward the source in the p-top layer. The electron current first flows into M1, because the potential of M1 is the highest among

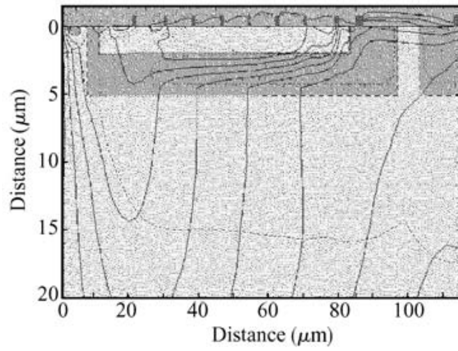


Fig. 6. Current contour in the structure.

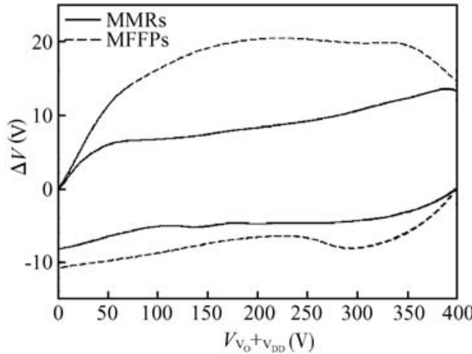
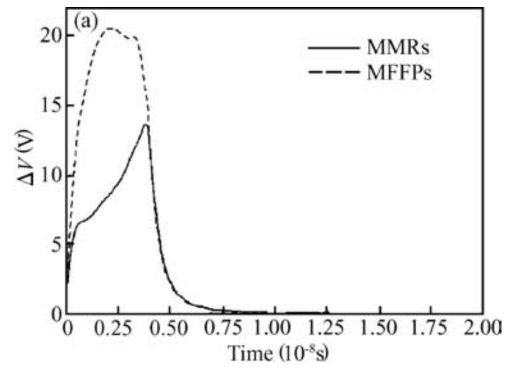


Fig. 7. Relation between $V_{V_O+V_{DD}}$ and ΔV.



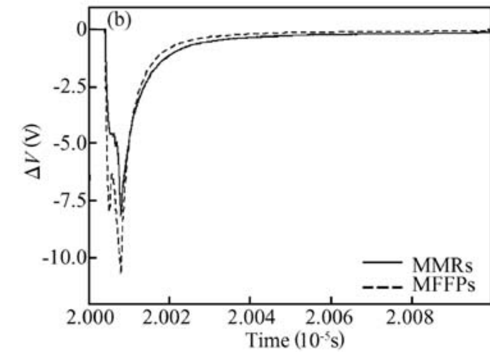


Fig. 8. Relation between ΔV and time during $V_{V_O+V_{DD}}$ (a) increasing and (b) dropping.

the MRs, and the effect is shown in Fig. 6. Since $V_{V_O+V_{DD}}$ of the HVJT is larger than V_{drain} of the n-MOST, the parasitical diode is first developed in the n-MOST. Then the capacity constituted by M1 and the silicon surface in the HVJT region is charged mainly by this electron current from the n-MOST and the holes current from the source is diminished, so the parasitical diode will be able to not be developed in the HVJT. With the voltage increasing, the electron current has opportunity to flow into M2, next into M3, then into M4, but these currents are less than that into M1 because the capacity made by M1 and the silicon surface is lager than the capacity made by the other metal rings and the silicon surface in the HVJT. Since the area of the HVJT of the high-side gate driver is large, the part of the electron current for charging the capacities of the HVJT in the n-MOST is large. However the total electron current is fixed in the n-MOST, the part of electron current flowing toward the drain is decreased. When the voltages of all of MRs are saturation, the holes current for charging disappears and the parasitical diode is off.

A MEDICI circuit simulation is adopted as follows. The cross-sections along the dashed lines AA′, BB′, CC′ and DD′ in Fig. 3 are connected as the devices in a special order. We suppose that the widths of the n-MOST and the HVJT of the high-side gate driver are 100 and 10 000 μm respectively. The widths of the cross-section along the dashed lines CC′ and DD′ are supposed by the metal rings width respectively. In MEDICI circuit simulation, both the ramp time of the voltage of terminal O from 0 to 400 V and from 400 to 0 V are both supposed 4 ns. The voltage of terminal O is supposed to change rapidly because there are two forces to hold the current continuity in the inductive loading circuit. One is to charge or discharge the capacities of the voltage sustaining region and the other is to trigger the flyback diode.

The solid-lines in Fig. 7 show the results of numerical simulation of the relation between $V_{V_O+V_{DD}}$ and ΔV of the structure of this paper. When $V_{V_O+V_{DD}}$ starts to increases and is small, ΔV increases rapidly, because the parasitical diode is not triggered and electron current flows toward the drain. When $V_{V_O+V_{DD}}$ continues increasing, ΔV starts to increasing slowly due to the parasitical diodes becomes being turned on gradually. When the voltages of all of FMRs are arriving saturation and the demand of the charging current is diminishing, ΔV starts to increase rapidly. However, as shown by the dashed lines in Fig. 7, in the structure of Ref. [10], the drain current is determined by the displacement current for charging the capacities constituted by the FFPs and the silicon surface. ΔV increases rapidly at firstly because all of the FFPs need to be charged and the displacement current is large. After ΔV arrive the peak value, all of the capacities arrives saturation gradually, and the charging current diminishes, then ΔV descends. The $V_{V_O+V_{DD}}$ dropping process is almost the same between two structures due to there is no parasitical diode developed. The difference is caused by the difference of the voltage sustaining region, i.e., the difference of MMRs and MFFPs.

Figures 8(a) and 8(b) show the relations between ΔV and time during $V_{V_O+V_{DD}}$ increasing and dropping process respectively. The time in which ΔV arrives at the stable state in the two structures is nearly the same.

Through comparing the simulation results stated above, when two n-MOST are off, the maximum value of ΔV of the level-shifting structure in this paper is 30% less than that in Ref. [10].

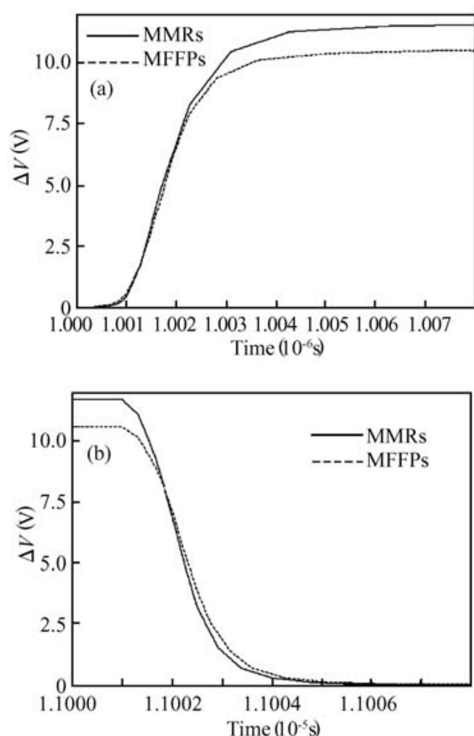


Fig. 9. Relation between ΔV and time during HVM1 switching (a) from off to on and (b) from on to off.

2.2.2. HVM1 or HVM2 being on

When the potential of terminal O equals HV with the HVM2 being off, during the HVM1 is from off to on and from on to off, the simulation result of the relations between ΔV and time is shown in Figs. 9(a) and 9(b) respectively. The ramp time of the gate voltage of the n-MOST is supposed to be 1 ns. From Fig. 9, the switching rate of two structures is nearly equal and both the values of ΔV are about 10 V. In the process, the current is limited in the n-MOST, so the current isolation is well carried out. The case When the potential of terminal O equals zero with the HVM1 being off during the HVM2 switching is almost the same as the above. From the simulation results, the level-shifting structure in this paper can complete accurately the work of level-shifting and transmitting the drive signal from the control logic to the floating high-side gate driver.

3. Conclusion

A 600 V n-MOST and a level-shifting structure with MMRs by divided RESURF technique have been proposed. The device and electrical performances of the structure are analyzed and simulated by the MEDICI. The simulation results show that this structure is able to complete accurately the function of level-shifting and transmitting the drive signal from the control logic to the floating high-side gate driver. In comparison to the level-shifting structure by the divided RESURF technique used before, the structure with MMRs is more reliable and yields less ΔV by the parasitical diode when the output voltage of the MOST half bridge changes rapidly. The maximum value of ΔV of the structure in this paper is 30% less than that used before. Good voltage isolation and current isolation are obtained. These structures have no limit of level-shifting voltage basically, and these areas are always smaller than a conventional structure in all kinds of level-shifting voltage.

Although RESURF technique is used in this paper for sustaining high voltage, it is evident that other techniques, such as the optimized variational lateral doping (VLD) technique can be adopted for the drift region of the level-shifting structure[12].

Therefore this structure could be applied to the level-shifting circuit of various applications.

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