A 1.8 V LDO voltage regulator with foldback current limit and thermal protection*

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Abstract: This paper introduces the design of a l.8 V low dropout voltage regulator (LDO) and a foldback current limit circuit which limits the output current to 3 mA when load over-current occurs. The LDO was implemented in a 0.18 μm CMOS technology. The measured result reveals that the LDO′s power supply rejection (PSR) is about −58 dB and –54 dB at 20 Hz and 1 kHz respectively, the response time is 4 μs and the quiescent current is 20 μA. The designed LDO regulator can work with a supply voltage down to 2.0 V with a drop-out voltage of 200 mV at a maximum load current of 240 mA.

Key words: LDO; bandgap; current limit; thermal protecting; error amplifier
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1. Introduction

Current limit circuits are extensively used in LDO circuits. They can protect LDO when load currents exceed safe values. The current limit embedded on an LDO must limit the output current to a small value when load over-current occurs. A classical current limit circuit (Fig. 1) can constrain the load current to a safe value but not a very small one by using a one stage current mirror to copy the load current in a certain ratio. The current limit circuit consumes a great deal of power when load over-current occurs. To solve this problem a foldback current limit circuit is proposed in this paper. It constrains the load current using two stage current mirrors. One can limit the load current to a fixed value, and simultaneously, output voltage decreases. The other can constrain the output current to a very small value.

Linear regulators are based on a feedback topology which requires frequency compensation to achieve closed-loop stability. It is difficult to maintain LDO stability because of the wider output current range, which causes the pole located at the LDO output to vary. To solve the issue, VCCS frequency compensation was proposed in Ref. [1] and current source amplifier frequency compensation was proposed in Ref. [2]. This paper uses off-chip capacitor ESR frequency compensation to overcome the stability problem.

2. Current limit circuit analysis

Figure 1 shows a classical current limit protecting circuit[5]. M2 and PW are made up of a current mirror. When $I_{\rm load}$ reaches the protecting current, $V_{\rm EB} + R_1 I_1 > V_{\rm ref2}$, M1 opens. I_1 is the current passing through the M2 transistor. The value of $(W/L)_{\rm PW}$ is very large (8880 in this paper); when $I_{\rm load}$ is 260 mA and $V_{\rm in}$ is 2.4 V, the PW transistor is still in the saturation region. When not considering channel length modulation, the maximum load current is

$$I_{\rm load} = K\frac{V_{\rm ref2} - V_{\rm EB}}{R_1}, \tag{1}$$

where $K = (W/L)_{\rm PW}/(W/L)_{\rm M2}$. In fact, when $I_{\rm load}$ reaches the protecting current, $I_{\rm load}$ continues to increase; the increasing coefficient depends on the classical current limit circuit. This is because

$$\frac{I_{\rm load}}{I_1} = K\frac{1+\lambda(V_{\rm in} - V_{\rm out})}{1+\lambda(V_{\rm in} - V_{\rm D2})}, \tag{2}$$

where λ is the channel length modulation coefficient. $V_{\rm D2}$ is the drain voltage of M2. When load over-current occurs,$V_{\rm D2}$ equals $V_{\rm ref2}$. According to Eq. (2), we can get:

$$I_{\rm load} = \frac{K(1+\lambda V_{\rm in})I_1}{1+\lambda(V_{\rm in} - V_{\rm D2}) + K\lambda R_{\rm load} I_1}, \tag{3}$$

where $I_1 = (V_{\rm ref2} - V_{\rm EB})/R_1$. $R_{\rm load}$ is the load resistor. Figure 3 shows the simulation result when K = 96, $V_{\rm in}$ = 3 V, $V_{\rm ref2}$ = 1.2 V. According to the above analysis, a classical current limit circuit can limit the output current to a specific range, but the large output current consumes a great deal of power when current limiting occurs.

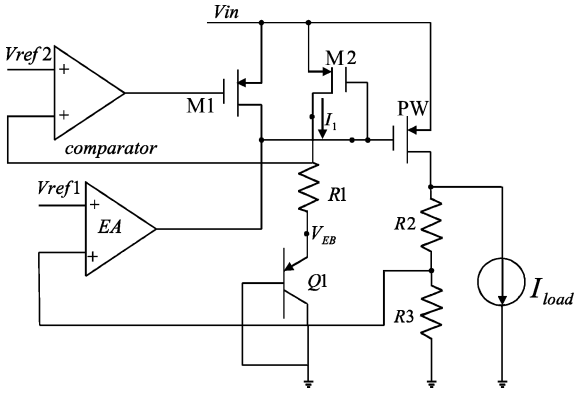

Fig. 1. Classical current limit circuit.

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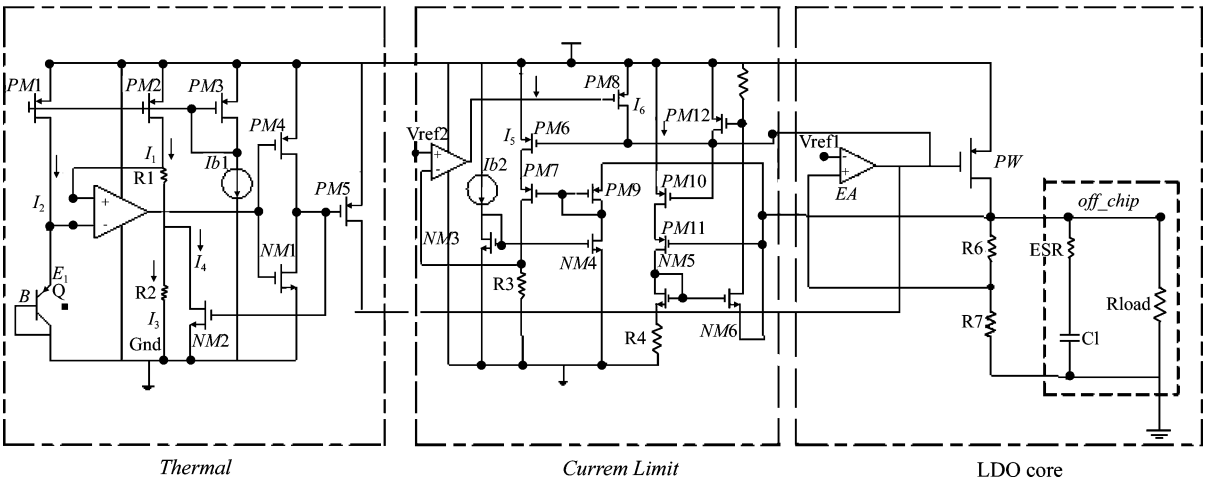

Fig. 2. The proposed LDO.

To solve the problem, a foldback current limit was proposed in Ref. [5]. The proposed current limit topology in this paper is shown in Fig. 2. The current limit topology includes two current mirrors to copy the output current. The first current mirror is made up of PM6 and PW. PM9 and PM7 can mitigate the influence of a channel length modulation on PM6. The second current mirror is made up of PM10 and PW. When load over-current occurs, the first current mirror limits the output current to

$$I_{\text{load1}} = K_1 \frac{V_{\text{ref2}}}{R_3}, \tag{4}$$

where $K_1 = \frac{(W/L)_{\text{PW}}}{(W/L)_{\text{PM6}}}$. Simultaneously, the output voltage decreases[5], then M6 opens. The following equation (5) is given according to the second current mirror.

$$V_{\text{GS5}} = \sqrt{\frac{2I_6}{(W/L)_{\text{NM5}}}} + V_{\text{tn}}, \tag{5}$$

$$R_4 I_6 + V_{\text{GS5}} - V_{\text{out}} - V_{\text{tn}} \approx \sqrt{\frac{2V_{\text{tp}}}{R_5}\left(\frac{W}{L}\right)_{\text{NM6}}}, \tag{6}$$

where $K_2 = \frac{(W/L)_{PW}}{(W/L)_{\text{PM10}}}$. According to Eqs. (5) and (6), the following equation (7) is solved.

$$I_{\text{load}} \approx \frac{\sqrt{2V_{\text{tp}}/(R_5(W/L)_{\text{NM6}})}}{(R_4/K_2) - R}. \tag{7}$$

When current limiting occurs ($R_4/K_2 \gg R$), the output current is very small, usually several millamperes. The output current simulation results are shown in Fig. 3 with no current limit, and classical and foldback current limits in the LDO circuit.

3. Stability of the proposed LDO and thermal protecting

The small signal equivalent circuit of the LDO core is shown in Fig. 4. Because $(W/L)_{\text{pw}}$ is very large, C_{pgs} and C_{pgd} substantially influence LDO stability.

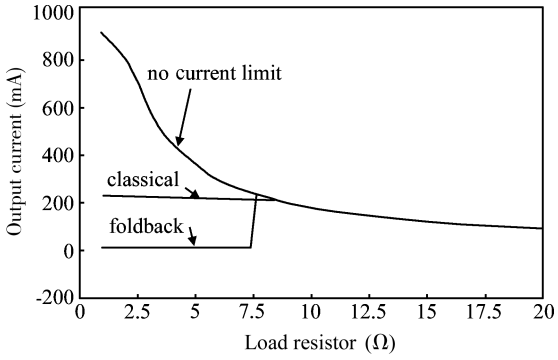

Fig. 3. Current limit spectra simulation results.

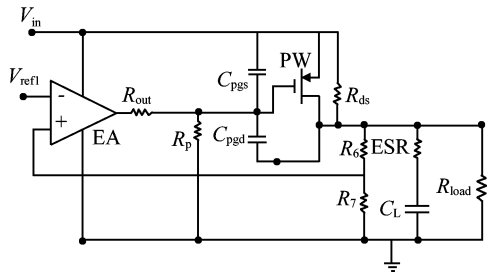

Fig. 4. Small signal equivalent circuit of the LDO core.

In this paper, LDO stability is achieved by the off-chip capacitor's equivalent series resistance (ESR) frequency compensation which provides an ESR zero (ϖ_{ESR}) for the open-loop transfer function and contributes pole-zero cancellation to ensure closed-loop stability. The two main poles in Fig. 4 are ϖ_{P1} and ϖ_{P2}, where $\varpi_{\text{P1}}$is at the gate of the PW transistor. ϖ_{P2} lies in the drain of the PW transistor[1].

$$\varpi_{\text{ESR}} = \frac{1}{\text{ESR} \times C_{\text{L}}}, \tag{8}$$

$$\varpi_{\text{P1}} = \frac{1}{C_{\text{L}}(R_{\text{Load}} \| (R_6 + R_7) \| R_{\text{ds}})}, \tag{9}$$

$$\varpi_{\text{P2}} = \frac{1}{R_{\text{P}}\left(C_{\text{pgs}} + g_{\text{mpw}} C_{\text{pgd}}(R_{\text{Load}} \| (R_6 + R_7) \| R_{\text{ds}})\right)}. \tag{10}$$

So the open-loop gain transfer function of the proposed LDO

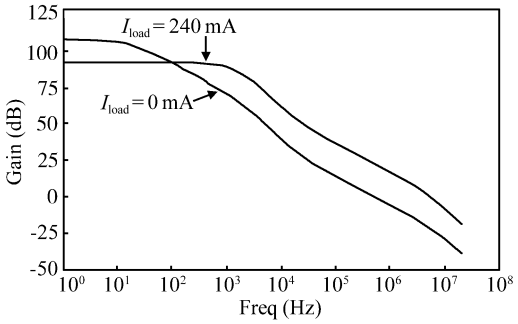

Fig. 5. Full range open loop gain of AC response.

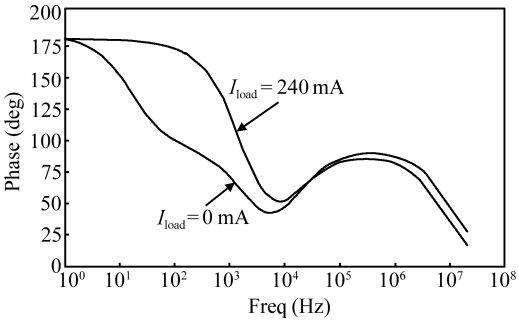

Fig. 6. Full range open loop phase of AC response.

voltage regulator is given as follows.

$$H(s) = \frac{A_0\left(1 + \dfrac{s}{\varpi_{\mathrm{ESR}}}\right)}{\left(1 + \dfrac{s}{\varpi_{\mathrm{P1}}}\right)\left(1 + \dfrac{s}{\varpi_{\mathrm{P2}}}\right)}, \tag{11}$$

A_0 is the DC open loop gain of the error amplifier, PW transistor, and feedback resistors[1].

$$A_0 = g_{\mathrm{mPW}}[(R_6 + R_7)\|R_{\mathrm{ds}}\|R_{\mathrm{load}}]\frac{R_7}{R_6 + R_7}A_{\mathrm{v}}\frac{R_{\mathrm{p}}}{R_{\mathrm{out}} + R_{\mathrm{p}}}, \tag{12}$$

g_{mPW} is the transconductance of the PW transistor. R_{out} is the output impedance of the error amplifier. R_{p} is the parasitic resistor of the PW transistor[1]. The stability simulation results are given as follows. The full open loop gain is shown in Fig. 5 and the full open loop phase is shown in Fig. 6.

When the chip temperature exceeds a certain value T_1, the PW transistor should be closed (thermal protecting circuit undertakes this role), otherwise the chip would be damaged and work abnormally. A new thermal protecting circuit was proposed in Ref. [6]. A thermal protecting circuit is proposed (Fig. 2) in this paper. When the temperature reaches the protecting temperature T_1, I_3 increases to I_1.

When temperature returns to T_2, LDO starts to work normally again.

$$T_1 = \frac{[(R_1 + R_2)I_1 - R_2 I_4]q}{k\ln(I_2/I_{\mathrm{EBS1}})}, \tag{13}$$

$$T_2 = \frac{(R_1 + R_2)I_1 q}{k\ln(I_2/I_{\mathrm{EBS2}})}, \tag{14}$$

$I_{\mathrm{EBS1}}, I_{\mathrm{EBS2}}$ are the emitter base reverse saturation currents at temperatures T_1 and T_2 respectively.

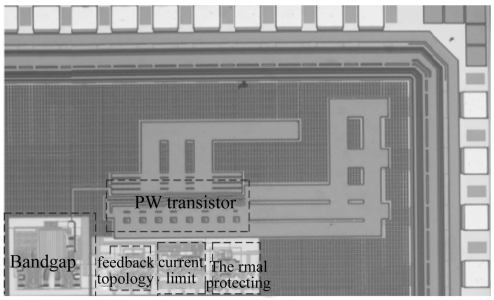

Fig. 7. Micrograph of the proposed LDO.

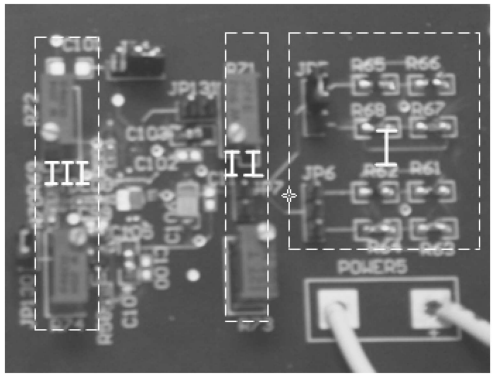

Fig. 8. Test circuit used in COB technology.

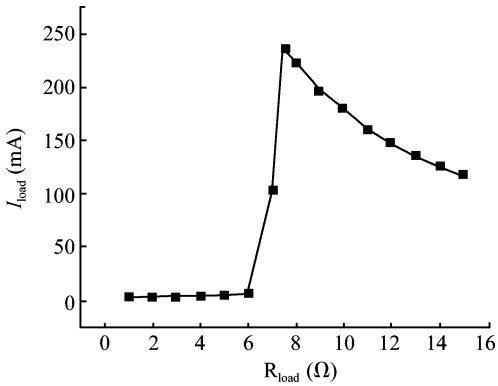

Fig. 9. Current limit measured result.

4. Measured results

The LDO regulator was measured when R_0 = 40 kΩ, R_1 = 80 kΩ, V_{ref1} = 1.2 V, C_1 = 1 μF, ESR = 150 mΩ, R_{load} ranged from 1 Ω to 2 kΩ, the DC input voltage ranged from 2.0 V to 3.5 V and the DC output voltage was 1.8 V. Figure 7 shows a micrograph of the proposed LDO. Figure 8 shows the test circuits. Part I tests the transient response time. Part II measures the load regulation. Part III supplies a voltage to current limit circuit V_{ref2}.

4.1. Current limit

The current limit circuit is measured when the load resistor ranges from 1 Ω to 15 Ω. Figure 9 shows the measured result when V_{in} = 3 V.

4.2. Thermal protecting

In order to protect the LDO working at a suitable temperature, a thermal protecting circuit is necessary. Figures 10 and 11 show the measured results when V_{in} = 2.3 V and I_{load} =

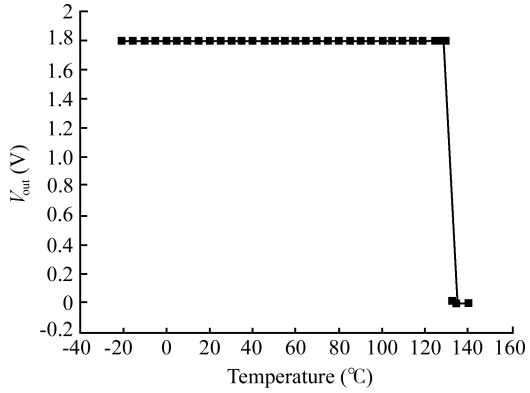

Fig. 10. V_{out} versus temperature when temperature ranges from −20 to 140 °C.

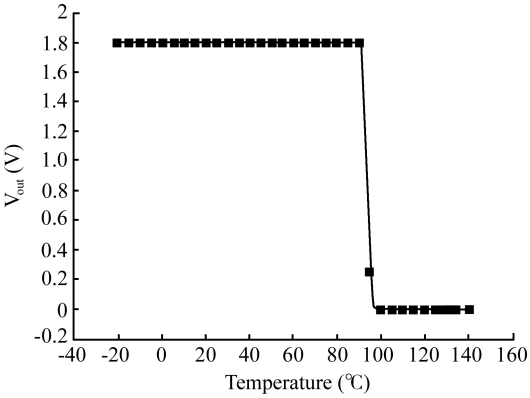

Fig. 11. V_{out} versus temperature when temperature ranges from 140 to −20 °C.

200 mA. T_1 = 133 °C and T_2 = 88 °C. So $\Delta T = T_1 - T_2$ = 45 °C.

4.3. PSR performance

The frequency of voltage source noise is mainly between 10 Hz and 100 kHz. LDO should have high PSR in the frequency. PSR is important, especially in some RF circuits, such as VCO, LNA, and Mixer. According to Fig. 4, Equation (15) is solved.

$$\mathrm{PSR} = 20\lg\frac{Z_{\mathrm{out}}}{R_{\mathrm{ds}} + Z_{\mathrm{out}}}, \tag{15}$$

where $Z_{\mathrm{out}} = \left[(R_6 + R_7)\|R_{\mathrm{ds}}\|(ESR + \frac{1}{sC_{\mathrm{L}}})\right] \Big/ \left(1 + \frac{R_7}{R_6 + R_7}A_0\right)$.

4.4. Load regulation

Load regulation characteristics are not symmetrical for increase and decrease in load current[1]. When I_{load} decreases, feedback resistors R_6, R_7, and the error amplifier generate a lower voltage to control the PW transistor gate. When I_{load} increases, the feedback loop generates a high voltage to the PW transistor gate. So the output voltage is stable. Equation (17) gives the relationship between V_{out} and R_{load}.

$$I_{\mathrm{load}} = K\left[\left(V_{\mathrm{in}} - V_{\mathrm{G}} - V_{\mathrm{tp}}\right)(V_{\mathrm{in}} - V_{\mathrm{out}}) - \frac{(V_{\mathrm{in}} - V_{\mathrm{out}})^2}{2}\right], \tag{16}$$

$$\frac{\partial V_{\mathrm{out}}}{\partial R_{\mathrm{load}}} \approx \frac{V_{\mathrm{out}}}{R_{\mathrm{load}}\left[1 + K\left(\frac{2}{3}V_{\mathrm{in}} - \frac{4}{3}V_{\mathrm{out}} + V_{\mathrm{ref1}}\right)A_0\right]}, \tag{17}$$

Table 1. Summary of the measured results.

Parameter	Value
Process	CMOS 0.18 μm
V_{out}	1.8 V
Drop voltage	0.2 V @ 240 mA
I_{load}	0–240 mA
Quiescent current	20 μA
Response time	4 μs
PSR	–58 dB @ 20 Hz, I_{load}= 100 mA; –54 dB @ 1 kHz, I_{load}= 100 mA
Load regulation	1/60 @ I_{load}= 1–180 mA, 3/4 @ I_{load}= 180–240 mA
Voltage regulation	7.5/100 @ V_{in} = 2.0–2.4 V 0.21/100 @ V_{in} = 2.4–3.5 V
Chip area	0.18 mm^2
Temperature coefficient	10 ppm

where $K = \mu_{\mathrm{p}}c_{\mathrm{ox}}\left(\frac{W}{L}\right)_{\mathrm{PW}}$ and $\frac{R_6}{R_7} = \frac{1}{2}$.

4.5. Voltage regulation

The LDO can regulate the dc output voltage, and is not influenced by input voltage. When the input voltage increases, the output voltage increases instantaneously, and the PW transistor gate voltage increases accordingly. Finally the output voltage remains stable. Voltage regulation of the regulator is determined by the loop dc gain[1].

5. Conclusion

This paper presents a foldback current limit circuit which limits output current to a small level when the output current exceeds the protecting current and also presents a thermal protecting circuit design. The measured result is shown in Table 1. Current limit and thermal protecting do not influence the load regulation, voltage regulation, transient response, and PSR performance. It is also proved that they do not consume much power.

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