A 2.4-GHz SiGe HBT power amplifier with bias current controlling circuit*

Peng Yanjun(彭艳军)[1,2], Song Jiayou(宋家友)[1,3], Wang Zhigong(王志功)[1,†], and Tsang K F(曾剑锋)[2]

(1 Institute of RF- & OE-ICs, Southeast University, Nanjing 210096, China)
(2 Department of Electronic Engineering, City University of Hong Kong, Hong Kong, China)
(3 School of Information Engineering, Zhengzhou University, Zhengzhou 450052, China)

Abstract: A 2.4-GHz SiGe HBT power amplifier (PA) with a novel bias current controlling circuit has been realized in IBM 0.35-μm SiGe BiCMOS technology, BiCMOS5PAe. The bias circuit switches the quiescent current to make the PA operate in a high or low power mode. Under a single supply voltage of +3.5 V, the two-stage mode-switchable power amplifier provides a PAE improvement up to 56.7% and 19.2% at an output power of 0 and 20 dBm, respectively, with a reduced quiescent current in the low power mode as compared to only operating the PA in the high power mode. The die size is only 1.32×1.37 mm^2.

Key words: power amplifier; SiGe HBT; bias circuit
DOI: 10.1088/1674-4926/30/5/055008 **EEACC:** 1350; 2220

1. Introduction

In modern wireless communications systems, the design of RF power amplifiers (PA) for mobile equipments is a challenging task. A PA generally consumes considerable power in the whole transceiver system. The efficiency of the RF PA is, therefore, one of the key requirements. On the other hand, the growing demands for information throughput for rapidly evolving consumer wireless products have resulted in the implementation of RF modulation schemes, which have low tolerance for system non-linearity. The design of highly efficient and highly linear PAs has become a critical issue.

The efficiency of a PA is mainly determined by the efficiency of the power transistor and by losses in the output matching network. Both of them strongly depend on the choice of the technology. In past years, HBT PAs have dominated the medium power transmitter market due to their excellent linearity and PAE. Since GaAs-based integrated circuits are relatively expensive and the heat dissipation of the substrate is poor, SiGe HBTs are more attractive due to their higher substrate thermal conductivity, lower turn-on voltage, lower saturation voltage $V_{CE,SAT}$ and lower cost. Unfortunately, SiGe HBTs have their own disadvantages: the resistivity of the substrate is low, which adds significant parasitics to both active and passive components; the breakdown and early voltages are relatively low, which are detrimental to the gain, the linearity, and the dynamic range of the PA[1].

Usually, a PA has a higher efficiency at its maximum output power, but in most cases it only needs to work in a middle output power state[2]. A back-off of the output power results in a significant decrease in efficiency. A well-known technique for improving the average system efficiency is to use a bias control system. In this work, we report on a 2.4-GHz SiGe HBT PA with a novel bias current controlling circuit. It is realized in IBM's BiCMOS5PAe, a standard 0.35-μm SiGe BiCMOS technology. The bias circuit switches the quiescent current to make the PA operate in high or low power mode. Under a single supply voltage of +3.5 V, the two-stage mode-switchable PA provides a PAE improvement up to 56.7% and 19.2% at an output power of 0 and 20 dBm, respectively, owing to the reduced quiescent current in the low power mode.

2. Technology description

This work was based on the IBM 0.35-μm SiGe BiCMOS process with base-after-gate integration approach. It provides two state-of-the-art NPNs, a high performance NPN and a high voltage NPN, with f_T–BV_{CEO} values of 40 GHz / 6.0 V and 27 GHz / 8.5 V, respectively. Owing to the fact that the signal in the power amplifier has a large swing, the high voltage transistor is suitable for the PA design. When biased under the Class-AB operation, the supply voltage of the HBT can be set to 3.5 V since the maximum operation of a SiGe HBT is largely limited by its average voltage and current [3].

As shown in Fig. 1, this process also provides high quality on-chip passives: 1.35 fF/μm^2 MIMcaps with 40 V breakdown voltage (a dual MIM stack allows up to 2.7 fF/μm^2 capacitance density), 60 Ω/sq. TaN resistors, and a thick

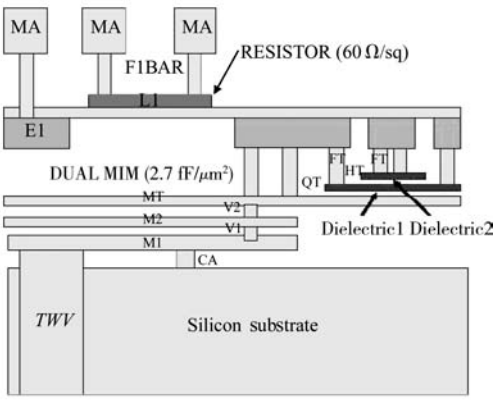

Fig. 1. Sketch of the back-end-of-the-line stack.

* Project supported by the City University of Hong Kong (Nos. 700182, 7002007).
† Corresponding author. Email: zgwang@seu.edu.cn
Received 26 September 2008, revised manuscript received 9 November 2008

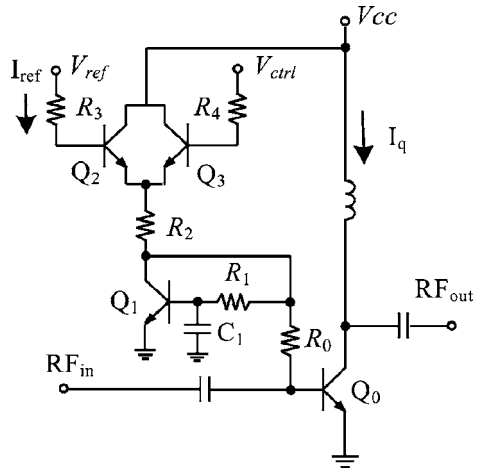

Fig. 2. Schematic of the bias current controlling circuit.

dual-metal (3.0 μm Cu and 4.0 μm Al) for high Q inductors. The most notable characteristic of this technology is that it provides a low resistance and inductance ground through-wafer-via (TWV), rendering the possibility to design a high performance PA at low cost[4].

3. Bias circuit design

In order to increase the efficiency, it is common practice to bias a HBT PA at low quiescent current when working in the back-off state. For bias switching mode operation, a new on-chip bias current controlling circuit is devised, as shown in Fig. 2. The emitter follower bias circuit provides temperature compensation and reduces the need for a reference current[5]. The collector current density of the reference transistor Q1 is designed so as to be equal to the collector current density of power transistor Q0. It is important to provide a proper ratio of the balance resistors R_1 to R_0, which is equal to the area ratio S of Q0 to Q1. If the needed quiescent current of Q0 is I_q, the needed current I_{ref} drawing from reference voltage V_{ref} is as follows:

$$I_{ref} = \left(\frac{I_q}{\beta} + \frac{I_q}{\beta S} + \frac{I_q}{\beta S}\beta\right)\frac{1}{\beta} = \left(\frac{1}{\beta^2} + \frac{1}{\beta^2 S} + \frac{1}{\beta S}\right)I_q. \quad (1)$$

If β and the area ratio S are large enough (> 100), the emitter follower bias circuit only needs tens of microampere current while the conventional mirror current bias circuit needs several milliampere, and it is also insensitive to a variation of the reference voltage. The parallel capacitor C_1 connecting to the base of Q1 forms a low pass filter with resistors R_1 and R_0, which provides a good isolation between the bias circuit and the RF signal path. When V_{ctrl} is less than 0.5 V, the designed PA works in the low power mode and V_{CE} of Q3 becomes 0 V. In this case, Q3 cannot supply current, and only Q2 supplies current to the base of Q0. When V_{ctrl} varies in the range of 1.7–2 V, the PA works in the high power mode, and both Q2 and Q3 supply current to the base of Q0.

4. Circuit design and layout techniques

Figure 3 shows the schematic of the 2.4-GHz two-stage mode-switchable SiGe PA with the base bias circuit. All

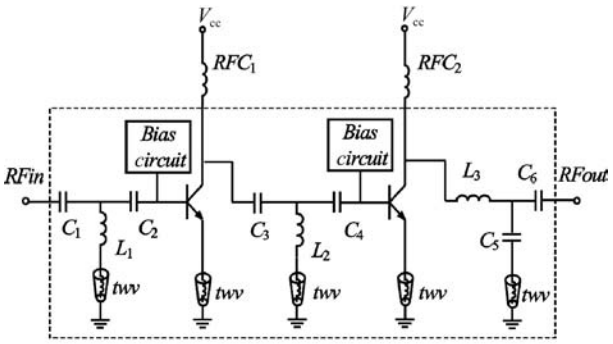

Fig. 3. Schematic of the mode-switchable SiGe HBT PA.

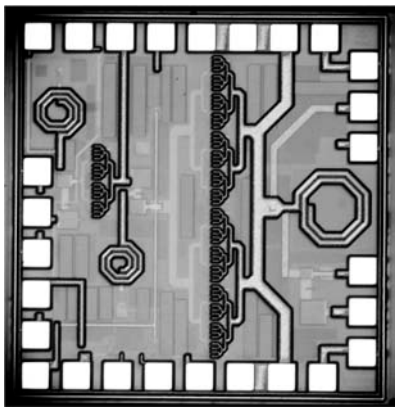

Fig. 4. Photograph of the mode-switchable SiGe HBT PA.

components except the RF choking inductors are integrated on the chip. The high pass T-type input matching network consisting of C_1, L_1, and C_2 and increases the overall stability of the PA because it reduces the gain at low frequencies below the operating frequency band. In the same way, the inter-stage matching network consisting of C_3, L_2, and C_4 and has a significant effect on the stability and bandwidth of the PA. The output matching network is a low pass T-type network, which can suppress the high-order harmonics in the output signal; thus, improving the linearity and the efficiency.

A well-designed mask layout is important for an RF PA design. For a high power design, a multitude of devices should be used in parallel in order to distribute the large current among small unit devices. The binary feed lines can effectively keep an equal phase front in all unit cells. Thirty two high voltage NPN HBTs with an emitter area of 1536 μm^2 are used in the output stage, and eight identical NPN HBTs with an emitter area of 384 μm^2 are used in the driving stage. The device size of the driving stage is larger than what is needed. Hence, enough margin is left to guarantee the linearity of the driving signal. To deliver a high power, a large current should flow in the power cells, which will cause excessive heat in the active devices. The excessive heat is destructive to the power cells and should be dissipated. The grounded TWV connected to the emitter of the active devices are used as heat ducts and are placed uniformly and close to the power cells. Therefore, the excessive heat can be dissipated by the ground plane of the substrate. On the other hand, it is also equally important to have uniform heat conduction for each of the unit cell. The photograph of the power amplifier is shown in Fig. 4.

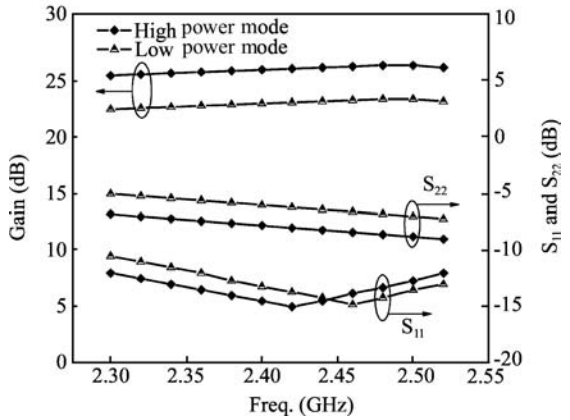

Fig. 5. Measured gain, S_{11}, and S_{22} of the mode-switchable SiGe HBT PA.

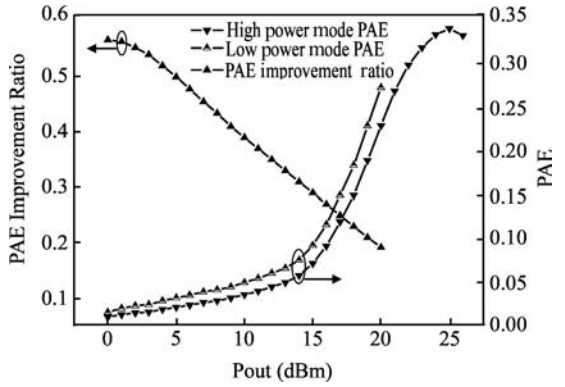

Fig. 6. Measured PAE and PAE improvement ratio of the mode-switchable SiGe HBT PA.

5. Test results

Our Agilent test equipment includes a DC power supply 66309D, a network analyzer E5071B (300 kHz–8.5 GHz), a signal generator E4438C (250 kHz–6.0 GHz), and a spectrum analyzer E4440A (3 Hz–26.5 GHz). As shown in Fig. 5, when operating in the low power (LP) mode, the measured small-signal gain is 23 dB, S_{11} is –14.5 dB, and S_{22} is –6.5 dB at 2.45 GHz; while in the high power (HP) mode, the gain is 26.2 dB, S_{11} is –14.3 dB, and S_{22} is –8.3 dB. Figure 6 shows the measured $\mathrm{PAE_L}$ and $\mathrm{PAE_H}$, PAE improvement ratio (PAEIR) of this mode-switchable PA. The PAEIR is defined as[6]

$$\mathrm{PAEIR} = \frac{\mathrm{PAE_L} - \mathrm{PAE_H}}{\mathrm{PAE_H}} \times 100\%. \quad (2)$$

The PAEIR is 19.2% at an output power of 20 dBm but achieves 56.7% at an output power of 0 dBm. Figure 7 shows that the second and third harmonics are –32 and –42.5 dBc at the peak output power 20.3 dBm ($P_{\mathrm{1dB\_LP}}$) when working in LP mode. In HP mode, the second and third harmonics are –34.5 and –43.5 dBc at the peak output power 25.2 dBm ($P_{\mathrm{1dB\_HP}}$).

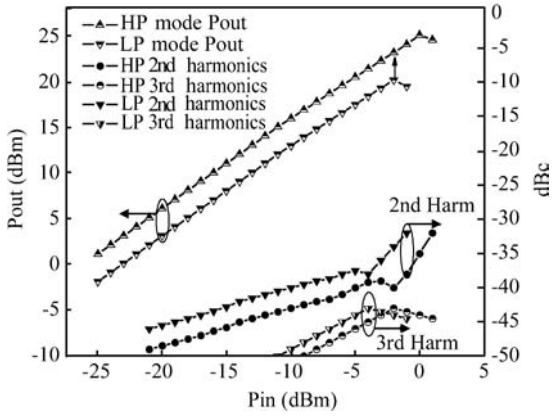

Fig. 7. Measured fundamental output power, second and third harmonics suppression ratio of the mode-switchable SiGe HBT PA.

6. Conclusion and analysis

A mode-switchable SiGe HBT power amplifier for high efficiency using a novel bias current controlling circuit has been realized. With a reduced quiescent current in the low power mode operation, it provides a PAE improvement up to 56.7% at an output power of 0 dBm and 19.2% at an output power of 20 dBm as compared to the operation in the high power mode. It also proves that the low-cost technology, SiGe BiCMOS5PAe, enables a path for an integrated all-silicon PA module for future wireless communication systems.

Acknowledgment

The authors thank the IBM Semiconductor Research and Development Center for supporting and free wafer fabrication. The authors would also like to express their gratitude to Zhang Xiaoli and Li Wei for their help in the circuit design and test.

References

[1] Johnson J B, Joseph A J, Sheridan D C, et al. Silicon-germanium BiCMOS HBT technology for wireless power amplifier applications. IEEE J Solid-State Circuits, 2004, 39(10): 1605

[2] Fowler T, Burger K, Cheng N S, et al. Efficiency improvement techniques at low power levels for linear CDMA and WCDMA power amplifies. Proc IEEE RFIC Symp, 2002: 41

[3] Kraft J, Loffler B, Ribic N, et al. BVCER-increased operation voltage for SiGe HBTs. IEEE 44th Annual International Reliability Physics Symposium, 2006: 507

[4] Joseph A, Liu Q, Hodge W, et al. A 0.35 μm SiGe BiCMOS technology for power amplifier applications. Bipolar/BiCMOS Circuits and Technology Meeting, 2007: 198

[5] Sato T, Grigorean C. Design advantages of CDMA power amplifiers built with MOSFET technology. Microwave J, 2002, 45: 64

[6] Noh Y S, Kim J H, Park C S. MMIC power amplifier with on-chip bias current controlling circuit for W-CDMA mobile handset. Electron Lett, 2002: 1686