# A 540-$\mu$W digital pre-amplifier with 88-dB dynamic range for electret microphones

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**Abstract:** We design a digital pre-amplifier which can be directly connected to an electret microphone. The amplifier can convert analog signals into digital signals, has a wide voltage swing and low power consumption, as is required in portable applications. Measurement results show that the dynamic range of the digital pre-amplifier reaches 88 dB, the equivalent input referred noise is 5 $\mu$Vrms, the typical power consumption is 540 $\mu$W, and in standby mode the current does not exceed 10 $\mu$A. Compared with an analog microphone, an electret microphone with digital pre-amplifier offers a better SNR, higher integration, lower power consumption, and higher immunity to system noise.

**Key words:** digital microphones; CT integrator; LDO; electret microphone
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## 1. Introduction

A microphone is a useful device to convert an audio signal into an electrical signal. A conventional microphone is based on analog techniques. The audio signal is amplified, modulated or composed by a series of analog devices. In most cases, the analog electrical signal is converted into a digital signal via an analog-to-digital converter (ADC). Due to its low immunity to noise, analog signals are easily influenced by radio frequency (RF) and electromagnetic interference (EMI) on the transfer path. Thus, in order to guarantee a good signal quality, additional efforts, which involve cost, physical space and time, have to be made.

Nowadays, people desire more advanced audio communication experiences. However, for analog microphones, it is difficult to satisfy this demand. In this paper, a digital pre-amplifier for electret microphones is designed. It can convert analog signals into digital signals, has a wide voltage swing and low power consumption as is required in portable applications. The digital pre-amplifier meets the requirements of a new generation of advanced audio systems, offers higher integration, stronger immunity to system noise, lower power consumption and design cost.

## 2. Digital pre-amplifier architecture

Our digital pre-amplifier uses a single chip that integrates all stages necessary to convert the microphone output to digital code. Figures 1(a) and 1(b) show the conventional audio transfer path and the audio path using a digital pre-amplifier, respectively.

In the conventional audio transfer path, noise from RF and EMI in each stage affects the audio signal. This is especially true for the buffer and the programmable gain amplifier (PGA) stages. In these stages, the noise influences an analog signal that has a very low noise immunity. As a consequence, the quality of the audio signal will be affected.

The digital pre-amplifier presented in this paper is a new technology targeting at solving the above-mentioned disadvantages. This design does not simply put the buffer, the PGA, and the ADC together onto one chip, but it also simplifies and integrates their functions. The overall digital pre-amplifier architecture is shown in Fig. 2.

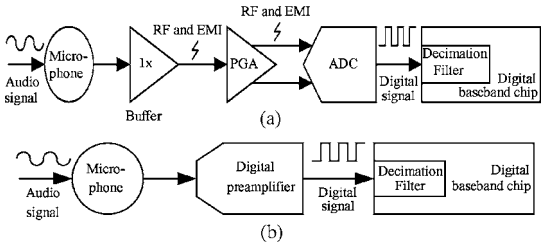


Fig. 1. (a) Conventional audio signal transfer path; (b) Signal transfer path with a digital pre-amplifier.

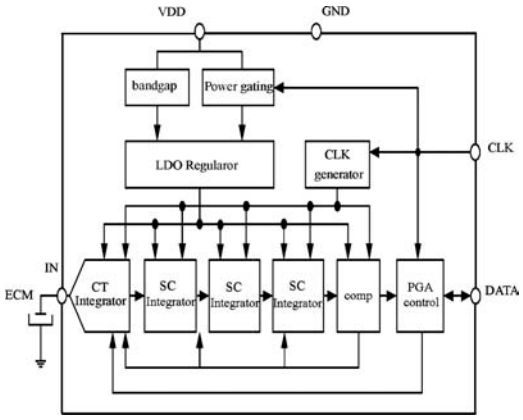


Fig. 2. Digital pre-amplifier architecture.

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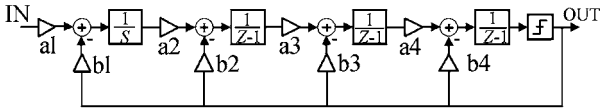


Fig. 3. CT-SC sigma-delta modulator architecture.

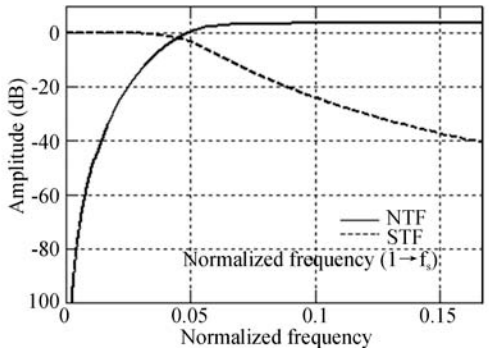


Fig. 4. NTF and STF magnitude characteristics.

The digital pre-amplifier includes two major blocks: a sigma-delta modulator and a clock-frequency-controlled low-dropout regulator (LDO). Because the modulator consumes most of the power, the design of this modulator is a key issue. The digital pre-amplifier presented in this paper was designed for a dynamic range of over 80 dB at a 20 Hz to 20 kHz bandwidth. A fourth-order single-loop single-bit sigma-delta modulator and an oversampling ratio of 64 were chosen. The LDO with a built-in voltage reference generates all the supply and reference voltages, and supports a standby mode controlled by the clock frequency.

## 3. Circuit design

As in all sigma-delta modulator designs, a choice has to be made between a switched-capacitor (SC) integrator and a continuous-time (CT) integrator. SC circuits offer better stability and they are also less sensitive to circuit non-idealities[1]. CT integrators can be designed with a single-ended input and a high input impedance, while all SC circuits need a driver in front of the integrator to charge the sampling capacitors. Another advantage of the CT integrator is its lower noise bandwidth; so a better performance versus power ratio can be achieved[2]. The digital pre-amplifier is connected with the single-ended input of its first integrator to one plate of the electret microphone. The microphone with a high output impedance delivers a $\mu$V-level signal. Therefore, a mixed CT-SC single-loop single-bit sigma–delta modulator is the most convenient choice in this paper. The modulator architecture is shown in Fig. 3.

This architecture allows for a good control of the noise transfer function (NTF) as well as for a good control of the signal transfer function (STF) by using the feedback coefficients $b_1$, $b_2$, $b_3$, and $b_4$. No higher-order integrators is connected to the input of the modulator, leaving only the first integrator to load the electret microphone[2].

The NTF and STF are designed using "The delta–sigma Toolbox" [12]. The input signal bandwidth is 20 kHz, the oversampling ratio (OSR) is 64, and the sample clock frequency is

Table 1. Modulator coefficients.

| | | | |
|---|---|---|---|
| a1 | 0.1 | b1 | 0.1 |
| a2 | 0.13 | b2 | 0.07 |
| a3 | 0.3 | b3 | 0.16 |
| a4 | 0.5 | b4 | 0.2 |

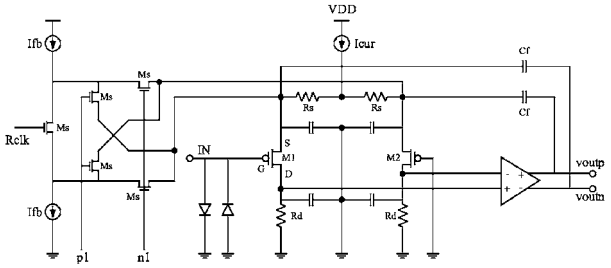


Fig. 5. New first CT integrator.

2.56 MHz. The design results for mapping to Z-domain polynomials representing NTF($z$) and STF($z$) can be written as

$$\mathrm{NTF}(z) = \frac{(z-1)^4}{(z^2-1.493z+0.5647)(z^2-1.702z+0.7871)},$$

$$\mathrm{STF}(z) = \frac{0.0061418}{(z^2-1.493z+0.5647)(z^2-1.702z+0.7871)}.$$

The normalized coefficients of the modulator are summarized in Table 1.

Normalized magnitude characteristics of the NTF and the STF are shown in Fig. 4. The quantization noise can be transferred to high-frequency by the NTF and the designed flatness of the STF magnitude is better than 0.1 dB from DC to 20 kHz. The peak signal-to-noise-ratio (SNR) of this modulator is 82.1 dB.

Conventional SC integrators and CT integrators do not need a high input impedance because in most applications a signal buffer is already available in front of the sigma–delta modulator. In order to connect the modulator directly to an electret microphone having a high output impedance, the new first CT integrator shown in Fig. 5 has been designed.

The single-ended microphone signal IN (Fig. 5) is connected to the gate of the PMOS transistor M1. The usage of PMOS devices provides an input range of more than −200 mV, enough to accommodate the microphone signal. The transistor pair M1/M2 works as a voltage-to-current converter and has high input impedance.

In order to make M1 operate in the saturation region, Equations (1) and (2) must be satisfied.

$$V_{\mathrm{DD}} = V_{\mathrm{DD}} - V_{\mathrm{S1}} + V_{\mathrm{SD1}} + V_{\mathrm{Rd}}, \tag{1}$$

$$V_{\mathrm{SG1}} = V_{\mathrm{S1}} - V_{\mathrm{IN}} < V_{\mathrm{SD1}} + |V_{\mathrm{TP}}|, \tag{2}$$

where $V_{\mathrm{S1}}$ is the M1 source voltage, $V_{\mathrm{SD1}}$ is the M1 source-drain voltage, $V_{\mathrm{SG1}}$ is the M1 source-gate voltage, $V_{\mathrm{TP}}$ is the p-channel transistor threshold voltage, and $V_{\mathrm{Rd}}$ is the $R_{\mathrm{d}}$ voltage. According to Eqs. (1) and (2), the input voltage of the microphone is given by

$$V_{\mathrm{IN}} = V_{\mathrm{G1}} > V_{\mathrm{Rd}} - |V_{\mathrm{TP}}|. \tag{3}$$

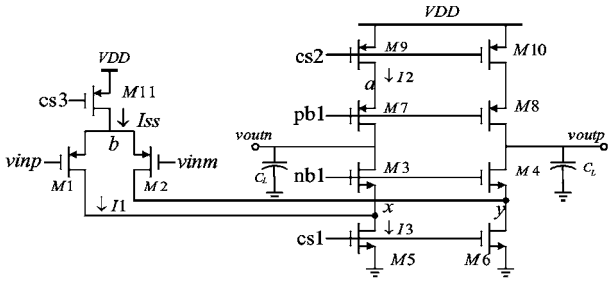


Fig. 6. Fully-differential folded-cascode amplifier.

If $V_{Rd}$ is less than 200 mV and $|V_{TP}|$ = 400 mV, then the input transistors can still operate with the gates at 200 mV below ground.

Figure 6 shows a fully-differential PMOS input folded-cascode amplifier as used in the first CT integrator. The first advantage of this amplifier is that it has only one single non-dominant pole. It is fairly easy to design and its frequency is very high. Therefore, the gain-bandwidth (GBW) can be quite high. The second important advantage is that the input transistors can operate at negative gate voltages.

A differential feedback current involving $I_{fb+}$ and $I_{fb-}$ is connected to the sources of M1 and M2, as seen in Fig. 5. The switches Ms are activated by the digital signals p1 and n1, directing the differential feedback current $I_{fb+}/I_{fb-}$ from the source of M1 to the source of M2, and vice versa. The feedback current is integrated by the operational amplifier on the feedback capacitors $C_f$ in the same manner as the signal current.

For the actual circuit, we first design a fourth-order sigma-delta modulator with SC integrators and then replace the first SC integrator with a CT integrator. The feedback voltage of the SC integrator is replaced by feedback current of the CT integrator. The feedback current $I_{fb}$ can be calculated as

$$I_{fb} = V_{ref} C_S f_{CLK}, \tag{4}$$

where $V_{ref}$ is the reference voltage, $C_s$ is the sample capacitor, and $f_{CLK}$ is the clock frequency. Then single-ended-to-differential conversion takes place at the level of the first CT integrator, and the current source of the differential circuit is connected with $R_S$ and $I_{fb}$. $R_S$ controls the gain $A$ of the modulator. The control "word" is written to the PGA control unit through the DATA and CLK pads, which makes it possible to set different $R_S$ values, and thus a different gain of the modulator.

$$R_S = \frac{1}{A f_{CLK} C_S} = \frac{V_{ref}}{A I_{fb}}. \tag{5}$$

The higher-order integrators are fully-differential SC circuits, as shown in Fig. 7. They consist of sampling capacitors $C_S$, integrating capacitors $C_i$ and an operational amplifier.

One advantage of the SC integrator is the decoupling of the input signal common-mode $V_{cmi}$ and the operational amplifier common-mode input $V_{cmo}$[2]. The two values, $V_{cmi}$ and $V_{cmo}$, are independently set. $V_{cmi}$ is tied to the middle of the supply voltage to take advantage of the rail-to-rail output capability of the previous integrator, while $V_{cmo}$ has a low value

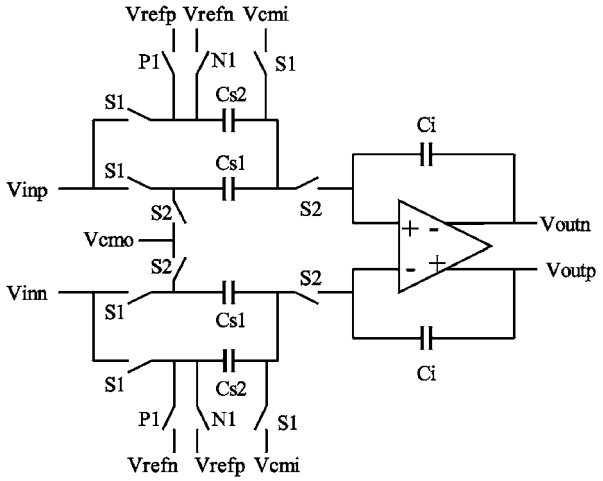


Fig. 7. SC integrator architecture.

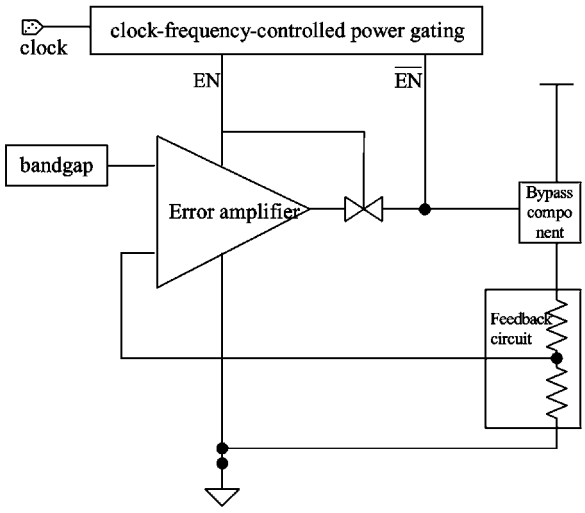


Fig. 8. LDO controlled by a clock frequency.

falling inside the common-mode input range of the PMOS-input amplifier. Another advantage of the SC integrator is the good control of capacitor ratios. In a sigma-delta modulator, the better control of each path gain means that the decrease of the modulator performance due to coefficient variations can be minimized.

The LDO controlled by a clock frequency is a central control unit of the digital pre-amplifier. The LDO generates all the supply and reference voltages, and supports a standby mode controlled by the clock frequency[5]. The LDO consists of a bandgap reference, an error amplifier, a bypass component, a feedback circuit and a clock-frequency-controlled power gating. Figure 8 shows the LDO architecture.

The bandgap is a voltage reference, which must be well-defined and insensitive to process, temperature, power supply and load variations. The resolution of the digital pre-amplifier is limited by the precision of the bandgap reference voltage over the supply voltage and operating temperature ranges. The bandgap voltage reference is required to exhibit both high power supply rejection and a low temperature coefficient, and it is probably the most popular high performance voltage reference used in integrated circuits today[6]. Figure 9 shows a low voltage, low power CMOS bandgap voltage reference, which

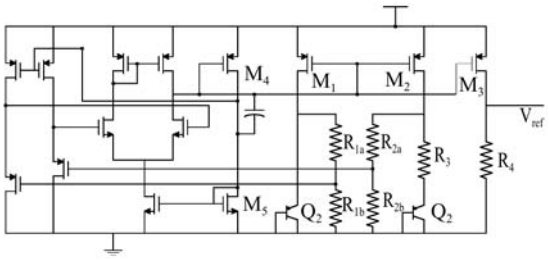


Fig. 9. Low voltage, low power CMOS bandgap.

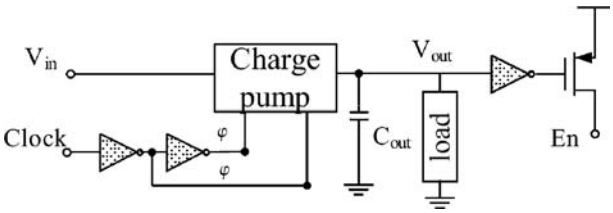


Fig. 10. Clock-frequency-controlled power gating.

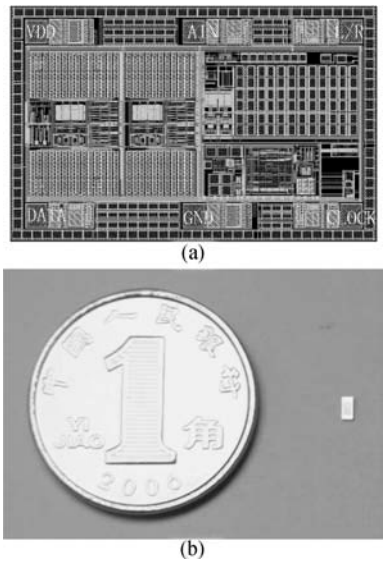


Fig. 11. (a) Layout of the digital pre-amplifier; (b) Size of the digital pre-amplifier chip.

supports a voltage range from 0.9 to 3.6 V and a temperature range from −40 to 125 °C. The bandgap generates a 601.8 mV reference voltage, consumes 5.18 $\mu$A current and delivers a reference voltage varying by less than 0.17% as a result of supply voltage, temperature and process changes.

Clock-frequency-controlled power gating, which is shown in Fig. 10, monitors the clock of the digital pre-amplifier. When the clock frequency is lower than the standby frequency, the power gating outputs a sleep signal, causing the digital pre-amplifier to enter the standby mode. Contrary, when the clock frequency exceeds the standby frequency, the power gating sends a wake-up signal, and the digital pre-amplifier enters the normal mode. Since the standby frequency is not very accurate, the design of the power gating can utilize a charge pump.

The output voltage of the charge pump is directly proportional to the clock frequency. Using this characteristic, we design a simple low-current charge pump. When the clock frequency reaches a certain level, the output voltage of the charge pump exceeds the threshold voltage of the inverter causing it to send the enable signal, En. Likewise, when the clock frequency is below the standby frequency, the signal En is disabled. In this way, we use the clock frequency to control the power supply.

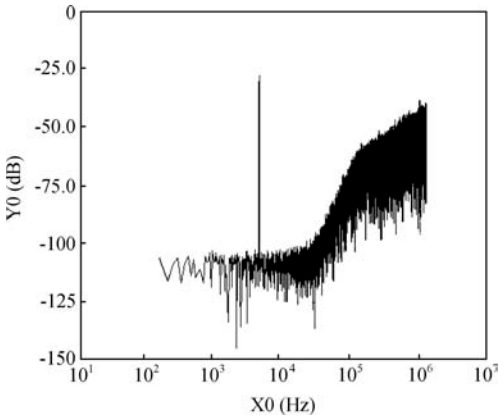


Fig. 12. FFT spectrum with –26 dBFS 4.375 kHz input.

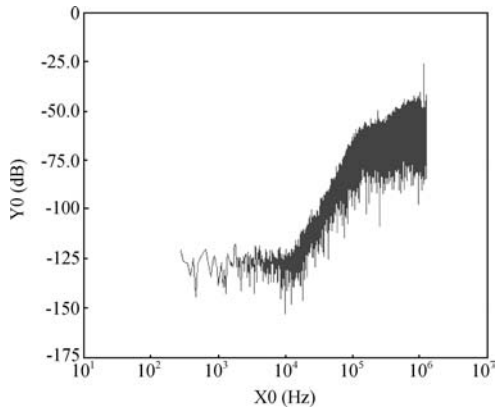


Fig. 13. FFT spectrum with noise.

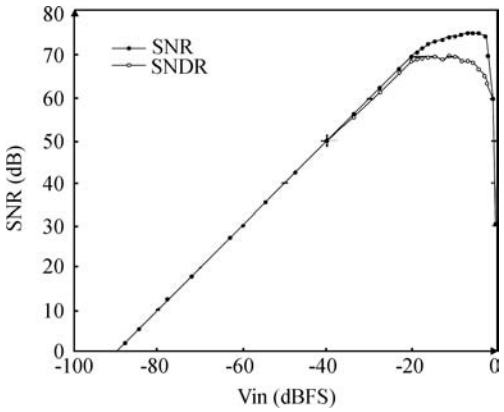


Fig. 14. Measured SNR and SNDR.

## 4. Measurement results

The whole digital pre-amplifier was fabricated in a 0.18 $\mu$m one-poly four-metal CMOS process. It dissipates about 540 $\mu$W and uses a single 1.8 V supply. The chip area including I/O pads is approximately 0.96 mm$^2$. The whole layout and product after tapeout are shown in Figs. 11(a) and 11(b).

Figure 12 shows a fast Fourier transformation (FFT) plot with a –26 dBFS 4.375 kHz input. The SNR is measured to be

Table 2. Performance summary.

| Parameter | Value |
|---|---|
| Dynamic range | 88 dB |
| SNR | 75 dB |
| Peak SNDR | 68 dB |
| PSRR | –65 dBFS |
| Equivalent input referred noise | 5 $\mu$Vrms |
| Power supply | 1.6–3.5 V |
| Modulator power consumption | 465 $\mu$W |
| LDO power consumption | 35 $\mu$W |
| Bandgap power consumption | 10 $\mu$W |
| Total power consumption | 540 $\mu$W |
| Standby current | $< 10$ $\mu$A |
| Clock freq. | 1–4 MHz |

Table 3. Performance comparison.

| Ref. | [4] | [1] | [11] | This work |
|---|---|---|---|---|
| Tech ($\mu$m) | 0.18 | 0.5 | 0.065 | 0.18 |
| $V_{DD}$ (V) | 1.8 | 2.2 | 1.5 | 1.8 |
| $f_B$ (kHz) | 80 | 3.4 | 20 | 30 |
| Power ($\mu$W) | 5000 | 200 | 2200 | 540 |
| Peak SNDR (dB) | 76 | 70 | 77 | 68 |
| DR (dB) | 81 | 80 | 95 | 88 |
| $\text{FOM}_{\text{SNR}}$ (pJ) | 6.1 | 11.4 | 9.5 | 4.4 |
| $\text{FOM}_{\text{DR}}$ (pJ) | 3.4 | 3.6 | 1.2 | 0.4 |

aboud 75 dB. Figure 13 shows the FFT plot with noise. Figure 14 shows the measured SNR and signal-to-noise-distortion-ratio (SNDR) for a 4.375 kHz input signal. A dynamic range (DR) of 88 dB is achieved in a 20 kHz signal bandwidth.

The results are summarized in Table 2. The figure of merit (FOM) of the converter is determined as

$$\text{FOM}_{\text{SNR}} = \frac{P}{2f_{\text{B}}2^{(\text{peakSNDR}-1.76)/6.02}}, \tag{6}$$

$$\text{FOM}_{\text{DR}} = \frac{P}{2f_{\text{B}}2^{(\text{DR}-1.76)/6.02}}, \tag{7}$$

where $P$, $f_{\text{B}}$, DR, peakSNDR, denote the power consumption, signal bandwidth, dynamic range (in dB) and peak SNDR (in dB), respectively.

Table 3 shows a performance comparison between different designs found in the literature and this work. The digital pre-amplifier of this work operates at a 30 kHz signal bandwidth with only 540 $\mu$W power dissipation and achieves $\text{FOM}_{\text{SNR}} = 4.4$ pJ and $\text{FOM}_{\text{DR}} = 0.4$ pJ, which are small compared with other designs.

## 5. Conclusion

Measurement results show that the dynamic range performance of our digital pre-amplifier is 88 dB, the equivalent input referred noise is 5 $\mu$Vrms, the power consumption is 540 $\mu$W in normal mode, and the standby current is under 10 $\mu$A. Due to its properties, our digital pre-amplifier is well suited for use in the new generation of advanced audio systems.

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