Overlay mark optimization for thick-film resist overlay metrology

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Abstract: For thick resist implant layers, such as a high voltage P well and a deep N well, systematic and uncorrectable overlay residues brought about by the tapered resist profiles were found. It was found that the tapered profile is closely related to the pattern density. Potential solutions of the manufacturing problem include hardening the film solidness or balancing the exposure density. In this paper, instead of focusing on the process change methodology, we intend to solve the issue of the overlay metrology error from the perspective of the overlay mark design. Based on the comparison of the overlay performances between the proposed overlay mark and the original design, it is shown that the optimized overlay mark target achieves better performance in terms of profiles, dynamic precision, tool induced shift (TIS), and residues. Furthermore, five types of overlay marks with dummy bars are studied, and a recommendation for the overlay marks is given.

Key words: overlay metrology error; dynamic precision; tool induced shift; statistical process control; depth of focus; exposure latitude

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1. Introduction

As the semiconductor device geometry shrinks down to 100 nm, requirements for overlay accuracy have become increasingly strict even for some non-critical implant layers. One important contributor to the overlay error is the overlay metrology uncertainty. In semiconductor manufacturing, a rather thick resist of 3 to 4 μm is commonly used for high-energy well implant layers (e.g., high voltage P wells, deep N wells, etc.). Typically, a poor uniformity for the overlay was observed[1, 2]. Although there are some recent studies focusing on the CD-SEM metrology of the overlay residues[3], the overlay tools in current foundries are mainly optical-based tools. These are limited by the achievable optical resolution. There are also other papers addressing this metrology tool capability induced problem by optimizing the lithography process[1, 2]. In this paper, instead of focusing on the process change methodology, we aim to solve this manufacturing issue from the overlay mark optimization perspective. We also aim to solve the issue of the overlay metrology error by applying optimized overlay marks with dummy bars.

2. Problem definition and diagnosis

In semiconductor fabrication, our box-in-bar overlay metrology shows a large systematic and uncorrectable intra-field error for thick resist implant layers since steppers are unable to magnify independently in the X and Y directions. Figure 1 shows an example of the overlay raw map and the residue vector map. It badly impacts the overlay performance and may lead to wrong parameter corrections in the feedback system. Figure 2 presents the overlay statistical process control (SPC) chart of the 0.15-μm technology high voltage N well (HVNW) layer. Product 1 and product 2 have the same process condition, but different layout designs. Wafer level X direction 3sigma for product 2 suffers out-of-specification (OOS) even if the corresponding parameter such as the shot magnification is compensated.

In order to find the root cause of the overlay issue, a test reticle of overlay marks with symmetric and asymmetric pattern densities is examined. As shown in Fig. 3(a), the left region of the shot center overlay mark is the dark area, while the right region has a clear tone. For the overlay mark of the shot edge presented in Fig. 3(b), the surrounding region is mainly dark. Figure 4 shows the residue vector map, in which the pattern density dependent residues are noted. It is found that overlay marks in the shot center have a relatively larger residue than those at the shot edge. Consequently, further cross-section investigations are carried out to find the root cause of the large uncorrectable residues. In order to make it consistent among the layouts, SEM images, and the cross-section view, the layouts and the SEM images are rotated by 90 degree anticlockwise. The inspection under an SEM illustrates that an asymmetric tapered overlay box profile exists, which leads to the inaccurate signal reading. The cross-section view of the overlay inner box also proves this hypothesis. Figures 5 and 6 illustrate an SEM picture of the asymmetric overlay inner box and the cross-section views of the profile of the shot center and the shot edge overlay marks. This loading effect can be further clarified by another test structure. Figure 7 presents the layout

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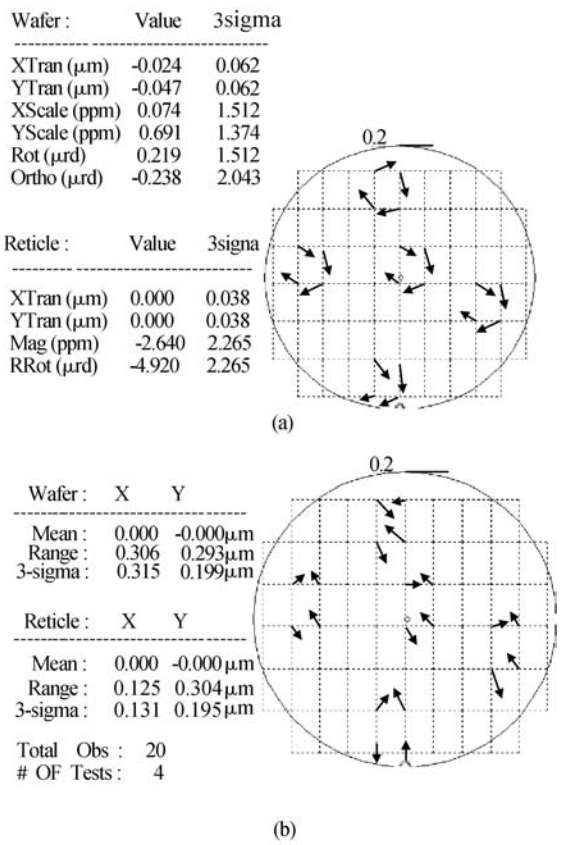

Fig. 1. (a) Overlay raw map and (b) residue map of the thick-film resist implant layer. The residues of the wafer level 3sigma *X* and 3sigma *Y* reach 315 nm and 199 nm, respectively. The residues of the reticle level 3sigma *X* and 3sigma *Y* are 131 nm and 195 nm, respectively.

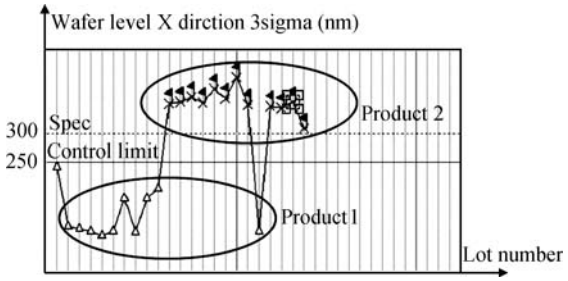

Fig. 2. Overlay SPC chart of 0.15 μm HVNW layer. (*X* direction 3sigma.)

of the test structure and the SEM image of the lower four trench bars. The trend-down of the slope width from the exterior trench to the interior one shows the alleviation of the loading effect introduced by the pattern density asymmetry. This test illustrates how to solve the overlay metrology error issue by balancing the local pattern density asymmetry. The details will be discussed in the next section.

3. The overlay mark optimization

Previous studies tried to solve this issue from the process change perspective[1, 2]. According to Yet[2] and Grandpierre[1], in order to harden the film solidness, various bake settings are proposed. These settings typically involve

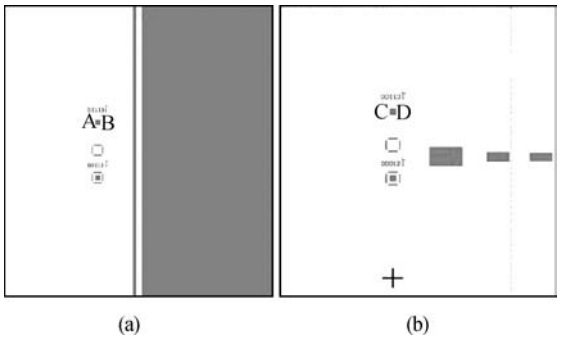

Fig. 3. Different pattern densities exist between (a) the shot center and (b) the shot edge. The dark area is the clear tone, while the white area is the dark tone.

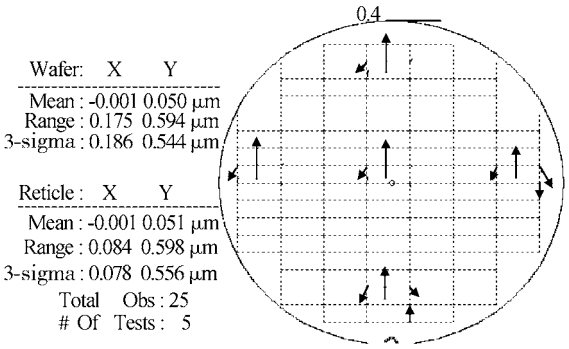

Fig. 4. Overlay residue differences between the shot center and the shot edge.

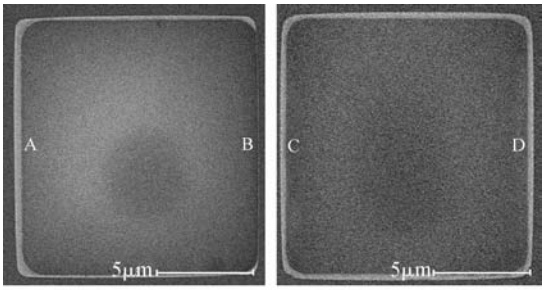

Fig. 5. SEM images of the inner box of (a) the shot center and (b) the shot edge.

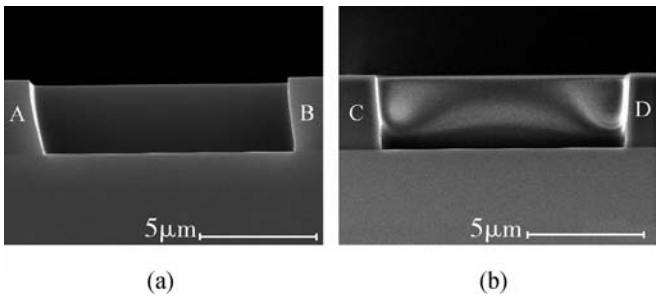

Fig. 6. Cross-section view of the inner box of (a) the shot center and (b) the shot edge.

changing the soft bake temperature or the post development bake conditions. However, applying new bake settings involves a series of process margin checks, such as the depth of focus (DOF) and the exposure latitude (EL). Furthermore, new bake settings will introduce different bake temperatures to the in-line lithography process, which will impact the in-line

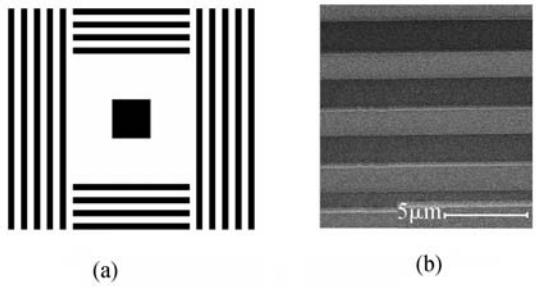

Fig. 7. (a) Another test structure; (b) SEM image of the lower four trench bars. The trend-down of the slope width from the exterior to the interior shows the alleviation of the loading effect introduced by the pattern density asymmetry.

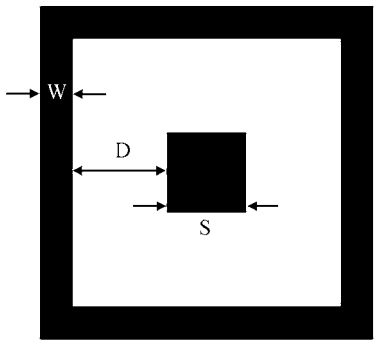

Fig. 8. Layout of the optimized overlay mark design.

throughput. Instead, we aim to solve this manufacturing issue from the overlay mark optimization perspective. According to the SEMI standards' recommendation, the labels, the border lines, the indicator marks, or any other adjacent features should be avoided to make patterns independent and symmetry be designed as circumstances permit[4, 5]. With the shrinking scribe-line and the thick resist film process, the device layout asymmetry has a significant impact on the resist profiles of the overlay marks. As a result, how to make the overlay marks independent turns out to be a serious problem. In this paper, an optimized overlay mark with dummy bars is proposed to balance the exposure density without changing the lithography process. In this study, the box in bar metrology is utilized. Figure 8 shows the layout of the proposed overlay mark design, which consists of three key parameters: the width of the main mark S, the distance between the main mark and the dummy bar D, and the width of the dummy bar W. In this paper, S is fixed to 12 μm. Five types of dummy bars are studied (W = 2 μm / D = 14 μm, W = 6 μm / D = 14 μm, W = 10 μm / D = 14 μm, W = 6 μm / D = 10 μm, W = 6 μm / D = 18 μm).

4. Results and discussions

4.1. Profile verification

Figures 9(a) to 9(e) show the SEM images of the inner box of the optimized overlay marks. By comparing the five images in Fig. 5, it is found that more symmetric profiles are possible. Moreover, the overlay mark with a larger W and a smaller D shows a better performance than the other overlay

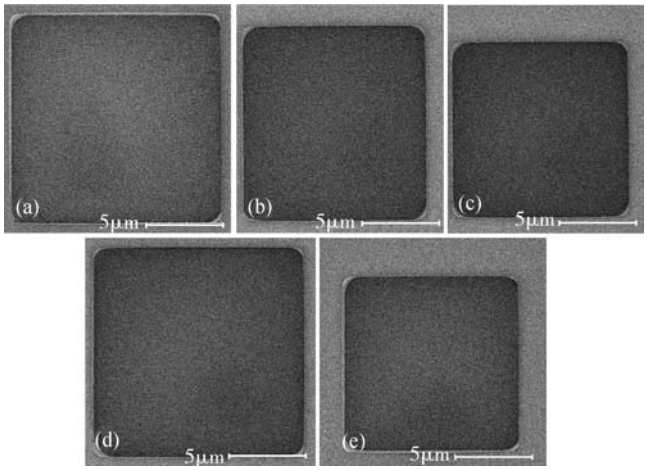

Fig. 9. SEM images of the inner box with different dummy bar targets. (a) W = 2 μm / D = 14 μm; (b) W = 6 μm / D = 14 μm; (c) W = 10 μm / D = 14 μm; (d) W = 6 μm / D = 10 μm; (e) W = 6 μm / D = 18 μm.

marks in the SEM view of the profile. This can be theoretically explained by the fact that the wider dummy bars with a smaller main-to-dummy distance will dominate the local loading effect more than the narrower dummy pars with a larger main-to-dummy distance, by alleviating the impact introduced by the surrounding structures. This hypothesis can be further illustrated in the following discussion. However, W is limited by the available space in the scribing line and D is limited by the resolution capability of the resist line between the main mark and the dummy bars.

4.2. Dynamic precision and TIS

The dynamic precision is defined as three times the standard deviation of the results of a series of measurements of the same overlay mark, when the measurements are done in a dynamic loop (including wafer alignment, mark acquisition, and measurement). The tool induced shift (TIS) is defined as the average of the overlay measurements performed on a given overlay mark before and after rotation by 180 degrees.

Dynamic precision and TIS terms from the different overlay marks are shown in Fig. 10. It is found that the optimized overlay marks show the better performance with the lowest absolute values of the dynamic precision, the TIS mean, and the TIS 3sigma. In addition, the overlay mark with a larger W and a smaller D shows a better performance.

4.3. Correctable terms comparison

Table 1 illustrates the correctable terms for each type of overlay marks, when using the same model. The parameters include translation, scaling, orthogonality, wafer rotation, field magnification, and field rotation. There is a trend-down for most of the correctable parameters, especially for the magnification and the reticle rotation.

4.4. Residue comparison

In order to compare the residue with the baseline, we expose the same wafer twice with resist thicknesses of 3.5 μm

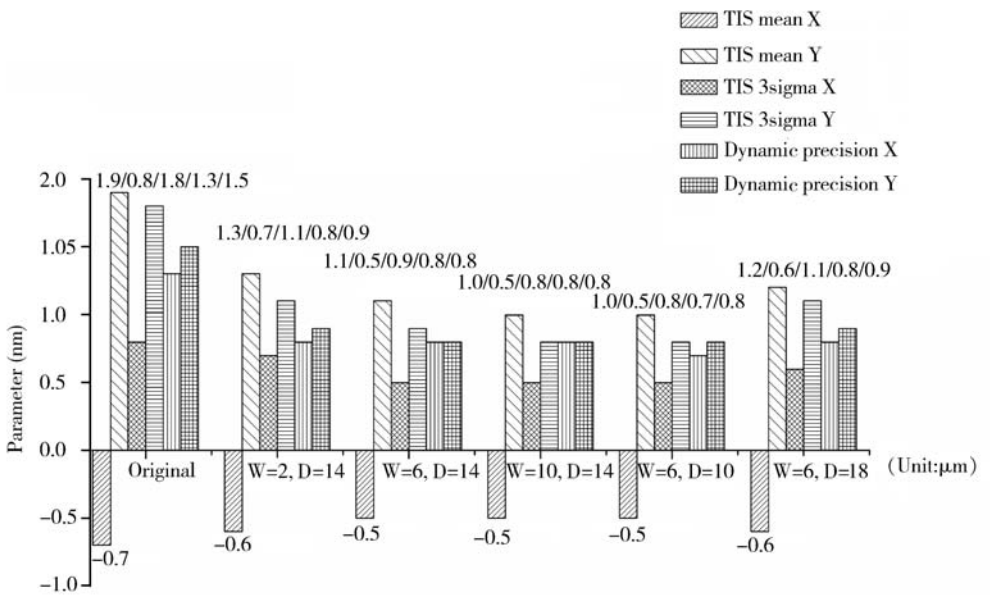

Fig. 10. TIS mean,TIS 3sigma,and dynamic precision for various overlay targets.

Table 1. Correctable terms for various overlay targets.

		Original	$W = 2$ / D = 14 (μm)	$W = 6$ / D = 14 (μm)	$W = 10$ / D = 14 (μm)	$W = 6$ / D = 10 (μm)	$W = 6$ / D = 18 (μm)
Wafer parameters	Translation X (μm)	−0.024	−0.02	−0.017	−0.017	−0.016	−0.019
	Translation Y (μm)	−0.047	−0.035	−0.035	−0.034	−0.033	−0.036
	Scaling X (ppm)	0.123	0.074	0.021	0.02	0.02	0.035
	Scaling Y (ppm)	0.691	0.202	0.029	0.026	0.027	0.061
	Wafer rotation (μrd)	0.219	0.012	−0.049	−0.05	−0.048	−0.033
	Orthogonality (μrd)	−0.238	0.1	0.052	0.05	0.051	0.074
Field parameters	Magnification (ppm)	−2.64	0.846	0.283	0.281	0.28	0.461
	Reticle rotation (μrd)	−4.92	−1.56	−0.15	−0.12	−0.14	−0.6

and 430 nm. After the 3.5 μm resist overlay measurement is finished, the wafer is sent to be reworked and then a 430 nm resist overlay metrology test is carried out with the same process conditions and the original overlay mark. Since the asymmetric profile induced overlay metrology errors can be ignored for the thin resist film, the overlay result of the thin resist film is supposed to be the baseline in this experiment. Figure 11 presents the residue analysis result. It is found that the optimized overlay mark with a larger W and a smaller D shows the closest performance to the "baseline". As is shown in Fig. 11, the 3sigma values of the five shots have decreased to 41 nm and 34 nm for X and Y directions, respectively, by using dummy bars of $W = 6$ μm / $D = 14$ μm.

From the above wafer data, it is found that a larger W and a smaller D tend to improve the overlay mark fidelity and lead to an overlay performance, which is closer to the baseline. However, the parameter W is limited by the available space in the scribing line, and D is limited by the resolution capability of the resist line between the main mark and the dummy bars. On the other hand, when the loading effect has been alleviated by the dummy bars with the increment of W and the decrement of D over a certain limit, the overlay performances become similar to each other. As a result, it is not necessary to design an overlay mark with excessively larger W and smaller D. Following our study, an overlay mark with $W = 6$ μm / $D = 14$ μm dummy bars is recommended.

5. Conclusion

In our study, systematic uncorrectable overlay residues are typically observed for thick resist implant layers. The cross-section analysis shows that an asymmetric resist profile existed, causing an inaccurate signal reading during the overlay measurement. Further studies find a correlation between the pattern density symmetry and the overlay mark profiles. Potential solutions for the issue resulting from the metrology tool capability include either applying new bake settings to change the profile shape or looking for a new approach to balance the pattern density. However, the lithography process change requires various condition checks, such as DOF, EL, and so on. This results in an increased engineering time. Moreover, higher bake temperatures will make it difficult to manage the in-line lithography process and the in-line throughput decreases. Instead of focusing on the process change methodology, another approach is proposed in this paper. In order to achieve the goal of loading effects correction, it applies optimized overlay marks with dummy bars. This methodology does not lead to a process change. Based on the comparison

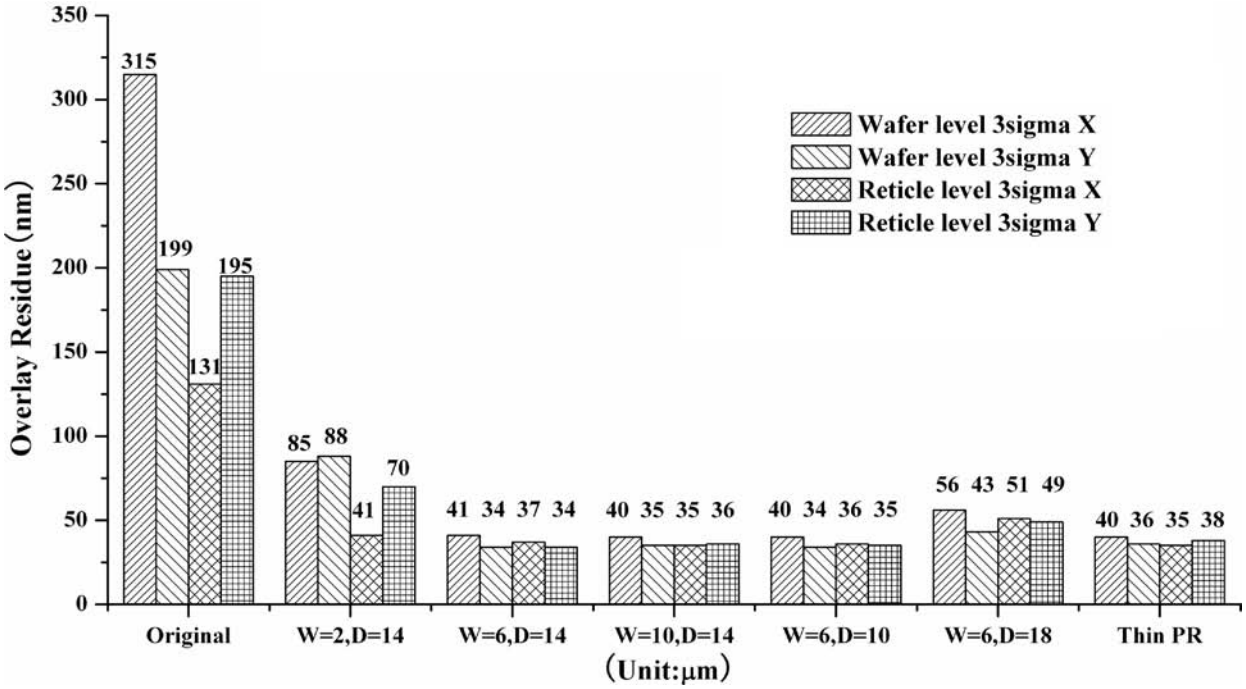

Fig. 11. Overall overlay residue performance.

of the overlay performances between the proposed overlay mark and the original design, it is shown that the optimized overlay mark target achieves a better performance in terms of profiles, dynamic precision, tool induced shift (TIS), and residues. Furthermore, it is found that a larger width of the dummy bars and a smaller main-to-dummy distance tends to improve the overlay mark fidelity and leads to a overlay performance, which is closer to the baseline. However, when the loading effect has been alleviated by the dummy bars, a further increment of the dummy bar width and a decrement of the main-to-dummy distance will not contribute significantly to the improvement of the overlay performances. So, it is not necessary to design an overlay mark with excessively wide dummy bars and a small main-to-dummy distance. Following our study, an overlay mark with $W = 6\ \mu$m/$D = 14\ \mu$m dummy bars is recommended.

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