Characteristics of vertical double-gate dual-strained-channel MOSFETs*

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Abstract: A novel device structure with a vertical double-gate and dual-strained channel is presented. The electrical characteristics of this device with a gate length of 100 nm are simulated. With a Ge content of 20%, the drain currents of the strained-Si NMOSFET and the strained-SiGe PMOSFET compared to the universal SOI MOSFETs are enhanced by 26% and 33%, respectively; the risetime and the falltime of the strained-channel CMOS are greatly decreased by 50% and 25.47% compared to their traditional Si channel counterparts. The simulation results show that the vertical double-gate (DG) dual-strained-channel MOSFETs exhibit better drive capability, a higher transconductance, and a faster circuit speed for CMOS compared to conventional-Si MOSFETs. The new structure can be achieved by today's semiconductor manufacturing level.

Key words: vertical; double-gate; dual-strained-channel
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1. Introduction

Conventional materials and device structures are approaching their physical limits since the feature sizes of integrated circuits (IC) are entering the deep-submicron (DSM) field. Problems, such as the short channel effect (SCE), the threshold voltage shift, and the leakage current increase, will more significantly affect the device performances. Therefore, research on novel device structures is an urgent topic. Adopting strained Si and strained GeSi as the channels individually for NMOS and PMOS transistors can effectively increase the carrier mobility, thus, increasing the drain currents and improving circuit speed[1,2]. In addition, new vertical single-gate and multi-gate complementary metal-oxide-semiconductor (CMOS) structures seem to satisfy the needs for future SOC applications with smaller feature sizes[3]. Vertical structures will replace plane structures for logical and for memory devices[4].

In this paper, a novel vertical double-gate and dual-strained-channel CMOS device is presented, which combines a vertical double-gate with strained-Si and strained-GeSi channels, thus, increasing the electron and hole mobility and the device's drive capability. Meanwhile, the on–off time can be reduced to satisfy the increasing speed requirement of circuits. The characteristics of the new devices' PMOS, NMOS, and CMOS transistors are simulated and compared with conventional Si-channel PMOS, NMOS, and CMOS transistors of the same size.

2. Device structural and physical models

The schematic cross section view of the novel vertical double-gate NMOSFET/PMOSFET and vertical double-gate dual-strained-channel CMOSFET are presented in Fig. 1. The structure and process parameters of the devices are also given in Table 1, where strained-Si is used as the NMOS channel and strained-GeSi as the PMOS channel. The widths are both 1 μm, while in the CMOS simulation the width of the PMOS is twice as wide as the width of the NMOS. The way to introduce a strained channel is to grow a strained-Si layer on relaxed-GeSi, thus, increasing the electron and hole mobility significantly. The mobility increase will enhance the drive capacity of the device. Since the basic device structures remain unchanged when strained materials are introduced, a process incompatibility can be avoided; this is of great advantage in improving the device performance. Compared with a single-gate device, the double-gate MOSFETs behave better in the gates controlling channels, avoiding SCE as well as enhancing the drive current of the devices[5].

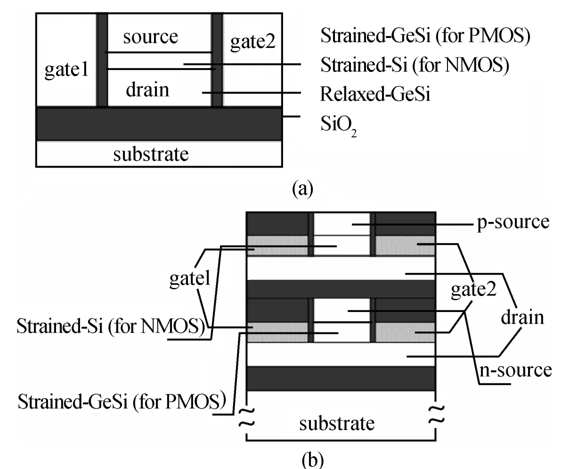

Fig. 1. Schematic cross section views of (a) the vertical double-gate NMOSFET/PMOSFET and (b) the vertical double-gate dual-strained-channel CMOSFET.

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Table 1. Geometric and process parameters of the devices.

Device type	NMOS	PMOS
Channel length (nm)	100	100
Gate doping concentration (cm^{-3})	As, 1×10^{20}	B, 1×10^{20}
S/D doping concentration (cm^{-3})	As, 1×10^{20}	B, 1×10^{20}
S/D junction depth (nm)	10	10
Gate oxide thickness (nm)	5	5
Strained-Si doping concentration (cm^{-3})	5×10^{17}	5×10^{17}
Strained-GeSi doping concentration (cm^{-3})	5×10^{17}	5×10^{17}

The characteristics of the devices are simulated with the two-dimensional simulation software ISE TCAD, considering second order physical effects in the DSM. When simulated, the accurate hydrodynamic model and the e/h quantum potential model are adopted as energy transportation models. The e/h high field saturation model, the mobility degradation induced by ionized impurity scattering (the doping dependence model) and the vertical electric field in the channel (the enorma model) are considered in the mobility model; the band to band model, the SRH (tunneling doping dependence) model, the Auger and e/h avalanche models are adopted in the recombination model, which make the simulated results reflect the reality much better.

In addition, we modified the physical model of the strained Si material in the simulation software, which is very important for the novel structure. In order to verify the model, we simulated the strained Si MOSFET proposed by Rim *et al.*[6] using the modified model. Because we simulated the de- vice with w = 1 μm, the drain current should be half of the current of Rim's device. The results in Fig. 2 show that the simulated output characteristics correspond to the curves in the paper of Rim *et al.*, indicating that the models we used are accurate.

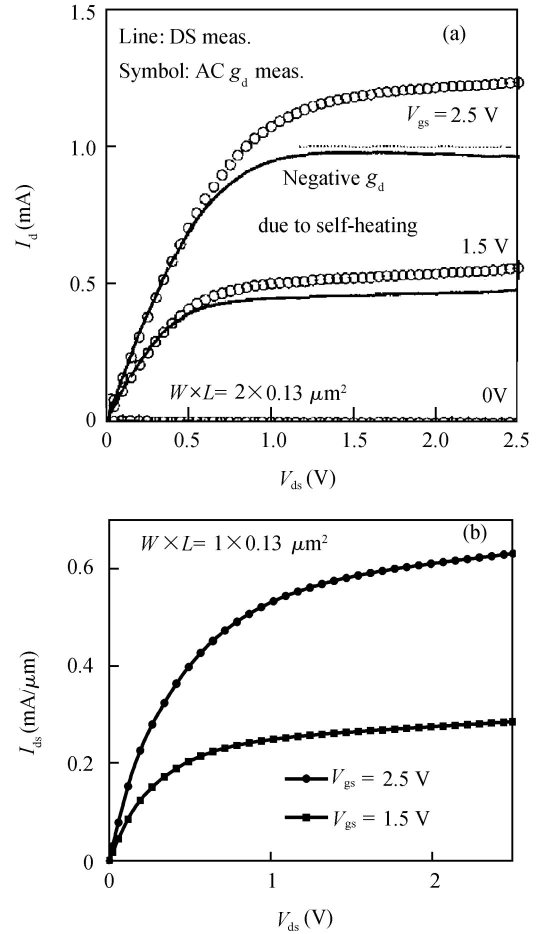

Fig. 2. Output characteristics of the same device: (a) The curves of Rim *et al.*[6]; (b) The curves simulated in this paper.

3. Analysis of device characteristics

In order to analyze the characteristics of the new devices, conventional Si-channel vertical double-gate devices are also simulated with the same size and structure, except that the strained channel is replaced by normal Si material.

3.1. Analysis of NMOS characteristics

A comparison of the transfer characteristics and the output characteristics of the strained-Si channel NMOSFET and the conventional Si channel NMOSFET is shown in Figs. 3(a) and 3(b), respectively, where in the strained material the Ge fraction is taken to be 0.2. From the figure, it can be seen that the drain current of the strained-Si device is enhanced more significantly than that of the Si device; the current of the former is 4157 μA/μm, while the current for the latter is 3322 μA/μm, i.e., an increase of 26%. The reason for this increase is that in strained-Si NMOS the increase in the mobility is due to the reduction in the carrier (mainly electron) effective masses and in the scattering probabilities between energy valleys. The six-fold degeneracy energy valley of the Si conduction band will be divided into two groups: one is the doubly degeneracy energy valley, whose energy is lower than the original energy valley, and the other is the four-fold degeneracy energy valley, whose energy is higher than the original valley. The direction of the doubly degeneracy valley is perpendicular to the original one, while the four-fold one is parallel to the original one. The empirical value of the difference between the lower and the higher valleys is 0.6x eV, where x stands for the Ge fraction. The tensile stress of the upper layer increases when x increases; so, the electron mobility is increased. The increase in the mobility will enhance the drive capability of the NMOS[7].

The transconductance characteristics of a strained-Si material channel NMOSFET and a conventional Si channel NMOSFET are compared in Fig. 3(c). From this figure, we can see that when the voltages are biased at V_{gs} = 2 V and V_{ds} = 0.1 V, the transconductance g_m of a strained channel device

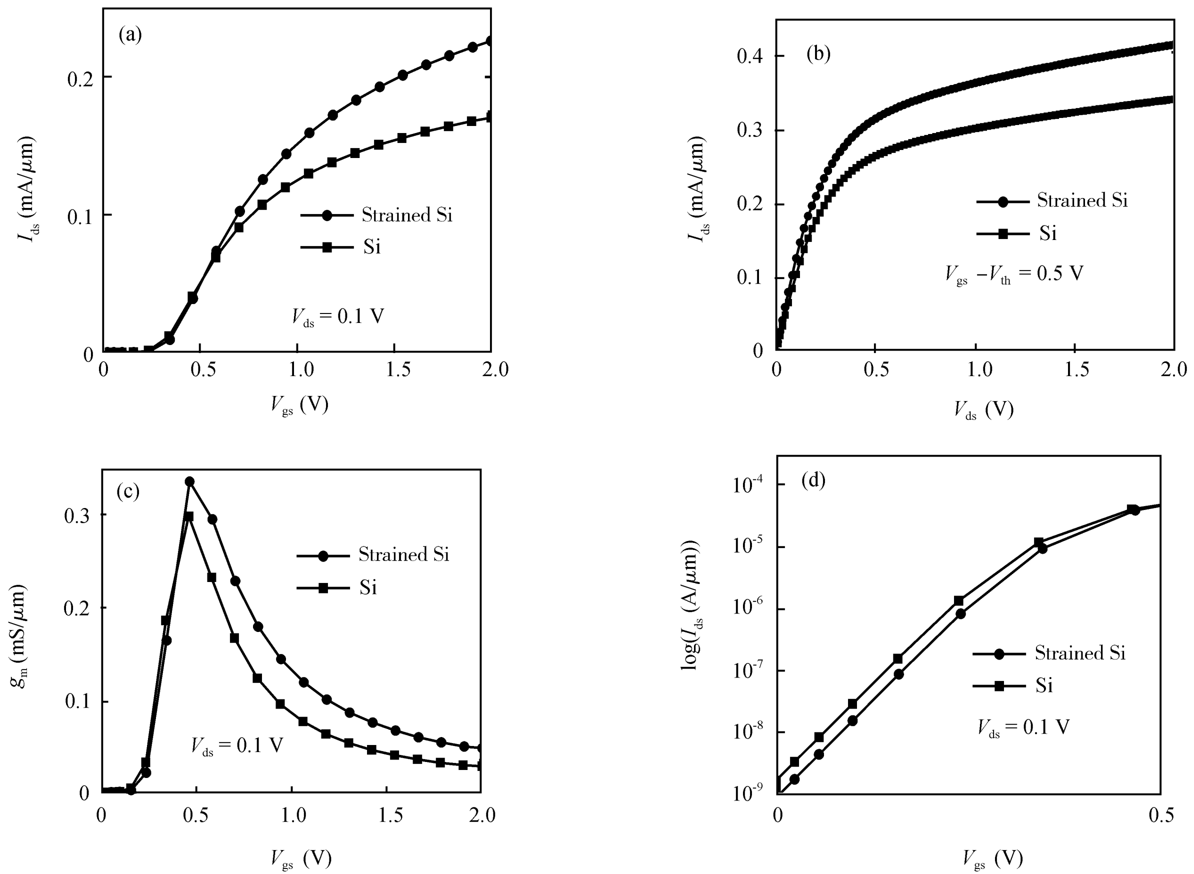

Fig. 3. Characteristics of strained-Si material channel NMOSFETs in comparison to conventional Si-channel NMOSFETs: (a) Transfer characteristics; (b) Output characteristics; (c) Transconductance characteristics; (d) Subthreshold characteristics.

and a Si channel device is 335.3 and 298.0 μS/μm, respectively; so, we can conclude that the gate control capability of the strained-Si channel NMOSFET is improved by 19%. The subthreshold characteristics of strained-Si material channel NMOSFETs and conventional Si channel NMOSFETs are illustrated in Fig. 3(d). S is 76.6 mV/dec for the strained-Si channel device, while it is 81.4 mV/dec for the Si channel device. Thus, the former shows better subthreshold characteristics and has better turn-off characteristics.

3.2. Analysis of PMOS characteristics

Figures 4(a) and 4(b) compare the transfer characteristics and output characteristics of the strained-GeSi channel PMOSFET and the conventional Si channel PMOSFET. From the figure, it can be seen that the drive capability of the strained-GeSi device is much better than that of the Si device. The current for the former is 1850 μA/μm, while the current for the latter is 1354 μA/μm, therefore increasing by 33%. In a strained-GeSi PMOS, the increase of the mobility results from the separation of the heavy and light energy bands in the Brillouin zone, resulting in lower scattering between bands. Meanwhile, the stress causes a change in the valence band profile and a reduction of the hole effective mass. So, the drive capability of PMOS is enhanced[8].

The transconductance characteristics of strained-GeSi material channel PMOSFETs and of conventional Si channel PMOSFETs are compared in Fig. 4(c). As shown in this figure, the transconductance $g_{\rm m}$ is 142.9 μS/μm for the strained channel device, while it is only 110.7 μS/μm for the Si channel device when $V_{\rm gs}$ is 2 V and $V_{\rm ds}$ is –0.1 V. Therefore, the transconductance is improving by 29%, and the gate control capability is enhanced. The subthreshold characteristics of the strained-GeSi channel PMOSFET and of the conventional Si channel PMOSFET are compared in Fig. 4(d). S is 93.4 mV/dec for the strained-GeSi channel, while it is 87.9 mV/dec for the Si channel. That is to say, when we introduce strained-GeSi to improve its drive capability, the subthreshold characteristics become worse[9]. This subthreshold degradation in GeSi PMOSs has been investigated by many people. Interface states at the front and back interfaces of the SOI layers can contribute to this subthreshold degradation. This degradation may be improved by several suitable advanced process steps.

3.3. Analysis of CMOS characteristics

The transient input–output characteristics of the vertical double-gate dual-strained-channel CMOS inverter and of the vertical double-gate dual-Si-channel CMOS are compared in Fig. 5. From the figure, we can see that the risetime and the falltime of the dual-strained CMOS are 20.00 and 24.56 ps, respectively; however, the risetime and falltime of the Si-channel CMOS are 30 and 30.69 ps. Thus, the risetime and falltime of the former are decreased by 50% and 25.47% over the latter, respectively. So, it can be concluded that the speed of the former is improved more significantly than the speed of the latter.

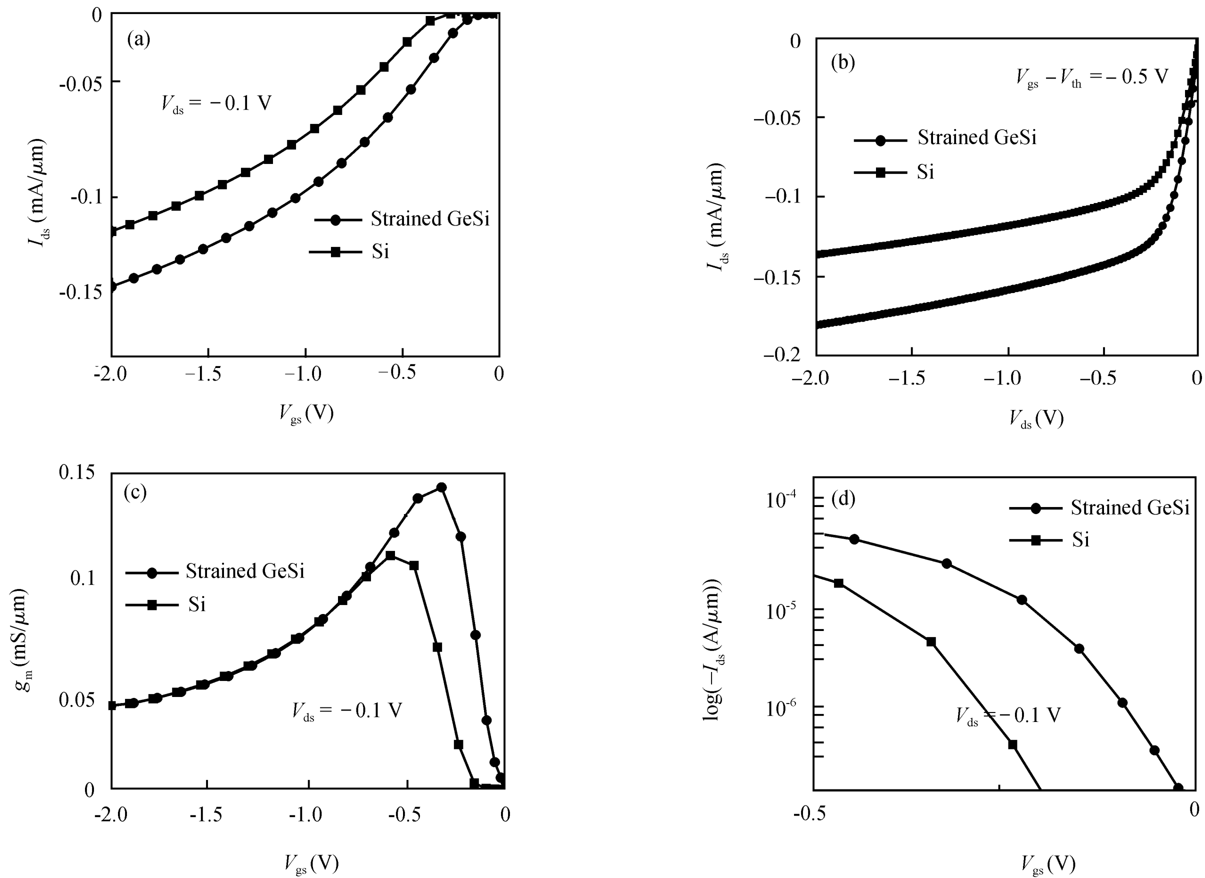

Fig. 4. Comparison of characteristics of strained-GeSi material channel PMOSFETs and conventional Si channel PMOSFETs: (a) Transfer characteristics; (b) Output characteristics; (c) Transconductance characteristics; (d) Subthreshold characteristics.

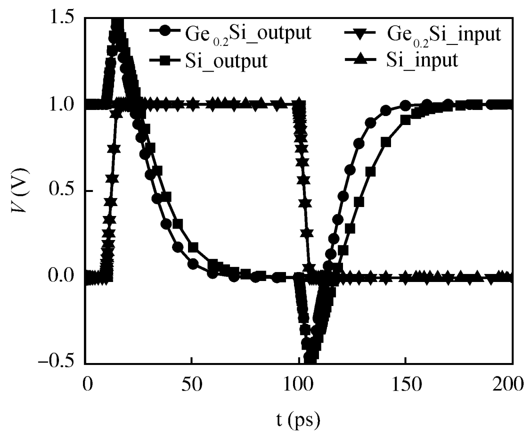

Fig. 5. Transient characteristics of the vertical double-gate dual-strained-channel CMOS inverter compared with the vertical double-gate dual-Si-channel CMOS.

This can be explained by the fact that by introducing strained-Si and strained-GeSi channels into vertical double-gate dual-strained-channel CMOS devices, the electron mobility in the NMOS and the hole mobility in the PMOS are both significantly increased. This increase improves the frequency characteristics of CMOS inverters, thus, allowing CMOS inverter to be used in higher frequency ranges.

4. Process implementation

The process of this kind of vertical double-gate dual-strained-channel CMOSFET presented in this paper can be realized under present process conditions. By referring to the relevant literature[11−14], the fabrication flow can be listed as follows:

(1) Deposit 100-nm polysilicon using LPCVD on a SOI (silicon-on-insulator) substrate; then deposit 150-nm SiO_2 on the polysilicon using LPCVD, as shown in Fig. 6(a).

(2) Etch the groove down to the Si layer and thermally grow the gate oxide to a thickness of 5 nm with a temperature below 700 °C for 8 h; deposit 100-nm Si_3N_4 to form a poly Si–SiO_3 stack, as shown in Fig. 6(b).

(3) Laterally etch the Si_3N_4 and gate oxide using RIE (reactive ion etching) and leave only the vertical direction; selectively implant a B concentration of 1×10^{20} cm^{-3} in the Si cap to form the drain; etch the Si_3N_4 in the vertical direction, as shown in Fig. 6(c).

(4)Grow *in situ* doped strained GeSi with an As concentration of 5×10^{17} cm^{-3} and *in situ* doped Si with a B concentration of 1×10^{20} cm^{-3} to form the source using selective area growth (SAG). At this point then PMOS is finished, as shown in Fig. 6(d).

(5) Deposit a low-temperature oxide (LTO) by LPCVD and polish the structure using CMP (chemical mechanical polishing); then bonding the polished LTO with relaxed GeSi (Ge

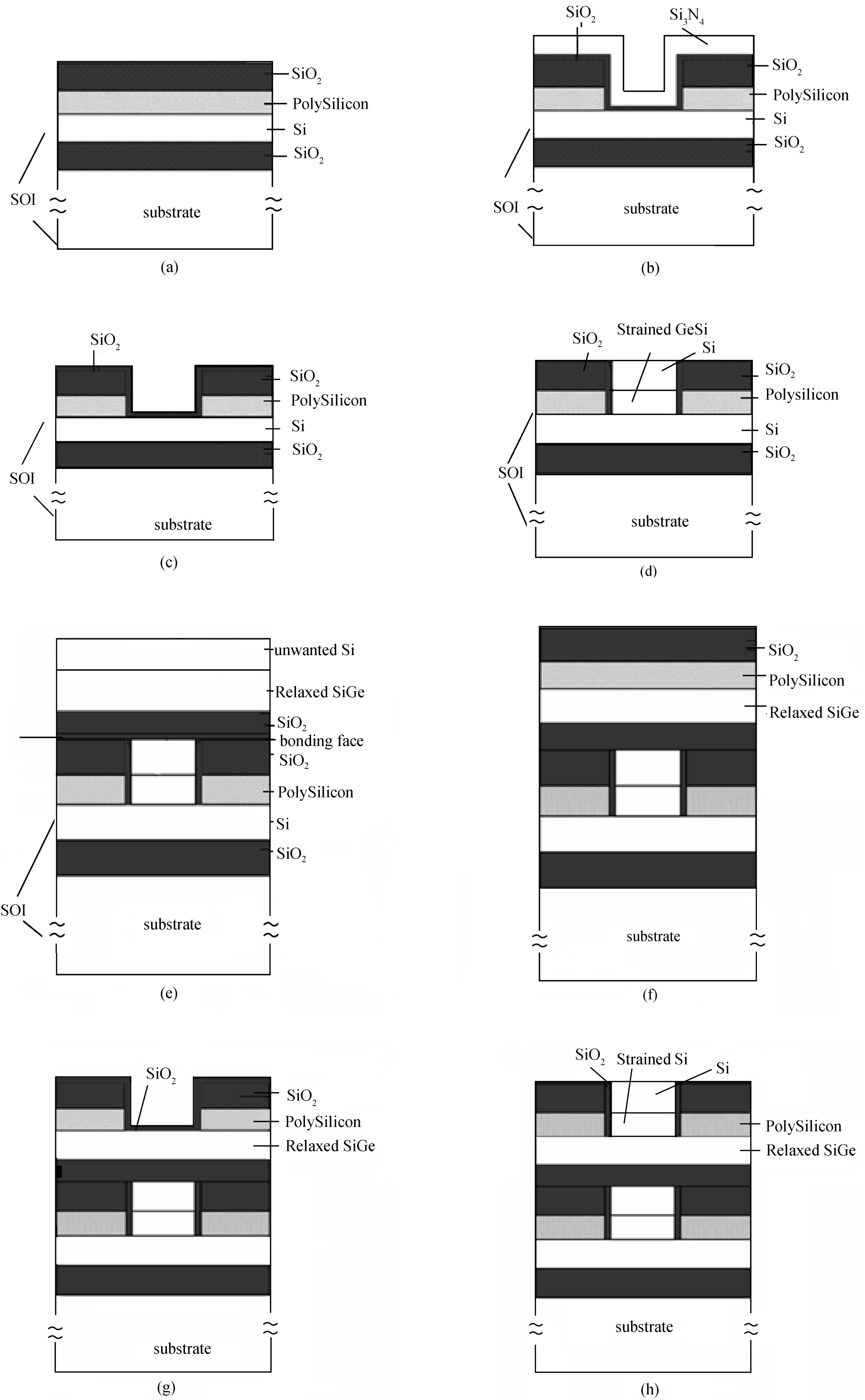

Fig. 6. Simplified process flow of the vertical double gate dual-strained channel CMOSFET.

content is 20%), which grows on a sacrificial silicon substrate on another wafer, as shown in Fig. 6(e).

(6) Remove the sacrificial silicon using an etch by CMP technology. Deposit 100-nm polysilicon using LPCVD, and deposit 150-nm SiO_2 on the polysilicon by LPCVD, as shown in Fig. 6(f).

(7) Etch the groove down to the GeSi layer and thermally grow 5-nm gate oxide at a temperature below 700 °C for 8 h; deposit 100-nm Si_3N_4 to form the poly Si–SiO_2 stack; then laterally etch the Si_3N_4 and the gate oxide by RIE and leave only the vertical direction; selectively implant an As concentration of 1×10^{20} cm^{-3} in the GeSi to form the drain; etch the Si_3N_4 in the vertical direction, as shown in Fig. 6(g).

(8) Grow *in situ* doped strained Si with a B concentration of 5×10^{17} cm^{-3} and *in situ* doped Si with an As concentration of 1×10^{20} cm^{-3} to form the source using SAG and polish the structure by CMP; at this point, then NMOS is finished as well. The finished CMOS structure is shown in Fig. 6(h).

5. Conclusion

In this paper a novel device structure with a vertical double-gate dual-strained channel is presented. The characteristics of the devices with a channel length of 100 nm of the NMOSFET, the PMOSFET, and the CMOS are individually simulated. To show the improvement over conventional channel devices, the characteristics of a Si channel, having the same structure and using the same process parameters, are also simulated. The results indicate that the strained-channel devices of the novel structures have a higher drive current, a higher gate control capability, and a higher transconductance. The transient characteristics show that this kind of CMOS performs better in terms of risetime and falltime, as compared to the conventional Si channel device. The outstanding performances show that a high frequency characteristic is obtained to satisfy the needs of more complicated SOC circuits.

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