Low-power wide-locking-range injection-locked frequency divider for OFDM UWB systems*

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Abstract: This paper describes a divide-by-two injection-locked frequency divider (ILFD) for frequency synthesizers as used in multiband orthogonal frequency division multiplexing (OFDM) ultra-wideband (UWB) systems. By means of dual-injection technique and other conventional tuning techniques, such as DCCA and varactor tuning, the divider demonstrates a wide locking range while consuming much less power. The chip was fabricated in the Jazz 0.18 μm RF CMOS process. The measurement results show that the divider achieves a locking range of 4.85 GHz (6.23 to 11.08 GHz) at an input power of 8 dBm. The core circuit without the test buffer consumes only 3.7 mA from a 1.8 V power supply and has a die area of 0.38×0.28 mm^2. The wide locking range combined with low power consumption makes the ILFD suitable for its application in UWB systems.

Key words: UWB; ILFD; frequency synthesizer; divide-by-two
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1. Introduction

The prospect of wireless date transmission at rates of hundreds of Mbps has drawn much attention from both academia and the industry to the ultra-wideband (UWB) system. Proposed by the multi-band orthogonal frequency division multiplexing (OFDM) alliance (MBOA), the entire UWB spectrum (from 3.1 to 10.6 GHz) is divided into 14 channels (bands) with a spacing of 528 MHz[1]. Usually, frequency synthesizers are employed in UWB transceivers to generate carriers for frequency hopping between different bands.

In phase locked loop (PLL)-based frequency synthesizers, the frequency divider (FD) is one of the most important building blocks and consumes a significant amount of power. More importantly, the power consumption of an FD will grow drastically with increasing operating frequency. Reducing the power consumption of the FD is, therefore, a critical issue in modern portable battery supplied equipment[2]. It remains a challenging task to design high-frequency dividers with low power dissipation.

Existing high-speed FDs can be categorized into three groups: flip-flop-based current-mode-logic (CML) FDs, regenerative dividers and ILFDs. CML FDs are widely used in high-speed PLLs due to their simple design and robust operation. However, they consume a significant amount of power at high input frequencies, which limits their applications in high-frequency low-power systems. Regenerative dividers can operate at very high frequencies (tens of gigahertz), but the main constrains are complex circuit implementation and large power dissipation. ILFDs are gaining popularity in recent years because they can reach higher operating frequencies and in the meantime dissipate less power[3]. Unfortunately, the ILFD has a narrow operating range and, more important, such a small operating range is also impacted by many factors, including the injected power and process variations.

In order to enhance the locking range of ILFDs and to extend their application potential, we propose in this paper a wide-locking-range ILFD, which is aiming at application in the frequency synthesizers for the high band groups (Group #3, #4, #5) of UWB systems. By utilizing both DCCA tuning together with varactor tuning and the dual-injection topology, the locking range of the presented ILFD is extended significantly. The principle of the injection locking and the concept of the proposed circuits are described and analyzed in detail, and the measurement results and a comparison with recently reported frequency dividers are also presented.

2. Principle of injection locking

2.1. Injection locking

Injection locking is a special type of forced oscillation in nonlinear oscillators. For a given free-running oscillator, either ring oscillator or LC tank-based oscillator, when perturbed by an external signal, its output frequency changes to that of the external signal when their frequencies are close. This concept can be illustrated with an LC oscillator perturbed by a small signal $I_{\rm INJ}$ having frequency $\omega_{\rm INJ}$, as shown in Fig. 1[4]. In the absence of the injected signal, the oscillator oscillates at its free-running frequency $\omega_0 = 1/\sqrt{\rm LC}$ and the current through the metal-oxide-semiconductor (MOS) transistors $I_{\rm M}$ is equal

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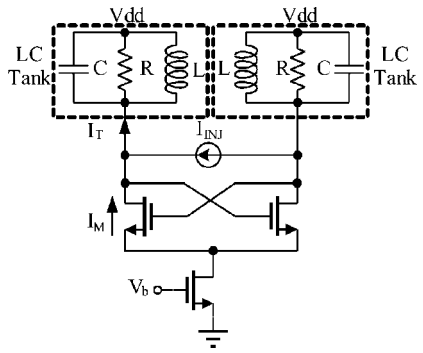

Fig. 1. LC oscillator under injection.

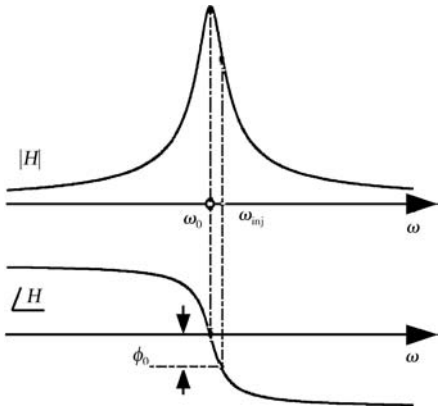

Fig. 2. Amplitude and phase of the LC tank impedance.

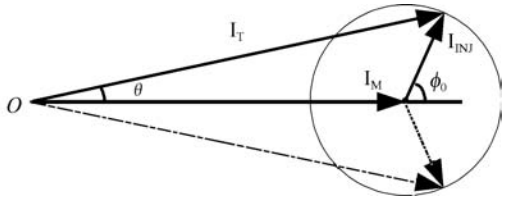

Fig. 3. Phasor diagram of the current signals in the LC oscillator.

to the tank current I_T in both amplitude and phase. When a small signal I_{INJ} with frequency $\omega_{INJ} \approx \omega_0$ is injected, it produces a phase difference between I_M and I_{INJ}. This forces the LC tank to oscillate at ω_{INJ} to contribute the necessary phase shift ϕ_0 in order to maintain $\vec{I}_T = \vec{I}_{INJ} + \vec{I}_M$, as shown in Fig. 2.

2.2. Locking range analysis

In order to investigate the locking range (the range of ω_{INJ} across which injection locking holds), we plot the phasor diagram of the signals in the oscillator in Fig. 3. The total current entering the tank, I_T, now has two components after signal injection: one is due to the transconductor current produced by the cross-coupled transistors, and the other is injected. Once the oscillator is locked to the injected frequency, the angle θ between the total tank current, I_T, and the transconductor current, I_M, must be equal to the phase shift created by the LC tank due to the shift of the oscillation frequency from ω_0 to ω_{INJ}. When ω_{INJ} moves away from ω_0, to compensate for the increasingly greater phase shift introduced by the tank, θ must also increase and it can be shown from Fig. 3 that,

$$\sin\theta = \frac{I_{INJ}}{I_T}\sin\phi_0 = \frac{I_{INJ}\sin\phi_0}{\sqrt{I_{INJ}^2 + I_M^2 + 2I_M I_{INJ}\cos\phi_0}}, \quad (1)$$

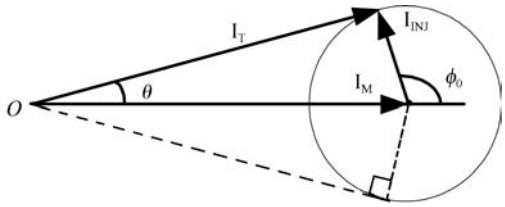

Fig. 4. Phasor diagram for maximum θ.

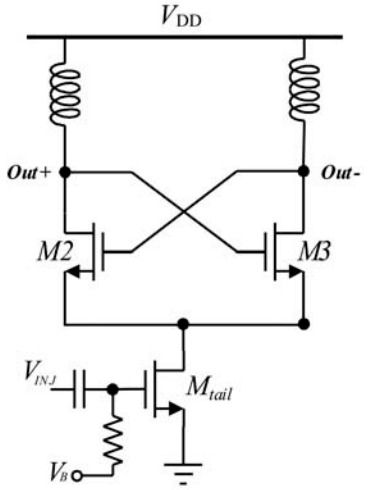

Fig. 5. Conventional divide-by-two ILFD.

which reaches a maximum of,

$$\sin\theta_{max} = \frac{I_{INJ}}{I_M} \text{ when } \cos\phi_0 = -\frac{I_{INJ}}{I_M}.$$

As depicted in Fig. 4, this condition translates to a 90° angle between the total current I_T and I_{INJ}. Then we get the following relations,

$$\tan\theta = \frac{I_{INJ}}{I_T} \text{ and } I_T = \sqrt{I_M^2 - I_{INJ}^2}. \quad (2)$$

To calculate the value of ω_{INJ} in this case, we should first note the expression of phase shift θ introduced by the LC tank, which is given in Ref. [5] as

$$\tan\theta \approx \frac{2Q}{\omega_0}(\omega_0 - \omega_{INJ}), \quad (3)$$

where Q is the quality factor of the LC tank. Combining Eqs. (2) and (3), we can obtain the locking range as

$$2|\Delta\omega| = \frac{\omega_0}{Q}\frac{1}{\sqrt{(I_M/I_{INJ})^2 - 1}}. \quad (4)$$

Therefore, equation (4) reveals critical insights for the design of an ILFD: either increasing the injection current I_{INJ} or reducing the quality factor of the LC tank can effectively enhance the locking range of the ILFD.

2.3. Divide-by-two ILFD

Injection locking can be used for frequency division when the signal is injected into the harmonic node of an oscillator. Figure 5 shows a conventional ILFD, where the signal is injected into the second harmonic node of the oscillator through a tail transistor. With proper amplitude and frequency,

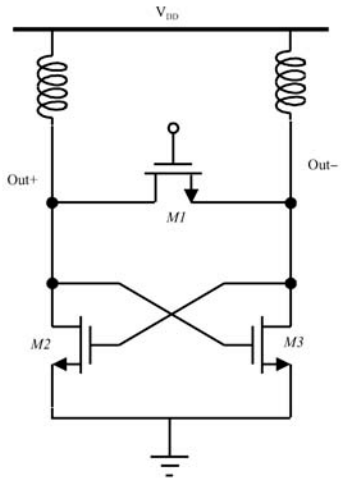

Fig. 6. Direct-injection divide-by-two ILFD.

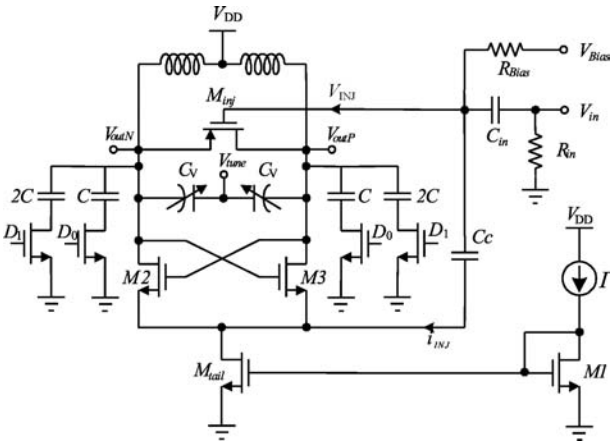

Fig. 7. Schematic of the proposed ILFD.

the input signal can lock the resonate frequency at exactly one-half of its own frequency. The 3-GHz 1.2-mW CMOS divide-by-two ILFD was reported with a 370-MHz locking range in Ref. [6].

Such a small locking range is obviously a drawback for an ILFD, and several techniques were proposed to enhance its locking range. Among them, the direct injection technique is the most promising and widely adopted one, as shown in Fig. 6[7]. Since the output signals are locked directly by the input signal through the switch M1, the signal injection efficiency is significantly enhanced. The 15-GHz 23-mW CMOS ILFD using direct injection achieves a locking range of 3 GHz. This paper presents a wide-locking-range ILFD using a novel dual-injection technique together with DCCA tuning, for which the measured locking range is 4.85 GHz from 6.23 to 11.08 GHz. Using a 1.8-V power supply, the proposed ILFD consumes only 3.7 mA of current.

3. Circuit design

Figure 7 shows the schematic of the proposed ILFD. The oscillator core consists of a cross-coupled transistor pair M2-M3 to provide the negative impedance needed for sustained oscillation. A center-tapped spiral inductor was realized in metal layer 6 to resonate with the tank capacitances. The simulated

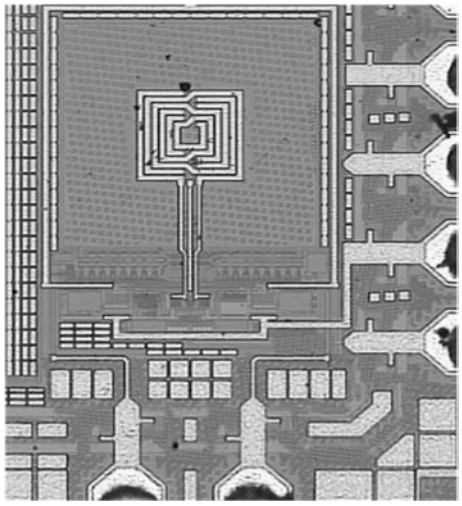

Fig. 8. Chip photograph of the ILFD.

values for the inductance and Q_L at 5 GHz are 0.9 nH and 10, respectively. The value we chose for the inductor was relatively small since Q_L should be decreased to achieve a wider locking range according to Eq. (3). However, such a degradation of Q_L entails higher tank losses which lead to an increase of power consumption. Therefore, a trade-off has to be made between locking range and power consumption at this design stage.

The free-running frequency of the oscillator is tuned in our design by both varactors and DCCA to obtain a wide tuning range. Two varactors connected back-to-back in the tank are formed by the accumulation MOS (A-MOS) varactor and are controlled by the tuning voltage V_{tune}. In addition, 2 bits digital control signals (D0, D1) are employed to switch the fixed capacitor array with unit value of 216 fF, which largely extends the tuning range of the oscillator. The free-running frequency of the oscillator is designed at one-half of the targeted input center frequency of the ILFD, which is around 4.3 GHz.

To further extend the locking range of the ILFD, the dual-injection technique was used in the proposed circuit topology. As shown in Fig. 7, two injection paths were formed at the input: one is injected through the switch connecting the differential outputs and the other is injected into the oscillator's second harmonic node through a coupling capacitor C_C. The additional current from the latter path can contribute a lot to the total injection current, which directly enhances the locking range based on Eq. (4).

4. Implementation and measurements

The ILFD was designed and fabricated in the Jazz 0.18-μm RF 1P6M CMOS process. The photograph of the chip is shown in Fig. 8. The circuit occupies an area of 0.38 × 0.28 mm^2 (without pads), and draws a static current of 3.7 mA from the supply voltage of 1.8 V.

The performance of the designed ILFD was measured with an Agilent E8257D PSG 20-GHz analog signal generator, an E4440A PSA 26-GHz spectrum analyzer and an Infiniium DSO90000A oscilloscope. The measured sensitivity curve of the frequency divider is plotted in Fig. 9. The solid line and the dotted line are measured for a V_{tune} of 1.8 V and 0 V, respec-

Table 1. Performance comparison of the proposed ILFD with other ILFDs previously reported in the literature.

	Technology	P_{in} (dBm)	V_{DD} (V)	$P_{diss.}$ (mW)	Area (mm^2)	Locking range (GHz)	Phase noise @ 1 MHz offset (dBc/Hz)
Ref. [7]	0.18 μm CMOS	7	1.5	23	0.49 × 0.47	14.2–17.2	NA
Ref. [8]	0.18 μm CMOS	0	1.8	13.8	NA	1.2–7.4	−130
Ref. [9]	0.35 μm CMOS	10	1.5	15.15	0.76 × 0.78	4.56–5.59	–128
Ref. [10]	0.18 μm CMOS	10	1.8	2.84	NA	4–8.2	NA
Ref. [11]	90 nm CMOS	5	1.2	6.4	0.33 × 0.08	19.5–22.0	−126.6
Ref. [12]	0.18 μm CMOS	5	1.8	38	0.50 × 0.53	18.8–23.2	−134.8
This work	0.18 μm CMOS	8	1.8	6.6	0.38 × 0.28	6.5–11.08	−137.9

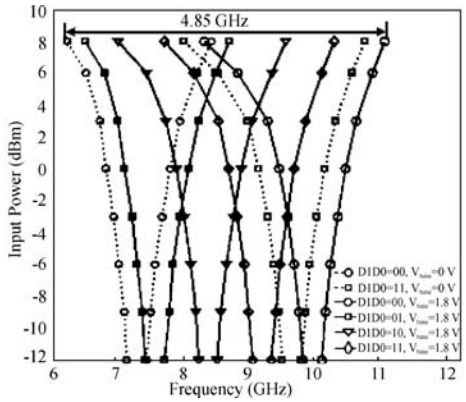

Fig. 9. Measured sensitivity curve of the ILFD.

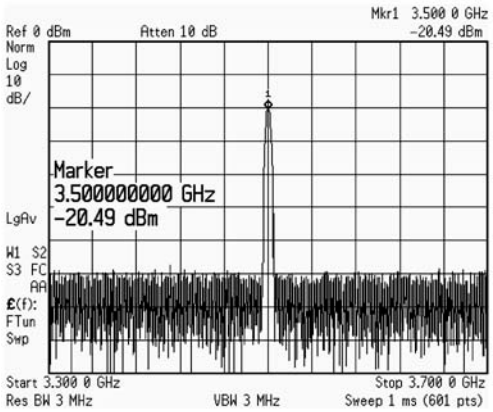

Fig. 10. Output spectrum at 7 GHz input.

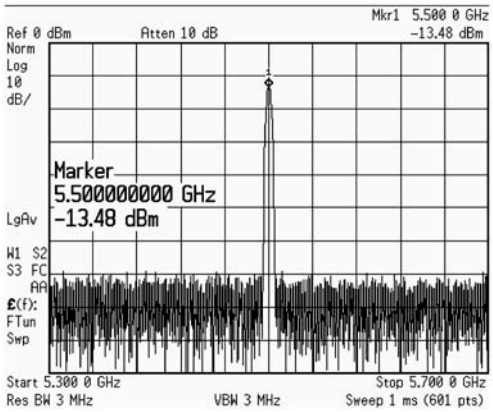

Fig. 11. Output spectrum at 11 GHz input.

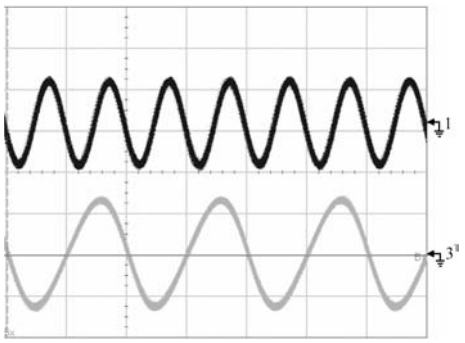

Fig. 12. Transient waveforms of input and output signals.

tively, with the control signals changing in incremental steps from D1D0 = 00 to D1D0 = 11. The entire locking range was measured at 4.85 GHz (from 6.23 to 11.08 GHz) with an input power of 8 dBm. Figures 10 and 11 show the measured output spectra for input signal frequencies of 7 and 11 GHz, respectively. It is noted that the output power at 3.5 GHz is much lower than that at 5.5 GHz, because the decrease of the oscillation frequency will reduce the equivalent resistance. The transient waveforms of a 10 GHz input and a 5 GHz output signals are plotted in Fig. 12.

Figure 13 shows the measured phase noise performances of the proposed ILFD. The phase noise of the free-running oscillator at 1 MHz offset is about −107.3 dBc/Hz. After external signal injection, the phase noise of the ILFD is about −137.9 dBc/Hz, while the input signal from the signal generator is 8 GHz with a phase noise of −132 dBc/Hz. The phase noise of the locked ILFD is lower than that of the free-running oscillator by 30 dB at an offset frequency of 1 MHz. Compared with its injection source, the ILFD shows a 6 dB improvement at low offset frequency. This has been verified by different carrier frequencies from 7 to 11 GHz. A 6 dB phase noise reduction has been found, as shown in Fig. 13. This is in good agreement with theoretical predictions for an ideal divide-by-two frequency divider. Figure 14 intuitively compares the phase noise performance between a free-running and an injection-locked divider for an injection signal of 10 GHz from a spectrum perspective.

Table 1 presents the performance comparison between the proposed ILFD and several recently published ILFDs.

5. Conclusion

This paper presents the design and implementation of an ILFD in a 0.18 μm RF CMOS process. At a supply voltage of 1.8 V, the power consumption of the proposed ILFD is only 6.6 mW. With the assistance of tuning methods and injection efficiency enhancement, the proposed ILFD achieves a locking range of 4.85 GHz from 6.23 to 11.08 GHz at an input

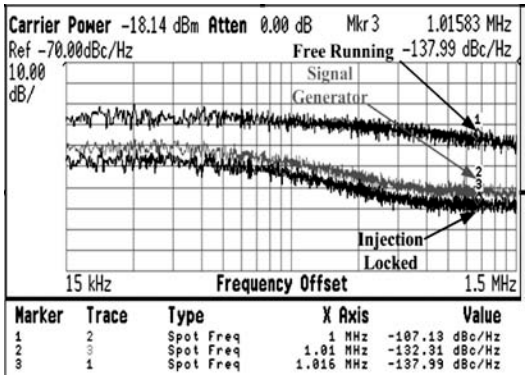

Fig. 13. Measured phase noise of the ILFD.

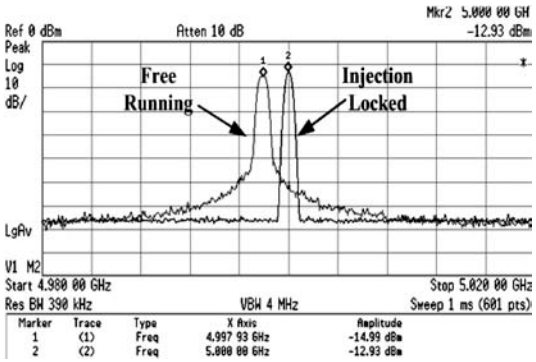

Fig. 14. Comparison of the output spectra for a free-running and an injection-locked divider.

power of 8 dBm. Such a wide locking range together with the low power consumption makes it possible for the ILFD to be applied in frequency synthesizers for the high group bands of UWB systems.

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