A 16-bit cascaded sigma–delta pipeline A/D converter

Li Liang(李梁), Li Ruzhang(李儒章)†, Yu Zhou(俞宙), Zhang Jiabin(张加斌), and Zhang Jun'an(张俊安)

(National Key Laboratory of Analog ICs, The 24th Institute, China Electronics Technology Group Corporation, Chongqing 400060, China)

Abstract: A low-noise cascaded multi-bit sigma-delta pipeline analog-to-digital converter (ADC) with a low oversampling rate is presented. The architecture is composed of a 2-order 5-bit sigma–delta modulator and a cascaded 4-stage 12-bit pipelined ADC, and operates at a low 8X oversampling rate. The static and dynamic performances of the whole ADC can be improved by using dynamic element matching technique. The ADC operates at a 4 MHz clock rate and dissipates 300 mW at a 5 V/3 V analog/digital power supply. It is developed in a 0.35 μm CMOS process and achieves an SNR of 82 dB.

Key words: multi-bit sigma–delta ADC; oversampling; pipeline; digital filter; switched capacitor
DOI: 10.1088/1674-4926/30/5/055010 **EEACC:** 1265H; 2570D

1. Introduction

Today, one of the most important trends in very large scale integration (VLSI) systems is the shift from signal processing in the analog domain to signal processing in the digital domain. Consequently, the ADC performance requirements become more stringent for both dynamic range and bandwidth. The wideband digital radio receiver is an example of a system that must simultaneously digitize strong and weak signals. Such systems need excellent SNR to avoid losing the weak signal in the quantization or thermal noise.

A sigma–delta ADC is based on two key principles to provide high data conversion accuracy: oversampling and noise shaping. It is quite common to use an oversampling rate (OSR) higher than 32 to achieve over 16-bit accuracy for analog-to-digital conversion[1, 2]. However, a high OSR leads to a low Nyquist data rate. Multi-bit sigma–delta modulators help to achieve high accuracy with moderate OSR (between 16 and 32), but precaution has to be taken to minimize the distortion and extra noise introduced by the mismatch of the feedback DAC element.

The feature of pipelined ADCs, on the other hand, is to obtain a high conversion speed with moderate high accuracy at the cost of a few clock cycles latency. The achievable accuracy of the pipelined ADC is limited by the matching of the capacitors inside the sub-blocks, such as the MDAC. When 14-bit accuracy is required, trimming or some kind of calibration is required, which tends to lower the speed of the overall ADC and increases the power consumption and complexity as well[3–5].

The proposed architecture operated with low OSR and high signal bandwidth, which combines a multi-bit sigma–delta modulator with a 12-bit pipelined converter, is described in this paper. Circuit implementation details for the cascaded sigma–delta pipeline ADC are discussed, including the 16-bit linear multi-bit D/A converters in the modulator, the 12-bit pipeline ADC, and the on-chip digital half-band FIR (finite impulse response) decimation filters. Noise limitations and measured performance of the integrated ADC are also reported.

2. Architecture design

Figure 1 shows the block diagram of a conventional multi-bit sigma–delta ADC providing high SNR for this 16-bit accuracy application. The digital output of the modulator Mout(z) is given by

$$\mathrm{Mout}(z) = G(z)V_{\mathrm{in}}(z) + H(z)Q_{\mathrm{M}}(z), \tag{1}$$

$$G(z) = F(z)/[1 + F(z)], \tag{2}$$

$$H(z) = 1/[1 + F(z)], \tag{3}$$

where $V_{\mathrm{in}}(z)$ is the ADC input signal, $G(z)$ is the signal transfer function (STF) of the modulator loop, $H(z)$ is the error or 'noise' transfer function (NTF) of the modulator loop, and $Q_{\mathrm{M}}(z)$ is the quantization error of the m-bit flash ADC[6].

In this application, the OSR is quite low (OSR = 8) and the required accuracy is quite high (16-bit). Therefore, a multi-bit quantizer must be employed. Although a higher order modulator ($N \geqslant 2$) tends to give higher SNR, the improvement at this low OSR is marginal. For example, if a classical NTF in the form of

$$H(z) = (1 - z^{-1})^N \tag{4}$$

is chosen, the improvement of the SNR with each increment in loop order N is 15 dB and 9 dB for OSRs of 16 and 8, respectively. If a 2-order modulator is chosen, the quantizer resolution has to be larger than 8 to ensure an SNR larger than 84 dB.

Since the quantizer in Fig. 1 is part of a feedback loop, it must quickly quantize the signal. Any delays in the modulator loop must be small enough to avoid destabilizing the

† Corresponding author. Email: lrzmail@163.com
Received 16 October 2008, revised manuscript received 11 November 2008

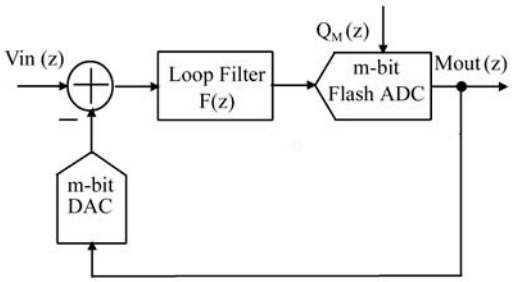

Fig. 1. Conventional multi-bit sigma–delta ADC.

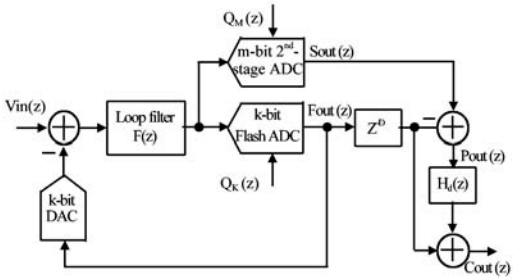

Fig. 2. Cascaded multi-bit sigma-delta ADC.

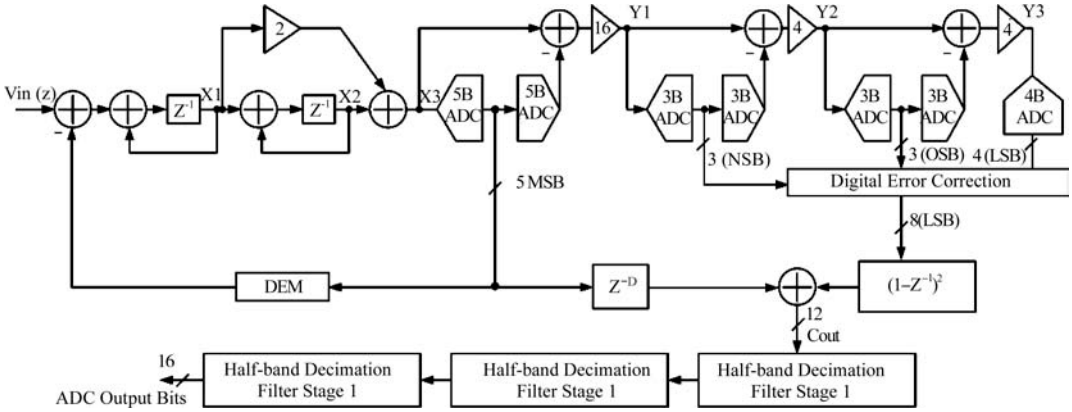

Fig. 3. The proposed cascaded multi-bit sigma-delta pipeline ADC.

loop. A flash ADC provides a small delay and is a good choice for the quantizer implementation. Unfortunately, the flash architecture is not well suited for high-resolution quantization, because the area and power consumption doubles for each additional bit of resolution. Consequently, the option of implementing a flash ADC into a conventional modulator with high resolution feedback is not promising.

Figure 2 shows the block diagram of a cascaded multi-bit sigma–delta ADC architecture, which may be implemented with an efficient high-resolution quantizer. In this architecture, a first-stage k-bit analog sigma–delta modulator is cascaded with a second-stage m-bit high resolution ADC ($m > k$). The first-stage modulator includes a loop filter, a k-bit flash ADC, and a k-bit feedback DAC. The second-stage ADC provides m-bit quantized digital output data at the same rate as the flash ADC conversion rate. A key feature of the structure is that the m-bit ADC is not within the modulator loop, and so its latency will not affect the stability of the modulator loop. Examples of ADC architectures that are good candidates for the second-stage ADC includes pipelined architectures[3–5] and parallel time-interleaved architectures[7, 8]. Both provide relatively high resolution at economical cost and a fast conversion rate. The relationships between them are as follows:

$$\mathrm{Fout}(z) = G(z)V_{\mathrm{in}}(z) + H(z)Q_{\mathrm{K}}(z), \tag{5}$$

$$\mathrm{Pout}(z) = \mathrm{Sout}(z) - Z^{-D}\mathrm{Fout}(z) = Q_{\mathrm{M}}(z) - Z^{-D}Q_{\mathrm{K}}(z), \tag{6}$$

$$\begin{aligned}\mathrm{Cout}(z) &= Z^{-D}\mathrm{Fout}(z) + H_{\mathrm{d}}(z)\mathrm{Pout}(z)\\ &= Z^{-D}G(z)V_{\mathrm{in}}(z) + Z^{-D}[H(z) - H_{\mathrm{d}}(z)]Q_{\mathrm{K}}(z) + H_{\mathrm{d}}(z)Q_{\mathrm{M}}(z),\end{aligned} \tag{7}$$

where the definitions of $V_{\mathrm{in}}(z)$, $G(z)$ and $H(z)$ are the same as in Eqs. (1)–(3). $Q_{\mathrm{K}}(z)$ and $Q_{\mathrm{M}}(z)$ are the quantized noise for the k-bit flash ADC and the m-bit pipeline ADC, respectively. Z^{-D} is the latency of the pipeline ADC, and D is the delay measured in number of clock cycles. $Q_{\mathrm{M}}(z)$ is much smaller than $Q_{\mathrm{K}}(z)$. If $H_{\mathrm{d}}(z)$ is equal to the NTF of modulator $H(z)$, then $Q_{\mathrm{K}}(z)$, as a greater term in the quantized noise, will be eliminated, and so

$$\mathrm{Cout}(z) = Z^{-D}G(z)V_{\mathrm{in}}(z) + H_{\mathrm{d}}(z)Q_{\mathrm{M}}(z). \tag{8}$$

Although the input is delayed by Z^{-D}, the noise feature is the same as that of the m-bit high-resolution modulator loop. Obviously, the structure in Fig. 2 is more suitable than that in Fig. 1. Furthermore, since the number of quantized bits in the modulator loop is reduced, the requirements for capacitance matching in the feedback DAC will decrease and the noise figure will be more favorable[9].

3. Circuit design

The proposed detailed block diagram of the 16-bit ADC is drawn in Fig. 3. The ADC includes a 5-bit 2-order modulator loop cascaded with a 4-stage 12-bit pipelined ADC. A 5-3-3-4 pipeline architecture provides high accuracy at a 4 MHz conversion rate. The pipelined ADC is implemented with a conventional fully-differential multi-bit-per-stage switched capacitor design that has been well described in the literature[1, 2, 5]. This converter provides full 12-bit linearity without trim or calibration. The use of 12-bit in the pipeline insures that the ADC noise performance is not dominated by the pipeline error (Q_{M}), either while operating at 8X OSR or at 4X OSR.

The outputs of the last three stages of the pipelined converter are combined in the pipeline correction logic to form the 8 LSBs, which provide an approximation of the large quanti-

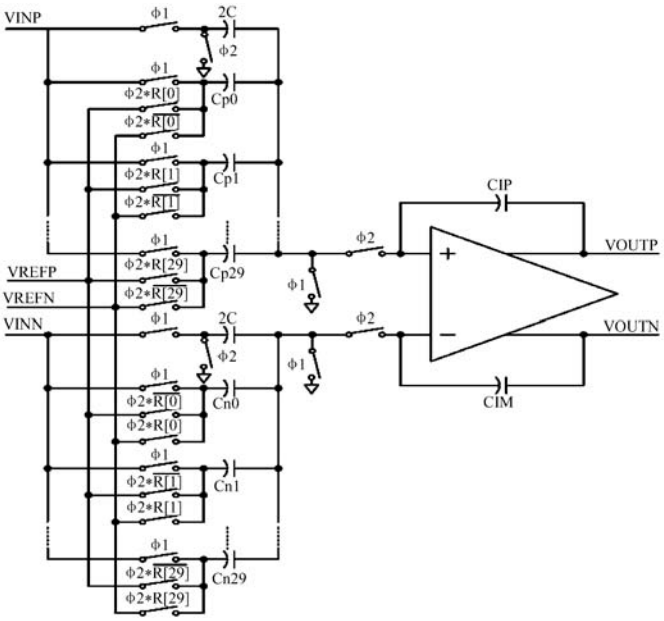

Fig. 4. Switched-capacitor DAC and integrator.

zation error (Q_K) of the 5-bit flash. The most significant bit of the 8 LSBs is aligned with the least significant bit of the 5-bit flash data during numerical processing of these two signals. Similarly, an extra bit of redundancy is also used in each of the 3-bit residue stages to facilitate digital correction of flash errors. The 2-order digital differentiation of the LSBs, provided in the LSB differentiator block, emulates the filtering of the flash quantization noise in the 2-order modulator loop. The differentiated LSBs are added to the time-delayed output of the modulator loop, resulting in a digital output Cout(z), which is equivalent to the output of a single 2-order modulator loop with 12-bit feedback. The digital hardware for the LSB differentiator and adder requires only four addition/subtraction operations of modest resolution. Half-band decimation filters are implemented in each of the 2X decimator blocks to provide filtering and 8X decimation of the output data.

Two significant simplifications are implemented in the block diagram in Fig. 3, as compared to the diagram in Fig. 2. First, the flash ADC in the modulator loop is shared by the pipelined ADC. This 5-bit flash ADC is used both as the quantizer in the modulator loop and the first stage of the 5-3-3-4 pipeline, providing a significant die area reduction of the integrated ADC. Second, the digital processing circuitry is simplified. The difference in the first 5-bit stage of the pipeline provides an analog representation of the 5-bit flash quantization error Q_K. The last three stages of the pipeline digitize this quantity. Thus, the need for the analogous differencing operation provided by the digital difference in Fig. 2 is eliminated.

3.1. 2-order multi-bit sigma-delta modulator

The loop filter of the 2-order modulator shown in Fig. 3 can be derived as

$$L(z) = [z^{-1}/(1-z^{-1})][2+z^{-1}/(1-z^{-1})] = (2z^{-1}-z^{-2})/(1-z^{-1})^2. \quad (9)$$

Thus, the noise transfer function (NTF) can be obtained as

$$H(z) = 1/(1 + L(z)) = (1 - z^{-1})^2. \quad (10)$$

Equation (10) is identical to the digital filter transfer function to be matched (i.e. $H_d(z)$ in Eq. (7)). Therefore, under ideal conditions, the quantization noise from the modulator quantizer Q_K should be canceled, while the quantization noise from the pipeline ADC Q_M will be suppressed by this 2-order high-pass transfer function, which results in superior in-band SNR.

The low frequency distortion of the multi-bit sigma–delta ADC is limited by element mismatch errors of the multi-bit D/A converter. The DEM (dynamic element matching) block in Fig. 3 achieves a 1-order mismatch shaping effect by averaging the usage of each unit element. It should be emphasized that careful layout is mandatory to minimize the capacitor mismatch error in the feedback DAC. Double-poly capacitors should be chosen to reduce the parasitic bottom plate capacitance. Dummy capacitors should be placed around the capacitor array for better matching.

The fully-differential switched-capacitor structure shown in Fig. 4 implements the combination of DAC and first integrator functions. Each conversion period is divided into two non-overlapping clock phases. In phase phi1, all of the switches in the input switch array are switched on, connecting the bottom plates of all the DAC capacitors to the input signals, V_{INP} and V_{INN}. The top plates are connected to ground during phi1 and a charge proportional to the input signal is established on the DAC capacitor array. In phase phi2, the bottom plates of the capacitor elements in the DAC array are individually reconnected either to the positive reference voltage V_{REFP} or the negative reference voltage V_{REFN} using switches in the reference switch array. The top plates are simultaneously connected to the input terminals of amplifier A0, causing a transfer of charge from the DAC capacitors onto the integrating capacitors. The reference switches in Fig. 4 are controlled with 30 signals, R0 through R29. These control signals are generated by the DEM, which scrambles the 30 thermometer-code levels from the 5-b flash ADC to control the capacitor element selection in the DAC. For a flash thermometer code of $j (0 \leqslant j \leqslant 29)$, j capacitors in the upper DAC array are connected to V_{REFP} and 30-j capacitors are connected to V_{REFM}. The control signals to the reference switches in the lower array in Fig. 4 are inverted from those in the upper array to provide a corresponding equal and opposite control signal in the lower half of the differential circuit. The resulting charge transfer onto the integrating capacitors is proportional to the difference between the input signal and an analog representation of the flash thermometer code signal. The 5-bit flash ADC has 30 threshold values R [29:0], and thus a total of 31 thermometer codes. Compared with traditional full 5-bit quantizer, $2^5 - 2$ comparators are used, instead of $2^5 - 1$ comparators. This allows an errors of up to +/− 1/16 V_{REF} in the flash ADC threshold value since they can be corrected later on by digital error correction logic. A fully-differential comparator array structure will be used for maximum noise immunity.

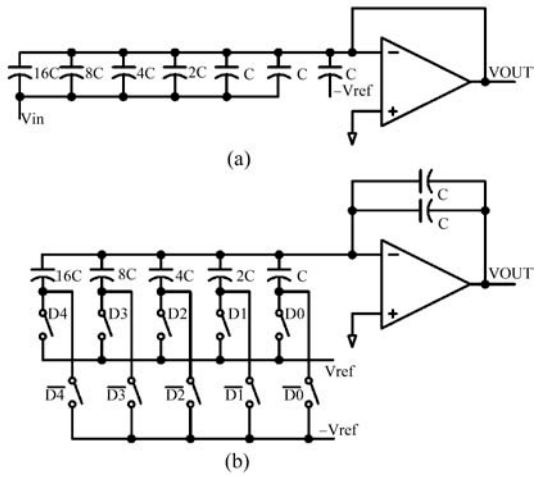

Fig. 5. MDAC-1 for pipeline ADC: (a) Sampling phase; (b) Multiplication phase.

3.2. 12-bit pipeline ADC

The pipeline ADC needs to provide 12-bit resolution, so that its quantization noise can be small enough to achieve 16-bit accuracy after being noise-shaped by a 2-order transfer function. As shown in Fig. 3, a 5-3-3-4 multi-stage architecture will be chosen. Part of the first 5-bit stage will be combined with the modulator. The 5-bit sub-DAC and multiplication by 16 will be combined together and implemented as a fully-differential switched-capacitor MDAC circuitry[10].

Figure 5 shows the proposed MDAC. Two-phase clocking will be used. During phi1, the MDAC enters into the sampling phase, where all the input capacitors sample the input voltage. The amplifier has its input/output shorted in this phase. Thus, any offset error from the amplifier will be stored across the input capacitors as well. This is usually called 'auto-zero' function. In phase phi2, the bottom plates of the input capacitors (C, $2C$, $4C$, $8C$ and $16C$) will be switched to either $V_{\rm refp}$ or $V_{\rm refn}$, depending on the decision made by the sub-ADC D_i, (i = 0–4). If D_i = '1', then the bottom plate of the corresponding capacitor will be tied to $V_{\rm refp}$, otherwise it will be tied to $V_{\rm refn}$. In this way, at the end of phi2, the difference between the current input voltage $V_{\rm in}$ and the feedback DAC voltage will be generated according to the following equation:

$$V_{\rm o} = 16V_{\rm in} - \sum D_i 2^i V_{\rm ref} - 0.5V_{\rm ref},\ \ i = 0, 1, 2, 3, 4. \quad (11)$$

The output voltage will feed as the input into the next stage of the pipeline, while the digitized value D_i (i = 0–4) appears as the first stage 5-bit output.

3.3. On-chip FIR decimation filters

The cascaded pipeline plus sigma-delta modulator ADC generates 12-bit output data clocked at $f_{\rm s}$ = 4 MHz. To get 16-bit final output, three stages of half-band filters are required. Each half-band filter will reduce the input data rate by a factor of 2 while increasing the bit-word length gradually from 12-bit to 16-bit. The first half-band filter is a 23-order FIR filter operating at $f_{\rm s}/2$. Due to the special property of the half-band filter, the other filter coefficients are all zero. Thus, there are only 13 non-zero filter coefficients needed. The implementation of the filter can be further simplified due to the symmetry inherent to FIR filters, that is:

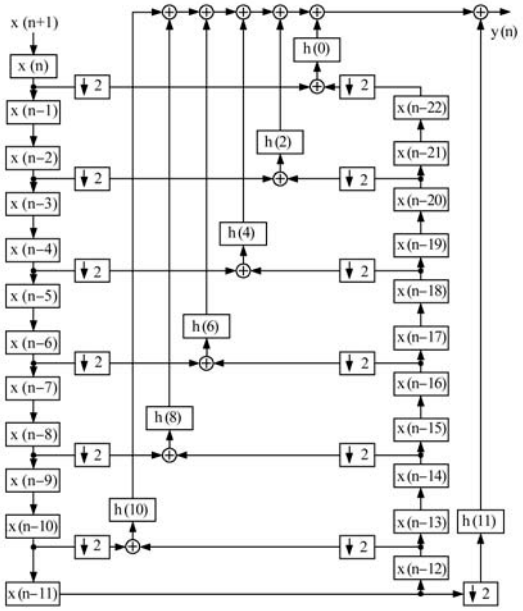

Fig. 6. First-stage half-band FIR filter.

$$H(n) = H(M - n), \ \ \text{where} \ \ M = 22, n = 0, 2, 4, \ldots \quad (12)$$

The element circuits of digital filters, in fact, refer to flip-flops, adders, and multipliers. To save area and power dissipation, the coefficients are fixed in the circuit, and the multiplier is replaced by a shift-adder. As a result, the circuit speed is increased and the scales for the circuit and layout are reduced. In general, if a binary bit corresponding to a filter coefficient is zero, one adder can be saved. The diagram of the whole 1st stage half-band FIR digital filter (HBF1) is shown in Fig. 6. The configuration of the following two stages are similar to the first one.

4. Noise limitations

Four important noise sources contribute to the overall noise performance of this ADC: 12-bit pipeline quantization noise ($Q_{\rm M}$), 5-bit flash ADC quantization noise leakage (H–$H_{\rm d}$)$Q_{\rm K}$, noise energy of capacitor mismatch errors in the modulator feedback DAC, and device thermal noise. The use of 12-bit in the pipeline stage and 5-bit feedback in the modulator loop ensures that the ADC is not limited by quantization noise, either from the pipeline ($Q_{\rm M}$) or from leakage of flash quantization errors ((H–$H_{\rm d}$)$Q_{\rm K}$) in the modulator loop. With 8X oversampling, the theoretical inband rms energy of the 12-b pipeline quantization noise ($Q_{\rm M}$) is 106 dB below that of a full-scale sine wave.

Behavioral simulation illustrates the effect of analog transfer function errors (i.e. $H \neq H_{\rm d}$) on the ADC noise performance. A gain error is modeled in the first integrator INT1 in these simulations. With 8X oversampling and a 0.5% gain error of INT1, the total in-band rms quantization noise energy

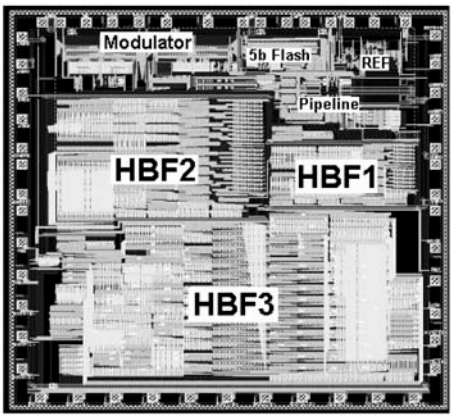

Fig. 7. The proposed 16-bit ADC chip layout.

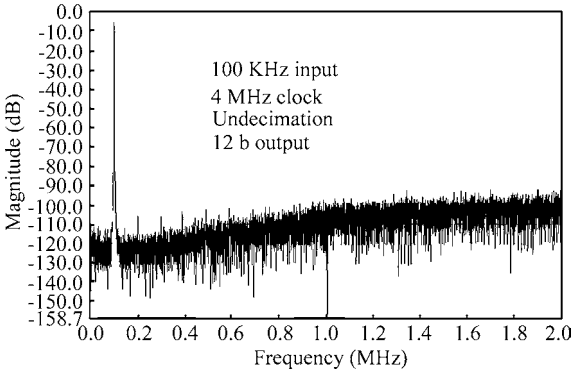

Fig. 8. Undecimated 12-b output.

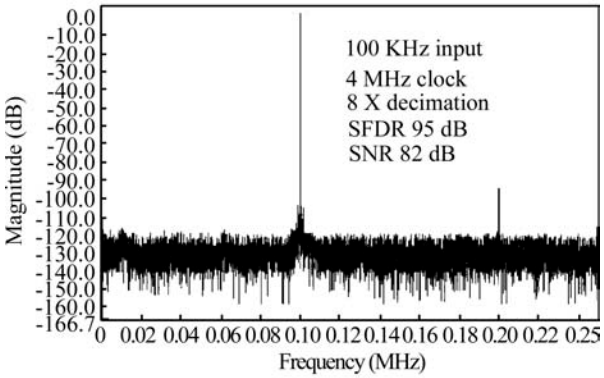

Fig. 9. 8X decimated 16-b output of the whole ADC.

Table 1. Comparision of performances.

Parameter	Ref. [1]	Ref. [2]	This work
Resolution (bit)	16	16	16
Data rate (kHz)	50	320	500
OSR (X)	256	64	8
DNL (LSB)	/	/	±1
INL (LSB)	/	/	±1.5
SNR (dB)	94	93	82
SFDR (dB)	98	96	95
THD (dB)	/	/	–92
Supply (V)	5	5	5/3
Die size (mm^2)	0.39	1.6	5

remains 95 dB below that of a full-scale sine wave. Also, a standard deviation mismatch of 0.1% is assumed to apply for the feedback DAC capacitors. The behavioral simulation indicates that the noise contribution from capacitor mismatch errors will remain at a level of less than –96 dB with respect to the full-scale signal.

5. Measurement results

The ADC has been realized in a 0.35 μm double-poly, treble-metal CMOS process. Figure 7 shows the layout of the chip. Full-custom analog and digital layout is adopted. Approximately 65% of the die area is dedicated to the implementation of digital circuitry, which includes the processing circuitry for the modulator and pipeline data, the three half-band decimation filters, and the control/test logic. The 5-bit flash ADC is centered between the modulator and the pipeline for convenience of sharing the functions of these two circuits.

The result is measured with a 100 kHz input signal and with a test mode enabled to allow the data to be captured directly from the output of the ADC, bypassing the three half-band decimation filters. Figure 8 shows the spectrum of the output of the ADC after the modulator and pipeline data have been digitally processed and combined. This spectrum clearly shows the reduction in quantization noise achieved with the cascaded sigma–delta pipeline architecture. The noise spectral density in Fig. 8 is equivalent to that of a 2-order 12-bit modulator loop (Q_M). Figure 9 shows the spectrum measured with 8X decimation of the ADC output data. With 8X oversampling, the noise performance of the ADC is limited by device noise primarily.

The measurement results are summarized in Table 1. Compared to previously published sigma–delta A/D converters[1, 2, 11, 12], the hybrid architecture provides excellent SFDR, linearity and dynamic range with low OSR and high output data rate.

6. Conclusion

A cascaded sigma–delta pipeline A/D converter achieves an 82 dB SNR and 95 dB SFDR is presented. The ADC architecture combines sigma–delta techniques with traditional high-speed Nyquist-rate A/D conversion techniques to simultaneously achieve wide bandwidth and wide dynamic range. The device operates at a 4 MHz sample rate and at a low 8X oversampling rate. The chip is integrated in a 0.35 μm double-poly, treble-metal CMOS process. Static power consumption is only 300 mW with a single 5 V analog supply and a single 3 V digital supply.

References

[1] Brandt B P, Wingard D E, Wooley B A. Second-order sigma-delta modulation for digital-audio signal acquisition. IEEE J Solid-State Circuits, 1991, 26(4): 618

[2] Yin G, Stubble F, Sansen W. A 16-b 320-kHz CMOS A/D converter using two-stage third-order $\sum\Delta$ noise shaping. IEEE J Solid-State Circuits, 1993, 28(6): 640

[3] Siragusa E, Galton I. A digitally enhanced 1.8-V 15bit 40-MS/s CMOS pipelined ADC. IEEE J Solid-State Circuits, 2004, 39(12): 2126

[4] Yun C, Gray P R, Nikolic B. A 14-b 12-MS/s CMOS pipeline ADC with over 100-dB SFDR. IEEE J Solid-State Circuits, 2004, 39(12): 2139

[5] Nair K, Harjani R. A 96 dB SFDR 50 MS/s digitally enhanced CMOS pipeline A/D converter. ISSCC, 2004: 456

[6] Norsworthy S R, Schreier R, Temes G C. Delta–sigma data converters: theory, design, and simulation. IEEE Press, 1997

[7] Limotyrakis S, Kulchycki S D, Su D, et al. A 150 MS/s 8b 71 mW time-interleaved ADC in 0.18 μm CMOS. ISSCC, 2004: 258

[8] Draxelmayr D. A 6b 600 MHz 10 mW ADC array in digital 90 nm CMOS. ISSCC, 2004: 264

[9] Bosi A, Panigada A, Cesura G. An 80 MHz 4x oversampled cascaded $\sum\Delta$-pipelined ADC with 75 dB DR and 87 dB SFDR. ISSCC, 2005:174

[10] Razavi B. Design of analog CMOS integrated circuits. New York: McGraw-Hill, 2001

[11] Boser B E, Wooley B A. The design of sigma-delta modulation analog-to-digital converters. IEEE J Solid-State Circuits, 1988, 23(6): 1298

[12] Matsuya Y, Uchimura K, Iwata A, et al. A 16-bit oversampling A-to-D conversion technology using triple-integration noise shaping. IEEE J Solid-State Circuits, 1987, 22(6): 921