The Bipolar Field-Effect Transistor: VI. The CMOS Voltage Inverter Circuit (Two-MOS-Gates on Pure-Base)*

Jie Binbin[1,†] and Sah Chih-Tang[1,2,3,†]

(1 *Peking University*, *Beijing* 100871, *China*)
(2 *University of Florida*, *Gainesville*, *Florida* 32605, *USA*)
(3 *Chinese Academy of Sciences*, *Foreign Member*, *Beijing* 100864, *China*)

Abstract: This paper reports the DC steady-state voltage and current transfer characteristics and power dissipation of the Complimentary Metal-Oxide-Silicon (CMOS) voltage-inverter circuit using one physical Bipolar Field-Effect Transistor (BiFET) of nanometer dimensions. The electrical characteristics are numerically obtained by solving the five partial differential equations for the transistor structure of two MOS-gates on the two surfaces of a thin pure silicon base layer with electron and hole contacts on both ends of the thin base. Internal and CMOS boundary conditions are used on the three potentials (electrostatic and electron and hole electrochemical potentials). Families of curves are rapidly computed using a dual-processor personal computer running the 64-bit FORTRAN on the Windows XP operating system.

Key words: bipolar field-effect transistor theory; surface channel; volume channel; CMOS inverter; CMOS-BiFET
PACC: 7340Q **EEACC**: 2560S; 2560B
CLC number: TN386.1 **Document code**: A **Article ID**: 0253-4177(2008)11-2079-09

1 Introduction

Field-effect transistor (FET) was the intended name coined by Shockley and Pearson in their unsuccessful experiment 60 years ago in 1948 to obtain conductivity modulation of a silicon film by the application of a perpendicular electric field[1]. Conductivity modulation was used first by Lilienfeld 80 years ago in his field-effect transistor patents filed in 1926 and 1928[1]. Only one charge carrier type, the electrons, was considered. Also, only one region, the volume of the semiconductor, was considered. Lilienfeld did not know surface channel and electronic states on the surface. Shockley and Pearson failed because of them. In addition, only drift current was considered. These two earlier restrictions or limitations (one carrier type and one conduction region, the volume) were continued by Shockley 55 years ago in 1952 in his invention of the volume-channel field-effect transistor using p/n junction gates to change the width of the volume channel and hence the conductance modulation of the volume channel, rather than conductivity modulation of the surface channel from changing the carrier concentration in the surface channel[1]. Shockley also stated explicitly, in the title of his 1952 invention paper, that it is unipolar, i.e. only the electrons or the holes are changed to give the modulation of conductance of the volume channel. Nevertheless, technology advances had enabled the manufacturing of electrical circuits using field-effect transistors with the MOS gate to control the conductivity of silicon surface, but still only either the electron or the hole channel on the surface under the gate oxide[1]. It was then reported in 1963 by Wanlass, Sah and Moore[2,3] that a very desirable (low power dissipation) voltage inverter can be obtained by connecting an unipolar p-surface-inversion-channel MOS field-effect-transistor in series with an unipolar n-surface-inversion-channel MOS field-effect-transistor. It was recognized only 18 months ago in March 2007 from the experimental data of nanometer MOS field-effect transistors[4,5] that six current components can be simultaneously present in one physical field-effect transistor, which are: electron and hole channels, on the surface and volume of the semiconductor, and diffusion and drift. Electron-hole generation-recombination-trapping is not included but is another, solely bipolar, mechanism. Thus, field-effect transistors are inherently bipolar (BiFET), although some of the bipolar currents can be suppressed by proper device design, but not eliminated. It was immediately recognized by us[4,5], based on our previous experiences[6], that the bipolar nature

* This investigation and Jie Binbin have been supported by the CTSAH Associates (CTSA), founded by the late Linda Su-Nan Chang Sah, in memory of her 70th year.
† Corresponding author. Email: bb_jie@msn.com and tom_sah@msn.com
Received 23 October 2008, revised manuscript received 28 October 2008

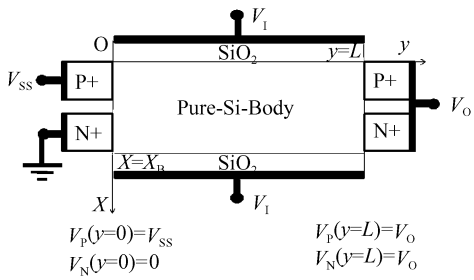

Fig. 1 The configuration of a BiFET with two MOS gates and a pure base under the CMOS voltage inverter circuit operation.

can be used to advantage for realizing of a circuit function in just one BiFET[4,5] such as the CMOS voltage inverter and the SRAM memory, which could give a factor of two jump of the Moore's law with existing technology. In this paper, we report for the first time, the calculated CMOS voltage inverter characteristics from one physical MOS BiFET, that were described earlier[4,5].

2 CMOS Voltage Inverter Circuit Bias Configuration and Theory

Figure 1 shows the cross-sectional view of a nanometer metal-oxide-silicon field-effect-transistor (MOSFET) with two identical MOS gates on a pure silicon base to illustrate the DC bias configuration for the voltage inverter circuit operation using one physical 2-MOS-gates Bipolar Field Effect transistor (BiFET). The physical realization of the voltage inverter function using two physical 1-MOS-gate Unipolar Field-Effect transistors (UniFET) had been reported by Wanlass, Moore and Sah some 45 years ago in 1963[1~3]. The two transistors of 1-MOS-gate had the two opposite base conductivity types and gate-voltage-induced surface inversion channels, the n-channel or electron-channel on the p-base and the p-channel or hole channel on the n-base. They coined this 2-transistor circuit in 1962 as the Complimentary Metal-Oxide-Silicon (CMOS) voltage inverter circuit. It was recently taught, in 1991, to college sophomore students as one of the two Basic Building Block (BBB) circuit[7].

For this new 1-transistor BiFET CMOS voltage inverter, the contacts to the two ends of the pure-base layer, as schematically illustrated in Fig. 1, are the unique specialty of this first circuit realization of the CMOS voltage inverter by one 2-gate BiFET, namely, these contacts are the source and drain (or sink) of electrons and holes, such as the two electrically isolated semiconductor junctions, the p + Drain/pure-Base and n + D/pure-Base junctions for the two drain contacts and the p + Source/pure-Base and n + Source/pure-Base junctions for the two source contacts. For our numerical computations, these contacts are assumed to cover the entire width and thickness of the two ends of the base layer or base sheet so that both electron and hole surface and volume channels are simultaneously present and conducting, which give the maximum geometry current. Such topology generalization offers device designers ingenuities to localize the current-carrying channels, hence quiescent state currents and power dissipation, and also peak switching current. To avoid symbol conflict between pure-Si and p-type-Si, we shall use the term intrinsic-Si or i-Si to denote pure-Si. Thus, these contacts to the pure-base layer are the p + D/i-B and n + D/i-B junctions. We recognize that the term "intrinsic" covers much broader conditions than "pure", such as an impure and a defective silicon at a sufficiently high temperature that the intrinsic carrier concentration is much higher than the chemical impurity and physical defect concentrations, $n_i \gg |N_{DD} - N_{AA}|$ and $n_i \gg N_{TT}$[7].

For the CMOS voltage inverter, the two drain contacts, n + D/i-B and p + D/i-B, are tied together by a metallic short circuit such as the interconnect conductor metal, and this serves as the output terminal node, with the terminal voltage or output voltage designated by $V_{DB} \equiv V_{OB} \equiv V_O$ where B is the reference-node of the applied voltage. The DC power supply voltages, 0 and V_{SS}, are applied to the two electrically isolated source contacts, with a positive voltage $V_{SS} > 0$ applied to the p + S/i-B contact, $V_{p+SB} = V_{SS} > 0$, and a negative voltage or zero reference applied to the n + S/i-B contact, $V_{n+SB} = V_{BB} \leqslant 0$. In our analysis, we use the asymmetrical or positive supply voltage, thus, $V_{BB} = 0$. For balanced case, we would have $V_{BB} = -V_{SS}$. The two MOS gates are identical, i.e. with the same threshold voltage, and they are tied together to serve as the input terminal with the input voltage, $V_I \equiv V_{GB}$. This CMOS bias configuration gives the following boundary conditions of the quasi-Fermi potentials of the MOS BiFET. In the mathematical analysis and numerical computations, all the potential variables, both internal and at the terminals, are normalized to the thermal voltage, $k_B T/q$, i.e. $U_N = qV_N/k_B T$, $U_P = qV_P/k_B T$ and $U_{IR} = qV_{IR}/k_B T$, where I is electric potential represented by the intrinsic Fermi potential, R = Reference potential node, k_B = Boltzmann constant and T = lattice or thermal phonon temperature. Then, in the not-normalized forms, the boundary values are:

$$V_N(y=0) = V_{BB} = 0,\ V_P(y=0) = V_{SS} \quad (1)$$

$$V_N(y=L) = V_P(y=L) = V_{OUTPUT} \equiv V_O \quad (2)$$

The DC electrical characteristics are governed by three DC steady-state Shockley equations (Poisson and Electron and Hole Current Continuity Equations)

with no electron-hole-generation-recombination-trapping. Five simultaneous DC MOS transistor equations were derived from the three Shockley equations[8], with the previously justified assumptions on (i) the x-independence of the electron and hole electrochemical potentials, (ii) the constancy and near thermal equilibrium of the electron and hole mobilities and diffusivity, $D_n(x, y, z, t, V_N, V_P, V, T) \equiv D_n \equiv (k_B T/q)\mu_n$ for electrons and similarly for holes, and (iii) the omission of 2-dimential terms in the Poisson equation. These five equations are (Integration $U = U_S$ to U_0):

The Voltage Equation:

$$U_{GS} - U_S = \text{sign}(U_S - U_0) \times (C_D/C_O) \times [\exp(U_S - U_N) - \exp(U_0 - U_N) + \exp(U_P - U_S) - \exp(U_P - U_0)]^{1/2} \quad (3)$$

The Thickness Equation:

$$X_B = 2\int \text{sign}(U - U_0)\partial_X U \div [\exp(U - U_N) - \exp(U_0 - U_N) + \exp(U_P - U) - \exp(U_P - U_0)]^{1/2} \quad (4)$$

The Total Current Equation:

$$I_N = + qD_n n_i L_D (W/L)(\partial U_N/\partial Y)\exp(-U_N)\int \exp(+U)\partial_X U \div [\exp(U - U_N) - \exp(U_0 - U_N) + \exp(U_P - U) - \exp(U_P - U_0)]^{1/2} \quad (5)$$

$$I_P = + qD_p n_i L_D (W/L)(\partial U_P/\partial Y)\exp(+U_P)\int \exp(-U)\partial_X U \div [\exp(U - U_N) - \exp(U_0 - U_N) + \exp(U_P - U) - \exp(U_P - U_0)]^{1/2} \quad (6)$$

The CMOS Circuit Transistor Total Internal Current Conservation-Continuity Equation (excluding loading)

$$I_{CH} = I_N = -I_P \quad (7)$$

The notations here are defined in [8] except that I_{CH} is the channel current of the BiFET connected as the CMOS voltage inverter. The boundary or terminal values are: $U_{n+SR} = U_{BR} = 0$, $U_{GR} = U_{Gn+S} = U_{GB} = U_{INPUT} = U_I = qV_I/k_B T$, and $U_{DR} = U_{Dn+S} = U_{DB} = U_{OUTPUT} = U_O = qV_O/k_B T$. Note subscript O here is for Output, not zero 0. In order to illustrate the device physics succinctly, we take $D_n = D_p = D$ so that electron and hole are interchangeable.

It is very important to note a cardinal device physics feature in the CMOS voltage inverter application, that is, when both the input voltage and output voltages are forced to be at one half of the power supply voltage, $U_I = U_O = U_{SS}/2$, the entire base region is at flatband, either a plane or a volume depending on solving the transistor as a 2-D or 3-D device. This flatband gives a very simple but most application important (maximum power dissipation solution) terminal current-voltage equation, which, from symmetry considerations, is also the peak current that can flow in the two surface channels and one volume channel in the 2-MOS-gate BiFET in the CMOS voltage inverter circuit connection. Using this important feature, without and before solving the five simultaneous equations given above, the exact total (not area density) electron current, I_N, (which is the sum of its surface and volume channel currents, which we can also compute separately, if needed, by x-integration or $U(x)$-integration between the gate-oxide/base-silicon interface and defined surface/volume channel boundary) and the exact total hole current I_P at $U_I = U_O = U_{SS}/2$ can be computed as follows where the device-physics-based coordinate normalizations are given by $X_B = x_B/L_D$ and $Y = y/L$ where L_D is the Debye length in the pure base and L is the base length:

$$I_N = qD(Wx_B)(N\partial U_N/\partial y) = qD(Wx_B)n_i \times \exp(U_{SS}/2 - U_N) \times (\partial U_N/\partial y)$$
$$= qD(W/L)(n_i L_D)X_B \times \exp(U_{SS}/2) \times \exp(-U_N) \times (\partial U_N/\partial Y) \quad (8)$$

$$I_P = qD(Wx_B)(P\partial U_P/\partial y) = qD(Wx_B)n_i \times \exp(U_P - U_{SS}/2)(\partial U_P/\partial y)$$
$$= qD(W/L)(n_i L_D)X_B \times \exp(U_{SS}/2) \times \exp(U_P - U_{SS}) \times (\partial U_P/\partial Y) \quad (9)$$

Using the boundary values of the electrochemical or quasi-Fermi potentials of electrons and holes given by (1) and (2) in the two total current equations given by (8) and (9)

$$U_N(Y = 0) = 0,$$
$$U_N(Y = 1) = U_P(Y = 1) = U_{SS}/2 \text{ and}$$
$$U_P(Y = 0) = U_{SS}, \quad (10)$$

we obtain the exact channel current expression at $U_I = U_O = U_{SS}/2$ which is a very simple one, most appealing certainly for compact modeling purposes (We temporarily call this the CMOS Leakage Current Peak Equation.):

$$I_{CH} = I_N = -I_P = (W/L)(qDn_i L_D)X_B[\exp(U_{SS}/2) - 1] \quad (11)$$

This is also the peak current, a very important number in applications with the consideration of power dissipation in the integrated circuits containing many MOS transistors.

When the input voltage deviates from $V_{SS}/2$, the output voltage and the channel current can only be obtained by numerically solving the simultaneous equations (3-7) with the boundary conditions (1-2).

It has been observed during our numerical calculation experiences, consistent with and expected from the well-known fact of the very steep or sharp-step in the voltage transfer characteristic of the CMOS voltage inverter circuit[7], that when the input voltage is only slightly less or more than $V_{SS}/2$, the output voltage is already very close to the power supply voltage or zero. The underlying device physics, readily proven by numerical calculations, is that when the input voltage is less than $V_{SS}/2$, a hole surface channel is formed in series with an electron volume channel, since the hole surface channel has much higher conductivity, due to high surface hole concentration, than the electron volume channel which has only the very low intrinsic electron concentration, most of the power supply voltage drop occurs along the electron volume channel. Thus the output voltage is close to the power supply voltage. Similarly, when the input voltage is larger than $V_{SS}/2$, a higher-conductivity electron surface channel is formed in series with the intrinsic-conductivity hole volume channel, most of the power supply voltage drop occurs along the hole volume channel, and thus the output voltage is close to the zero.

3 Analytical Solutions

3.1 Non-Recursive Solution

In order to obtain a fast numerical solution over the whole input voltage range of this CMOS voltage-inverter application of the single Bipolar Field Effect transistor with 2-MOS gates, simplifications of the five simultaneous equations (3-7) must be made. (Thickness and purity of the base layer are only special considerations made here by us to simplify the illustration on how this circuit works; they are not the necessary conditions, i.e. the transistor could be thick and not very pure, i.e., then it would approach two 1-gate bulk MOS transistors, and if for CMOS application, then the n-channel transistor and the p-channel transistor would require an abrupt or graded p/n junction or a buried oxide-or-insulator layer for isolation by dividing the base layer into two isolated base layers, but then without the most desirable consequences from the thin pure-base with simultaneous electron and hole surface and volume channels of our MOS Bi-FET.) To make these simplifications, four physical parameters are selected: (1) the surface potential at the source $Y=0$, U_{S0}, (2) the mid-plane potential at the source $Y=0$, U_{00}, (3) the total (areal density) hole concentration at the source $Y=0$, P_0, and (4) the total (areal density) electron concentration at the source $Y=0$, N_0. They are computed from the following equations where the integration is from $U=U_{00}$ to U_{S0}.

$$U_I - U_{S0} = \mathrm{Sign}(U_I - U_{SS}/2) \times (C_D/C_O) \times [\exp(U_{SS} - U_{S0}) - \exp(U_{SS} - U_{00}) + \exp(U_{S0}) - \exp(U_{00})]^{1/2} \quad (12)$$

$$X_B = \mathrm{Sign}(U_I - U_{SS}/2) \times 2 \times \int \partial_X U \div [\exp(U_{SS} - U) - \exp(U_{SS} - U_{00}) + \exp(U) - \exp(U_{00})]^{1/2} \quad (13)$$

$$P_0 = \mathrm{Sign}(U_I - U_{SS}/2) \times 2 \times (n_i L_D) \times \int \exp(U_{SS} - U) \partial_X U \div [\exp(U) - \exp(U_{00}) + \exp(U_{SS} - U) - \exp(U_{SS} - U_{00})]^{1/2} \quad (14)$$

$$N_0 = \mathrm{Sign}(U_I - U_{SS}/2) \times 2 \times (n_i L_D) \times \int \exp(U) \partial_X U \div [\exp(U) - \exp(U_{00}) + \exp(U_{SS} - U) - \exp(U_{SS} - U_{00})]^{1/2} \quad (15)$$

When the input voltage is less than half of the power supply voltage, the output voltage is very close to the power supply voltage, thus the following approximations are made to simplify the hole and electron current integrals:

$$\begin{aligned} I_P &= 2qDn_i W(L_D/L) \int (\partial_Y U_P) \exp(+U_P) \int \exp(-U) \partial_X U \div [\exp(U - U_N) - \exp(U_0 - U_N) \\ &\quad + \exp(U_P - U) - \exp(U_P - U_0)]^{1/2} \\ &\quad \text{with integration ranges of } U_P = U_{SS} \text{ to } U_O \text{ and } U = U_0 \text{ to } U_S \\ &\approx 2qDn_i L_D (W/L) \int (\partial_Y U_P) \exp(+U_{SS}) \int \exp(-U) \partial_X U \div [\exp(U - 0) - \exp(U_{00} - 0) \\ &\quad + \exp(U_{SS} - U) - \exp(U_{SS} - U_{00})]^{1/2} \\ &\quad \text{with integration ranges of } U_P = U_{SS} \text{ to } U_O \text{ and } U = U_{00} \text{ to } U_{S0} \\ &= 2qDn_i L_D (W/L)(U_O - U_{SS}) \int \exp(U_{SS} - U) \partial_X U \div [\exp(U) - \exp(U_{00}) \\ &\quad + \exp(U_{SS} - U) - \exp(U_{SS} - U_{00})]^{1/2} \\ &\quad \text{with integration range of } U = U_{00} \text{ to } U_{S0} \end{aligned}$$

$$I_P \approx + qD(W/L) \times (U_{SS} - U_O) \times P_0 \quad (16)$$

$$I_N = 2qDn_i L_D (W/L) \times (\partial U_N/\partial Y)\exp(-U_N)\int \exp(+U)\partial_X U \div [\exp(U-U_N) + \exp(U_0-U_N) + \exp(U_P-U) - \exp(U_P-U_0)]^{1/2}$$

with integration range of $U = U_0$ to U_S

$$\approx 2qDn_i L_D (W/L) \times (\partial U_N/\partial Y)\exp(-U_N)\int \exp(+U)\partial_X U \div [\exp(U-0) - \exp(U_{00}-0) + \exp(U_{SS}-U) - \exp(U_{SS}-U_{00})]^{1/2}$$

with integration range of $U = U_{00}$ to U_{S0}

$$I_N \approx -qD(W/L)(\partial U_N/\partial Y)\exp(-U_N) \times N_0 \tag{17}$$

Integrating (17) and using $U_N(Y=0)=0$ and $U_N(Y=1)=U_O$, we get

$$1-\exp(-U_O) = I_N \div [-qD(W/L) \times N_0] \tag{18}$$

Since $I_{CH} = -I_P = I_N$, combining (16) and (18)

$$1-\exp(-U_O) = (U_{SS}-U_O) \times P_0/N_0 \tag{19}$$

Noting $\exp(-U_O) \approx \exp(-U_{SS}) \ll 1$

$$U_{SS} - U_O = N_0/P_0 \tag{20}$$

$$I_{CH} = qD(W/L) \times N_0 \tag{21}$$

When the input voltage is larger than half of the power supply voltage, the output voltage is very close to the zero voltage, thus the following approximations are made to simplify the electron and hole current integrals:

$$I_N = 2qDn_i W(L_D/L)\int \partial_Y U_N \exp(-U_N)\int \exp(+U)\partial_X U \div [\exp(U-U_N) - \exp(U_0-U_N) + \exp(U_P-U) - \exp(U_P-U_0)]^{1/2}$$

with integration ranges of $U_N = 0$ to U_O and $U = U_0$ to U_S

$$\approx 2qDn_i L_D (W/L)\int \partial_Y U_N \exp(-0)\int \exp(+U)\partial_X U \div [\exp(U-0) - \exp(U_{00}-0) + \exp(U_{SS}-U) - \exp(U_{SS}-U_{00})]^{1/2}$$

with integration ranges of $U_N = 0$ to U_O and $U = U_{00}$ to U_{S0}

$$= 2qDn_i L_D (W/L) \times U_O \times \int \exp(U)\partial_X U \div [\exp(U) - \exp(U_{00}) + \exp(U_{SS}-U) - \exp(U_{SS}-U_{00})]^{1/2}$$

with integration range of $U = U_{00}$ to U_{S0}

$$I_N \approx qD(W/L) \times U_O \times N_0 \tag{22}$$

$$I_P = 2qDn_i W(L_D/L)(\partial U_P/\partial Y)\exp(U_P)\int \exp(-U)\partial_X U \div [\exp(U-U_N) + \exp(U_0-U_N) + \exp(U_P-U) - \exp(U_P-U_0)]^{1/2}$$

with integration range of $U = U_0$ to U_S

$$\approx 2qDn_i L_D (W/L)(\partial U_P/\partial Y)\exp(U_P)\int \exp(-U)\partial_X U \div [\exp(U-0) - \exp(U_{00}-0) + \exp(U_{SS}-U) - \exp(U_{SS}-U_{00})]^{1/2}$$

with integration range of $U = U_{00}$ to U_{S0}

$$= 2qDn_i L_D (W/L)(\partial U_P/\partial Y)\exp(U_P - U_{SS})\int \exp(U_{SS}-U)\partial_X U \div [\exp(U) - \exp(U_{00}) + \exp(U_{SS}-U) - \exp(U_{SS}-U_{00})]^{1/2}$$

with integration range of $U = U_{00}$ to U_{S0}

$$I_P \approx qD(W/L) \times (\partial U_P/\partial Y)\exp(U_P - U_{SS}) \times P_0 \tag{23}$$

Integrating (23) and using $U_P(Y=0) = U_{SS}$ and $U_P(Y=1) = U_O$

$$\exp(U_O - U_{SS}) - 1 = I_P/[qD(W/L) \times P_0] \tag{24}$$

Since $I_{CH} = -I_P = I_N$, combining (22) and (24)

$$\exp(U_O - U_{SS}) - 1 = -U_O \times N_0/P_0 \tag{25}$$

Noting $\exp(U_O - U_{SS}) \approx \exp(-U_{SS}) \ll 1$

$$U_O = P_0/N_0 \tag{26}$$

$$I_{CH} = qD(W/L) \times P_0 \tag{27}$$

The equations (12-15), (20-21) and (26-27), taken together, is the non-recursive approximate solution of the BiFET in the CMOS voltage inverter bias configuration which are derived from the recursive exact solution given by the five simultaneous equations (3-7).

3.2 Close-Form Solution

It is obvious that the equations (12-15) for four physical parameters, U_{00}, U_{S0}, P_0, and N_0 are still sufficiently too complicated for compact modeling. The following derivation is to simplify these equations further by use of the Taylor series expansion. To make the algebra easy, the following variable transformations are made:

$$u_I = U_I - U_{SS}/2, u_S = U_{S0} - U_{SS}/2, u_0 = U_{00} - U_{SS}/2, u = U - U_{SS}/2 \tag{28}$$

Equations (12-15) can then be rewritten as follows with the integration range of $u = u_0$ to u_S

$$u_I - u_S = \mathrm{Sign}(u_I) \times (C_D/C_O) \times \exp(U_{SS}/4) \times [\exp(-u_S) - \exp(-u_0) + \exp(u_S) - \exp(u_0)]^{1/2} \tag{29}$$

$$X_B = \mathrm{Sign}(u_I) \times 2 \times \exp(-U_{SS}/4) \int \partial_X u \div [\exp(-u) - \exp(-u_0) + \exp(u) - \exp(u_0)]^{1/2} \tag{30}$$

$$P_0 = n_i L_D \times \mathrm{Sign}(u_I) \times 2 \times \exp(U_{SS}/4) \int \exp(-u) \partial_X u \div [\exp(-u) - \exp(-u_0) + \exp(u) - \exp(u_0)]^{1/2} \tag{31}$$

$$N_0 = n_i L_D \times \mathrm{Sign}(u_I) \times 2 \times \exp(U_{SS}/4) \int \exp(+u) \partial_X u \div [\exp(-u) - \exp(-u_0) + \exp(u) - \exp(u_0)]^{1/2} \tag{32}$$

The second order Taylor expansion gives:

$$\exp(-u) - \exp(-u_0) + \exp(u) - \exp(u_0) \approx u^2 - u_0^2 \tag{33}$$

From the thickness equation (30),

$$X_B \approx 4 \exp(-U_{SS}/4) \times [(u_S - u_0)/(2u_0)]^{1/2} \times [1 - (1/3)(u_S - u_0)/(4u_0)] \tag{34}$$

Let $t = [(u_S - u_0)/(2u_0)]^{1/2} < 1$, then (34) can be rearranged as follows:

$$t = (X_B/4) \times \exp(U_{SS}/4) + (1/6) \times t^3 \tag{35}$$

From the voltage equation (29),

$$u_0 \approx u_I \div [(C_D/C_O) \times \exp(U_{SS}/4) \times 2t \times (1 + t^2)^{1/2} + 2t^2 + 1] \tag{36}$$

The total (areal density) hole concentration, (31), is approximated by

$$P_0 \approx (n_i L_D) 4 \times \exp[(U_{SS}/4) - u_0] \times [1 - (1 + 0.25/u_0)/3 \times (2t^2 u_0)] t \tag{37}$$

From the total (areal density) electron concentration equation (32),

$$N_0 \approx (n_i L_D) 4 \times \exp[(U_{SS}/4) + u_0] \times [1 + (1 - 0.25/u_0)/3 \times (2t^2 u_0)] t \tag{38}$$

The simplified approximation equations (35-38), (20-21), and (26-27) give a compact solution for the current-voltage and voltage-voltage characteristics of the 2-MOS-gate thin pure-base Bipolar Field-Effect transistor as wired for the CMOS voltage inverter operation.

4 Computed Transfer Characteristics

4.1 Comparison of the 1-BiFET and 2-UniFET CMOS Voltage Inverters

It is very important for us to provide a comparison of this novel one-BiFET (1-Transistor or 1-T) CMOS voltage inverter with the two-UniFET (2-Transistor or 2-T) CMOS voltage inverter which was first demonstrated and reported by Wanlass, Moore and Sah[2,3] in 1963. For this comparison, we use the ideal 2-T CMOS voltage inverter which was described by the 1964-Sah drift-current-only model, given by Equations (672.15) to (672.22) in section 672 of FSSE[7]. Based on the discussion of the threshold voltage of a BiFET in [9], we will assume that the p-UniFET has a threshold voltage $V_{TP} = -kT/q \log_e(C_O/C_D)$ while the n-UniFET has $V_{TN} = kT/q \log_e(C_O/C_D)$. In addition, the diffusion current in the subthreshold range of the two UniFETs, neglected in the UniFET CMOS example given by Fig. 672.24 on page 631 of FSSE[7] are now taken into account using the subthreshold diffusion-current approximation given by section 682 and Fig. 682.1 on page 655 of FSSE[7].

Figure 2 (a) shows that the one-BiFET CMOS voltage inverter (solid line) has a much sharper transition at transition voltage $V_{TR} = V_{SS}/2$ than that of the two-UniFET CMOS voltage inverter (dash lines). Figure 2 (b) shows that (i) the channel current peak, I_{TR}, of the 2-T UniFET CMOS voltage inverter have

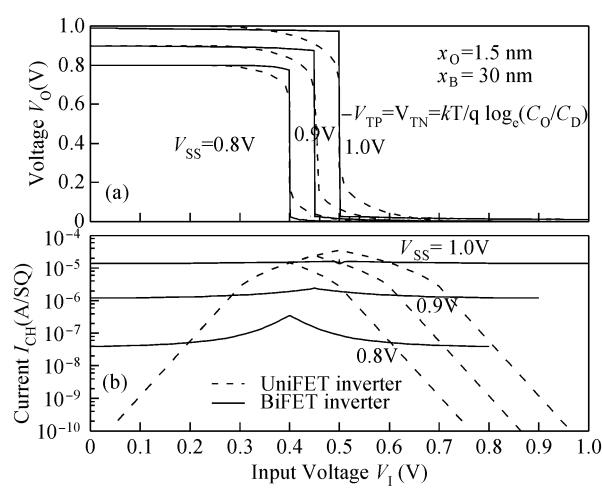

Fig. 2 Comparison of the one-BiFET CMOS voltage inverter and the two-UniFET CMOS voltage inverter.

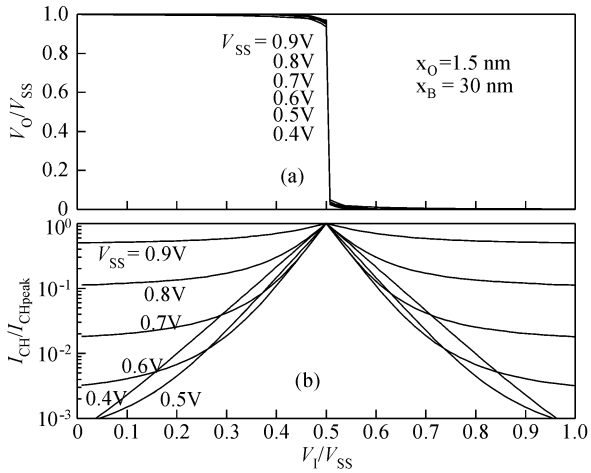

Fig. 3　Normalized transfer characteristics of a BiFET with two MOS gates and pure base under the CMOS voltage inverter circuit operation, with V_{SS} varied.

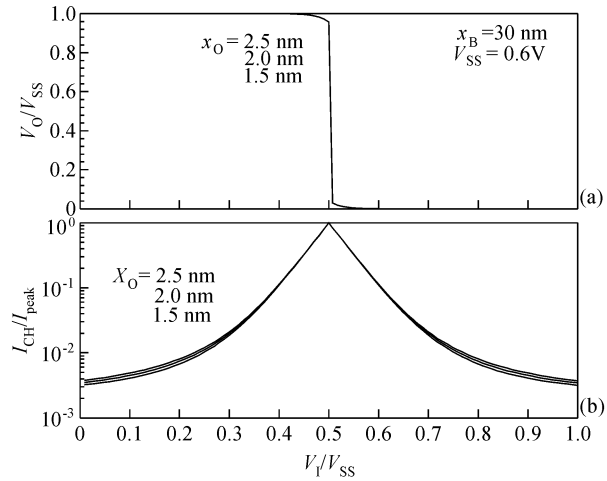

Fig. 5　Normalized transfer characteristics of a BiFET with two MOS gates and pure base under the CMOS voltage inverter circuit operation, with X_O varied.

slower rise with the power supply voltage, V_{SS}, than that of the 1-T BiFET CMOS voltage inverter; and (ii) the current in the 2-T UniFET CMOS voltage inverter has a sharper or exponential drop-off with the input voltage at the nearly ideal slope of 60mV per decay of a subthreshold surface inversion channel, while the current in the 1-T BiFET CMOS voltage inverter has a bell-shaped characteristic leveling off at the volume channel leakage current. These differences are accounted for analytically. For the 2-UniFET CMOS inverter Equation (672.19) of FSSE[7] gave $I_{TR} \sim V_{SS}^2$, and at the transition voltage, one saturated surface inversion p-channel and one saturated surface inversion n-channel are in series. For the 1-BiFET CMOS inverter, Equation (11) of this paper gave $I_{TR} \sim \exp(V_{SS}/2)$, and at the transition voltage, one volume p-channel and one volume n-channel are in series. Thus, the 2-UniFET CMOS inverter at both of the two quiescent states, $V_{INPUT} = 0$ or V_{SS}, has a subthreshold surface inversion channel (electron or hole) which leads to exponentially very small channel current that is exponentially dependent on the input voltage; while the 1-BiFET CMOS inverter at the two quiescent states, $V_{INPUT} = 0$ or V_{SS}, has a volume channel which leads to large channel current, but only nearly linear dependence on the power supply voltage applied to a thin intrinsic or pure silicon resistance with its width slightly modulated by the width of the two surface channels.

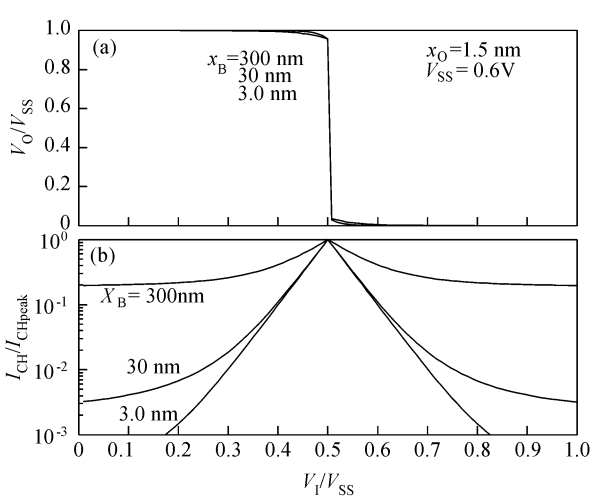

Fig. 4　Normalized transfer characteristics of a BiFET with two MOS gates and pure base under the CMOS voltage inverter circuit operation, with X_B varied.

4.2　Dependences of the 1-BiFET CMOS Voltage Inverter Characteristics on V_{SS}, X_B and X_O

The power supply voltage dependence of the voltage transfer and current transfer characteristics are computed using the recursive algorithm to investigate the power-supply voltage dependences, V_{SS}, and the dependences on the pure-base thickness, X_B, and gate oxide thickness, X_O. These are presented respectively in Figs. 3, 4, and 5, in normalized scales in order to show the salient features. Figures 3(a), 4(a) and 5(a) indicate that the sharp voltage transition shape is hardly affected by these three variables. Figure (b)'s show that the current decays exponentially with increasing $V_I = V_{INPUT}$ but overtaken quickly by the volume channel leakage current, while the quiescent state current increases with channel thickness as X_B^2 (in the 3nm to 300nm range) but nearly independent of the oxide thickness X_O (in the 1.5nm to 2.4nm range). These are consistent with that expected from the device equations and device physics.

4.3　Current Peak and Switching Power Dissipation

Peak current and switching power dissipation are

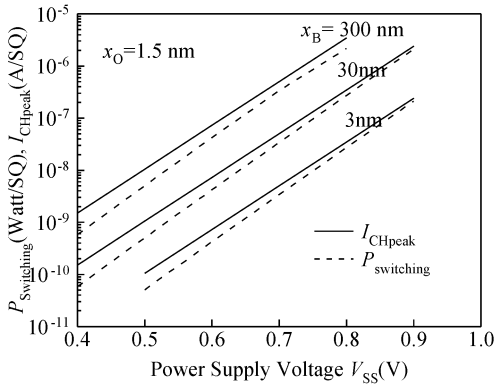

Fig. 6 Channel current peak value, I_{CHpeak}, and power dissipation, $P_{switching}$, of a BiFET with two MOS gates and pure base under the CMOS voltage inverter circuit operation, as a function of V_{SS} with X_B varied. Note that I_{CHpeak} and $P_{switching}$ are independent of X_O.

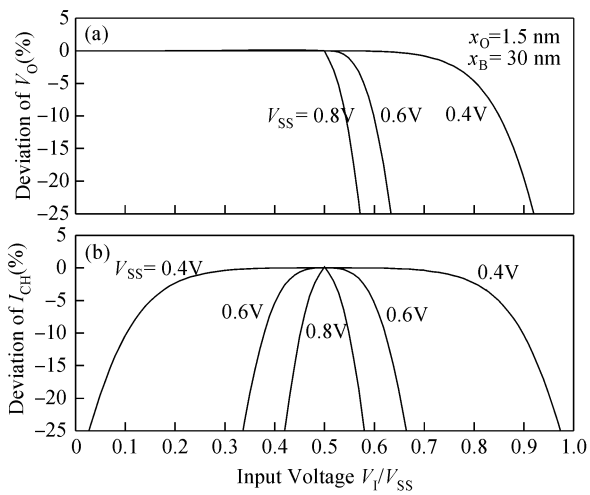

Fig. 7 Percentage deviation of channel current and output voltage of the close-form solution from the non-recursive solution, with V_{SS} varied.

the most important characteristics in circuit applications. Figure 6 shows the dependences of these characteristics on the power supply voltage, V_{SS}, with base thickness in the range of 3nm to 300nm and oxide thickness of 1.5nm since they are relatively insensitive to the latter. The computed curves show the expected linear dependence on the base layer thickness X_B from the leakage current through the width of the pure silicon base. They both show the exponential dependence on the power supply voltage V_{SS} with a slope (or voltage swing per decade of currents) between the two ideal limits of k_BT/q at 60mV and $2k_BT/q$ at 120mV per decade of current change.

4.4 Deviations of the Compact Solution

The deviations of the compact solution of the output voltage, V_O, and the channel current, I_{CH}, from their corresponding non-recursive solutions are shown in Figs. 7 (a) and 7 (b). The increasing V_O deviations occur when V_I is closer to V_{SS} and when V_O approaches zero. Similarly, the increasing percentage-deviation of I_{CH} occurs when V_I approaches the quiescent voltages, 0 and V_{SS}, where the current is small. Thus, deviations of the compact solution should not be serious when design applications require the use of the much faster compact solution.

5 Summary

We have presented in this paper the current-voltage and voltage-voltage transfer characteristics and power-dissipation-vs-supply-voltage characteristics of the 1-BiFET CMOS voltage inverter circuit. We also investigated the deviation of the compact solution from the recursive-iteration solution and compared the CMOS voltage inverter circuit using 1-BiFET with that using 2-UniFET.

Acknowledgment We thank Professor Wang Yangyuan of Peking University, Academician of Chinese Academy of Sciences, for his supports which have enabled us to undertake this study.

References

[1] Chih-Tang Sah, "Evolution of the MOS Transistor - from Conception to VLSI," Proceedings of the IEEE, 76(10), 1280-1326, October, 1988. For Shockley-Pearson field-effect experiment, see descriptions in the text citing reference [18]. See text describing Figs. 1-3 for Lilienfeld's 1926-1928 patents of field effect transistors based on the conductivity modulation principle which he explicitly stated in the patents. See text description for reference [30] on Shockley's invention of the unipolar field-effect transistor based on conductance modulation via the volume channel thickness by the two p/n junction gates.

[2] Frank Wanlass and Chih-Tang Sah, "Nanowatt Logic Using Field-Effect Metal-Oxide Semiconductor Triodes", IEEE Solid-State Circuit Conference Proceedings, 32-33, February 20, 1963.

[3] Gordon E. Moore, Chih-Tang Sah, Frank Wanlass, "Metal-Oxide-Semiconductor Field-Effect Devices for Micropower Logic Circuitry," 41-55, in Micropower Electronics, Edited by Edward Keonjian, New York: Pergamon Press, 1964.

[4] Chih-Tang Sah and Bin B. Jie, "Double-Gate Thin-Base MOS Transistor: The Correct Theory," and Bin B. Jie and Chih-Tang Sah, "Double-Gate Thin-Base MOS Transistor: Characteristics for the Short Channel," Late-News Papers presented on May 23, 2007 at the Workshop on Compact Modeling (WCM2007) of the NSTI Nanotechnology Conference and Trade Show, May 22-24, 2007, hosted by the Nano Science and Technology Institute, Cambridge, MA02139, USA. http://www.nsti.org/Nanotech2007/WCM2007/.

[5] Chih-Tang Sah and Bin B. Jie, "Bipolar Theory of MOS Field-Effect Transistors and Experiments," Chinese J. Semiconductors, 28(10), 1497-1502, October, 2007.

[6] H.S. Fu and Chih-Tang Sah, "A distributed-gate bistable MOS transistor", Solid-State Electronics, 14(9), 799-804, September, 1971.

[7] Chih-Tang Sah, Fundamentals of Solid-State Electronics, Singa-

pore：World Scientific Publishing Company，1991. For CMOS，see pages 624-631. For the two BBB circuits，see section 663 on pages 583 to 595 on the charge transfer gate，and section 672 on pages 614－631 on the MOS inverters.

[8] Chih-Tang Sah and Bin B. Jie，"The Theory of Field-Effect Transistors：XI. The Bipolar Electrochemical Currents（1-2-MOS-Gates on Thin-Thick Pure-Impure Base），" Journal of Semiconductors，29(3)，397-409，March 2008.

[9] Chih-Tang Sah and Bin B. Jie，"The Bipolar Field-Effect Transistor Theory：I. Electrochemical Current Theory（Two-MOS-Gates on Pure-Base），" Chinese Journal of Semiconductors，28(11)，1661-1673，November 2007.

双极场引晶体管：VI. CMOS 电压倒相电路（双 MOS 栅纯基）*，**

揭斌斌[1,†]　薛支唐[1,2,3,†]

（1 北京大学，北京　100871）
（2 佛罗里达大学，佛罗里达州 Gainesville，FL 32605，美国）
（3 中国科学院外籍院士，北京　100864）

摘要：本文报告了硅互补金属氧化层硅（CMOS）电压倒相电路的直流稳态电压和电流转移特性和功率耗散. 这电路用一只实际的、纳米尺度的双极场引晶体管（BiFET）实现. 通过数字求解五个偏微分方程，可获得这些电学特性. 方程是基于这种器件结构：在薄纯硅基层的两表面上各有一个 MOS 栅，在这薄基的两端都有电子和空穴接触. 内部条件和 CMOS 边界条件用于三种势（静电势和电子及空穴电化学势）. 用一台装有 Windows XP－PRO 下的 64 位 FORTRAN 语言的双核个人计算机，快速地计算出一系列曲线.

关键词：双极场引晶体管理论；表面沟道；体积沟道；CMOS 倒相器；CMOS-BiFET
PACC：7340Q　　**EEACC**：2560S；2560B
中图分类号：TN386.1　　**文献标识码**：A　　**文章编号**：0253-4177(2008)11-2079-09

* 该研究及揭斌斌由 CTSAH Associates（CTSA）资助. CTSA 由萨故夫人张淑南创建. 记念她第七十年.
** 萨支唐写成此摘要基于揭斌斌的现代语初稿. 感谢潘胜和北京大学原物理系教师赵立群和潘桂明的修改建议.
† 通信作者. Email：bb_jie@msn.com and tom_sah@msn.com
2008-10-23 收到，2008-10-28 定稿