A cross-coupled-structure-based temperature sensor with reduced process variation sensitivity*

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Abstract: An innovative, thermally-insensitive phenomenon of cascaded cross-coupled structures is found. And a novel CMOS temperature sensor based on a cross-coupled structure is proposed. This sensor consists of two different ring oscillators. The first ring oscillator generates pulses that have a period, changing linearly with temperature. Instead of using the system clock like in traditional sensors, the second oscillator utilizes a cascaded cross-coupled structure to generate temperature independent pulses to capture the result from the first oscillator. Due to the compensation between the two ring oscillators, errors caused by supply voltage variations and systematic process variations are reduced. The layout design of the sensor is based on the TSMC13G process standard cell library. Only three inverters are modified for proper channel width tuning without any other custom design. This allows for an easy integration of the sensor into cell-based chips. Post-layout simulations results show that an error lower than ±1.1 °C can be achieved in the full temperature range from −40 to 120 °C. As shown by SPICE simulations, the thermal insensitivity of the cross-coupled inverters can be realized for various TSMC technologies: 0.25 μm, 0.18 μm, 0.13 μm, and 65 nm.

Key words: CMOS; cross-coupled; delay; ring oscillator; temperature sensor; thermal insensitivity
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1. Introduction

In recent years, the power density and overall power dissipation of high performance chips increased continuously due to advances in the sub-micron technology and the increase of the number of transistors used in CMOS ICs. The increased power density introduces the problem of self-heating. According to Ref. [1], the highest hotspot temperature can be up to 120 °C. But a high temperature seriously harms the performance and reliability, and increases the subthreshold leakage of CMOS chips. Therefore, temperature sensors are implemented for thermal monitoring in order to control the clock frequency, the fan speed or the supply voltage[2, 3]. Only a few reports dealing with on-chip temperature monitoring have been published[4].

One problem of most proposed sensors is that they are designed using analog circuitry, which is not easy to integrate into cell-based designs. However, nowadays, cell-based design is an important trend for system-on-a-chip (SoC) chips. Some analog sensors[4–6] determine the temperature via a voltage or current measurement. In order to get a digital output, an additional analog circuit, such as an analog-to-digital converter (ADC) is needed. The integrated ADC increases the circuit area and the design complexity, and it leads to noise immunity problems. Chen *et al.*[7] integrated a special time-to-digital converter instead of an ADC into their temperature sensor. However, their sensor still has other types of analog circuits. Law *et al.*[8] proposed a sensor working in the time domain with a reduced supply voltage sensitivity. It is composed of analog circuits such as amplifiers and current mirrors.

Another problem is that most temperature sensors suffer from process variations. To eliminate these errors, the sensors have to be calibrated after fabrication. The calibration creates extra cost for the sensors, thus making their usage less likely. The sensors with nonlinear temperature output characteristics would cost more than the linear ones.

The ring oscillator is one of the well-known temperature sensor types[9, 10]. For these sensors no ADC is needed. The ring oscillator can be implemented using only digital and no analog circuitry[11]. This allows for an easily integration into cell-based designs. As depicted in Fig. 1(a), conventional ring-oscillator-based temperature sensors take advantage of the fact that the period of the ring oscillator is proportional to the temperature. In addition, the system clock is used as a reference in order to capture the results from the sensing oscillator. The frequency of the ring oscillator is very sensitive to process and supply voltage variations, while the system clock period is constant. Hence, errors caused by process and voltage variations are large for traditional ring-oscillator-based sensors.

In this paper, we propose an innovative, thermally-independent cross-coupled-structure. The structure is utilized in the design of a fully-digital temperature sensor, which is easy to integrate into cell-based chips. The block diagram of the proposed sensor is shown in Fig. 1(b). This sensor employs a temperature insensitive ring oscillator instead of the system clock. Because of the compensation between the two ring oscillators, the errors caused by process and supply voltage variations are reduced.

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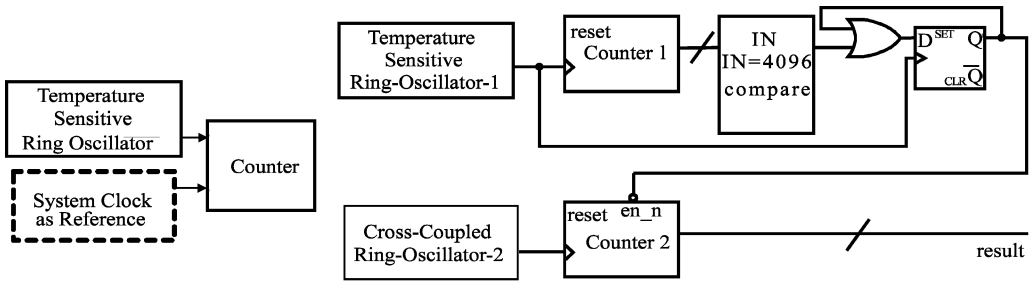

Fig. 1. (a) Conventional ring-oscillator-based temperature sensor; (b) Proposed temperature sensor.

2. Design of the cross-coupled-structure-based temperature sensor

The proposed sensor contains two ring oscillators, as depicted in Fig. 1. Ring-oscillator-1 is based on cascaded inverters. It has a linear dependence on temperature. Ring-oscillator-2 acts like a system clock and is not sensitive to temperature, since it is based on cross-coupled inverters.

2.1. Temperature sensitive ring oscillator

It is important to note that the delay of a CMOS logic gate is linearly proportional to the temperature. Taking advantage of this temperature dependency, CMOS delay lines can be used as the temperature-detecting element in sensor circuits[7, 11]. Ring-oscillator-1 is composed of an odd number of inverter gates connected in a circular chain. Thus, the ring oscillator can stimulate itself. The period of a ring oscillator can be expressed as

$$T_{\mathrm{P}} = N(T_{\mathrm{PLH}} + T_{\mathrm{PHL}}), \tag{1}$$

where N is the number of inverter stages in the ring oscillator, and T_{PLH} and T_{PHL} stand for the low-to-high and high-to-low transition delays. For a step input and with the assumption of negligible nonideal effects such as channel length modulation, the high-to-low and low-to-high propagation delay of an inverter can according to Ref. [12] be given as

$$T_{\mathrm{PHL}} = \frac{2C_{\mathrm{L}}V_{\mathrm{TN}}}{K_{\mathrm{N}}(V_{\mathrm{DD}} - V_{\mathrm{TN}})^2} + \frac{C_{\mathrm{L}}}{K_{\mathrm{N}}(V_{\mathrm{DD}} - V_{\mathrm{TN}})} \ln \frac{1.5V_{\mathrm{DD}} - 2V_{\mathrm{TN}}}{0.5V_{\mathrm{DD}}}, \tag{2}$$

$$T_{\mathrm{PLH}} = \frac{-2C_{\mathrm{L}}V_{\mathrm{TP}}}{K_{\mathrm{P}}(V_{\mathrm{DD}} + V_{\mathrm{TP}})^2} + \frac{C_{\mathrm{L}}}{K_{\mathrm{P}}(V_{\mathrm{DD}} + V_{\mathrm{TP}})} \ln \frac{1.5V_{\mathrm{DD}} + 2V_{\mathrm{TP}}}{0.5V_{\mathrm{DD}}}, \tag{3}$$

where $K_{\mathrm{N}} = \mu_{\mathrm{N}}C_{\mathrm{OX}}(W/L)_{\mathrm{N}}$, $K_{\mathrm{P}} = \mu_{\mathrm{P}}C_{\mathrm{OX}}(W/L)_{\mathrm{P}}$ are the transconductance parameters, and C_{L} is the effective load of the inverter. Here, the value of V_{TP} is always negative.

Among the parameters of T_{PLH} and T_{PHL}, the mobility μ and the threshold voltage V_{T} are temperature sensitive[13]:

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{km} \tag{4}$$

$$V_{\mathrm{T}}(T) = V_{\mathrm{T}}(T_0) + \alpha_{\mathrm{T}}(T - T_0), \tag{5}$$

where T_0 is the reference temperature, μ_0 is the mobility, and $V_{\mathrm{T}}(T_0)$ is the threshold voltage at the reference temperature T_0. The parameter km is always between -2.0 and -1.2, while the parameter α_{T} is always in the range of -3.0 to -0.5 mV/°C. With an increase in temperature, both μ and V_{T} decrease. Since the mobility and the threshold voltage adversely affect the delay, they cancel each other. For normal operation, the supply voltage V_{DD} is much larger than V_{T}. So according to Eqs. (2) and (3), the thermal behavior of the propagation delay is dominated by the mobility μ and the thermal coefficient of the propagation delay is positive. As the temperature increases, the propagation delay increases almost linearly.

2.2. Temperature-insensitive ring oscillator based on cross-coupled inverters

For a reduced supply voltage, the CMOS gate propagation delay may increase when the temperature decreases. Thus, the worst case delay is at −40 °C. This phenomenon leads to a reversal of the temperature dependence[14]. In this paper, we have found another phenomenon: for cascaded cross-coupled inverters the reversal of the temperature dependence can happen for normal operating voltages. In the Ring-oscillator-2, we assign T_{PLH} to be the negative temperature coefficient and T_{PHL} to be the positive coefficient. Then a temperature independency of the period, as decided by the sum of T_{PLH} and T_{PHL}, can be achieved.

First, we describe the phenomenon of the reversal of the thermal dependence of T_{PLH}. This can happen due to an interaction of two adjacent stages in a chain. To simplify the explanation of this phenomenon, we suppose a step high-to-low input pulse that leads to a low-to-high transition on node OUT, and we ignore the feedback of the second stage inverter inv2, as shown in Fig. 2. Under these simplified conditions, the two inverters inv1_r and inv2 work as load capacitances. The channel widths of inv1_r and inv2_r are smaller than the widths of inv1 and inv2.

Here, T_{PLH} is defined as the time interval from the step high-to-low input transition to the time when OUT reaches half supply voltage. Given a falling transition at node IN, the charge current flows to the node OUT through P1; at the same time a discharge current flows through N2, which works against P1. Finally, the voltage on node OUT changes from

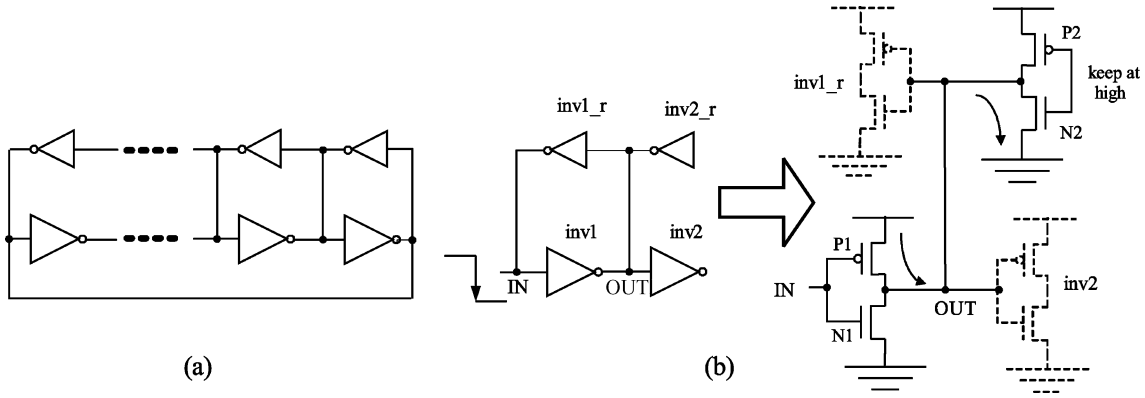

Fig. 2. (a) Ring-oscillator-2 with $2N$+1 stages of cross-coupled inverters; (b) Low-to-high transition between adjacent stages of two cross-coupled inverters.

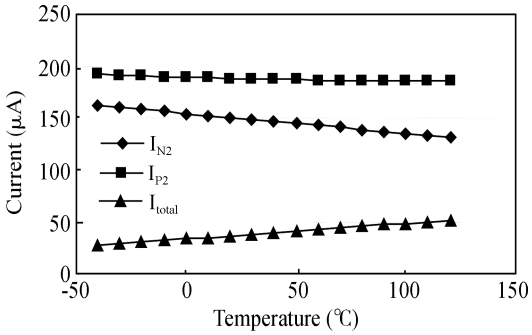

Fig. 3. Saturation current versus temperature.

zero to $V_{DD}/2$. The propagation delay of the oscillator depends on how fast the gates are charged, which is decided by the current charging the node OUT.

To demonstrate the thermal characteristic of T_{PLH}, let us use the first-order approximation:

$$T_{PLH} = \frac{C_L \frac{1}{2} V_{DD}}{I_{total}}. \tag{6}$$

The total current that charges the node OUT can be expressed as

$$I_{total} = I_{P1} - I_{N2}. \tag{7}$$

From the alpha power law model[15], it is known that

$$I = K(V_{DD} - V_T)^{\alpha}. \tag{8}$$

By substituting Eq. (8) back into Eq. (7), we have:

$$I_{total} = K_{P1}(V_{DD} + V_{TP})^{\alpha} - K_{N2}(V_{DD} - V_{TN})^{\alpha}. \tag{9}$$

Empirically, α can be set to 1.25[16]. In the saturation or linear regions, the drain-source current is dominated by the carrier mobility. As the temperature increases, the mobility decreases, as indicated by Eq. (4). Therefore, both currents I_{P1} and I_{N2} will decrease as the temperature increases, as shown in Fig. 3. However, in the mentioned silicon processes, the absolute value of km_N is always larger than that of km_P. Therefore, the sensitivity of I_N is always greater than that of I_P. That is why I_N decreases more rapidly than I_P. When a certain ratio of I_{P1}/I_{N2} is reached, I_{total} will increase with temperature.

To guaranty the correct function of the circuit and the reversed temperature sensitivity, two conditions must be satisfied at the same time:

(1) I_{total} should be positive, which means I_{P1} should be larger than I_{N2} when V_{OUT} is discharged from V_{DD} to $V_{DD}/2$. Since both $|V_{TP}|$ and $|V_{TN}|$ are smaller than V_{DD}, the Taylor series expansion of Eq. (9) gives:

$$I_{total} = K_{P1}(V_{DD} + 1.25V_{TP}) - K_{N2}(V_{DD} - 1.25V_{TN}) > 0. \tag{10}$$

Assuming that the channel length is set to the minimum feature size, the following expression can be deduced:

$$\frac{W_{P1}}{W_{N2}} > \frac{\mu_{0N}}{\mu_{0P}} \left(\frac{T}{T_0}\right)^{km_N - km_P} \frac{4V_{DD} - 5V_{TN}}{4V_{DD} + 5V_{TP}}. \tag{11}$$

(2) However, I_{N2} should also be large enough to control the temperature sensitivity.

To have reversed temperature sensitivity, the derivative of the total current with respect to the temperature must be positive, as shown in Fig. 3:

$$\frac{\partial(I_{P1} - I_{N2})}{\partial T} > 0. \tag{12}$$

Combining Eqs. (9), (4), and (5), we get the differential form of the current:

$$\frac{\partial I}{\partial T} = \frac{W}{L} C_{OX} \mu_0 \mathrm{KI}, \tag{13}$$

where

$$\mathrm{KI} = km \left(\frac{T}{T_0}\right)^{km-1} [V_{DD} - V_T(T_0) - \alpha_T(T - T_0)]^{\alpha} - \alpha\alpha_T \left(\frac{T}{T_0}\right)^{km} [V_{DD} - V_T(T_0) - \alpha_T(T - T_0)]^{\alpha-1}.$$

Here, KI represents the intrinsic temperature characteristic of the drain-source current. KI is not related to the layout size.

By combining Eqs. (12) and (13), we get the second condition:

$$\frac{W_{P1}}{W_{N2}} < \frac{\mu_{0N}\mathrm{KI}_N}{\mu_{0P}\mathrm{KI}_P}, \tag{14}$$

where KI_N and KI_P are both negative, and they represent the temperature sensitivity of the NMOS and the PMOS, respectively. According to Eq. (14), the total current increases when the temperature increases; i.e., we get the reversed delay-temperature relationship of T_{PHL}.

Table 1. Temperature characteristics of NMOS and PMOS transistors based on BSIM3v3 or BSIM4 models.

	NMOS current sensitivity	PMOS current sensitivity
TSMC 0.25 μm	26%	19%
TSMC 0.18 μm	31%	21%
TSMC 0.13G	25%	17%
TSMC 0.13LV	26%	21%
TSMC 65 nm	16%	7%

The two proposed conditions can be summarized as

$$\frac{\mu_{0N}}{\mu_{0P}}\left(\frac{T}{T_0}\right)_N^{km_N-km_P}\frac{4V_{DD}-5V_{TN}}{4V_{DD}+5V_{TP}}<\frac{W_{P1}}{W_{N2}}<\frac{\mu_{0N}KI_N}{\mu_{0P}KI_P}. \quad (15)$$

Essentially, this phenomenon depends on one important condition:

$$\left(\frac{T}{T_0}\right)^{km_N-km_P}\frac{4V_{DD}-5V_{TN}}{4V_{DD}+5V_{TP}}<\frac{KI_N}{KI_P}. \quad (16)$$

Equation (16) involves technology parameters and it should be satisfied in the full temperature range. The left side of the inequality is approximately equal to 1 since the value of $|V_{TP}|$ and $|V_{TN}|$ are nearly equal. In order for Eq.(16) to be valid, KI_N must be greater than KI_P. Thus the temperature dependence of the NMOS must be larger than the temperature dependence of the PMOS. This condition is satisfied for technologies from TSMC, as shown in Table 1.

We have simulated the saturation currents for different TSMC technology models. The results of these simulations are summarized in Table 1. The sensitivity of the current with respect to temperature is defined as

$$\frac{\text{current(LowTemperature)}-\text{current(HighTemperature)}}{\text{current(LowTemperature)}}.$$

The given NMOS and PMOS sensitivities can be used for a comparison of KI_N and KI_P. We can see from Table 1, that the NMOS transistor has a larger temperature coefficient for all the listed technologies. We have simulated ring oscillators composed of identical cross-coupled structures based on those technologies, and we have observed negative or zero temperature coefficients in those simulations.

Unlike P1 and N2 in T_{PLH}, N1 and P2 in T_{PHL} cannot satisfy Eq. (16). Hence, T_{PHL} cannot have this reversed dependency. The temperature coefficient of the oscillation period T_P can be tailored to be negative or zero. By choosing large values for W_{N1} and W_{P2}, T_{PHL} will be much smaller than T_{PLH}, causing T_{PLH} to dominate the temperature dependence of T_P.

To implement a temperature insensitive ring oscillator, Ring-oscillator-2 must follow the proposed design principle given by Eq. (15). The calculated results for the channel widths are used as starting values in cross-coupled inverters and then fine-tuned by simulation. The relative channel width ratios $W_{P1} : W_{N1} : W_{P2} : W_{N2}$ in our design are set to 5.6 : 4 : 1.2 : 1.

2.3. Function of the temperature sensor

Traditional oscillator-based sensors always utilize the system clock to capture sensed results such as the number of periods. As depicted in Fig. 1, during the oscillation en_n (low active count enable) is kept low and Counter-2, which acts like a system clock, clocks in the signal from Ring-oscillator-2. After a certain number of Ring-oscillator-1 periods, en_n is driven high by the compare block and the OR gate. This will cause the captured temperature result to be stored in the register of the second counter. In this way, the output result will be binary and increases linearly with temperature. The registers and counters will be reset before the next temperature sensing event. The schematic of the proposed sensor is shown in Fig. 1. In this design the buffers are inserted between the oscillators and the counters[7] in order to circumvent the runt pulse phenomenon and to minimize the load for the oscillators. The highest significant bit of Counter 1 is used to trigger the OR gate and a compare block is not needed.

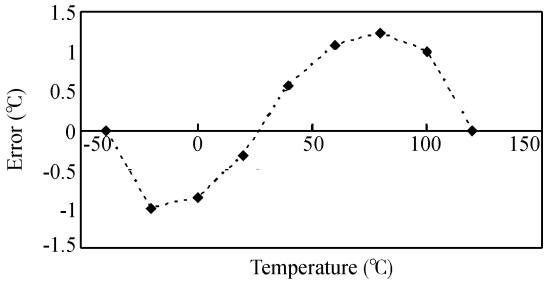

Fig. 4. Error in temperature versus real temperature according to a post-layout simulation for a typical corner and a supply voltage of 1.0 V. The error is defined as the difference between the measured temperature and the real temperature.

To increase the sensing resolution, the first ring oscillator should be as temperature sensitive as possible. According to the conclusion of part 2.2, the delay due to the NMOS transistors should be much larger than the delay due to the PMOS transistors. This means that the channel width of the NMOSs in the inverter should be much smaller than that of PMOSs. The widths of the transistors forming the inverters of Ring-oscillator-1 are set accordingly.

3. Simulation results

The sensor layout is implemented with the ARM standard cell library using TSMC 013G (0.13 μm) technology. The whole design of the proposed sensor utilizes commercial EDA tools without any custom design. The modification of the inverter layout including placement and routing are all done in Synopsys Astro. Calibre is used for the extraction of *RC* parasitic and HSPICE is used for the post-layout simulation. The total area of the sensor is less than 3600 μm^2.

According to post-layout simulations in a full SPICE model temperature range from −40 to 120 °C, the resolution is about 0.6 °C and the maximum error in typical corners is within ±1.1 °C, as shown in Fig. 4. The resolution is related to the counter's valid range. A better resolution needs a larger counter area and a slower response. Thus, a trade-off between resolution, circuit area and response time needs to be made. We have chosen to keep the resolution below the maximum

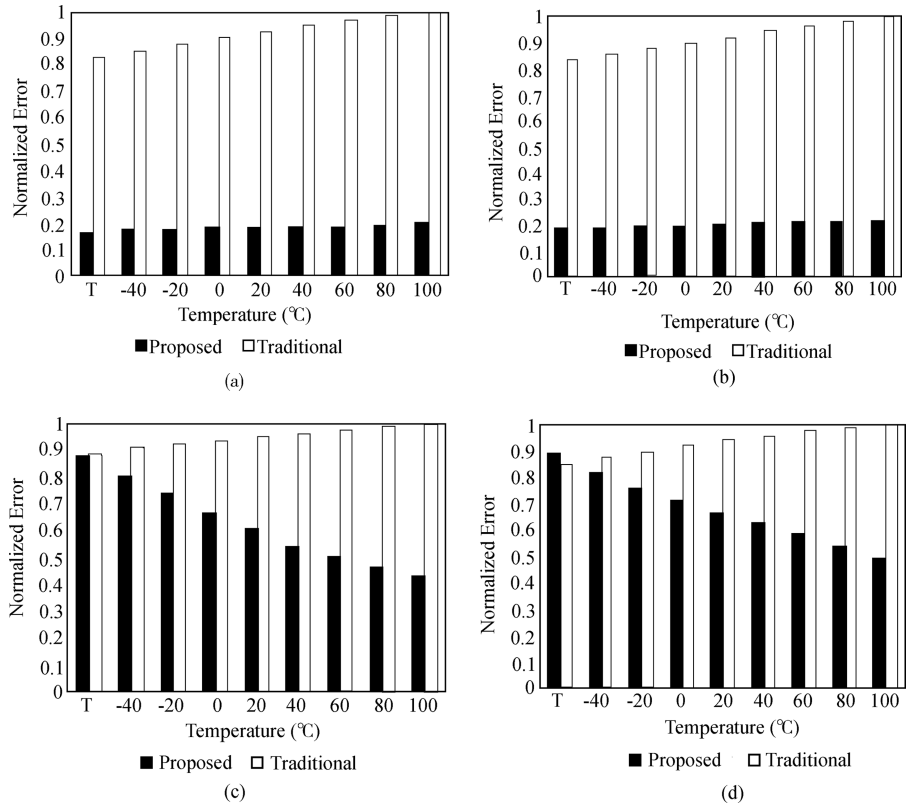

Fig. 5. Normalized error of the proposed sensor and a traditional sensor, assuming that no calibration is made: (a) For an FF process; (b) For an SS process; (c) For $0.9V_{DD}$; (d) For $1.1V_{DD}$.

Table 2. Comparison of temperature sensors.

Sensor type	Error	Power	Output	Area/Process
TV measurement sensor[9]	± 1 °C	N/A	Frequency	0.5 mm^2/1 μm
TDC sensor[7]	± 0.6 °C	1.5 μW@5 samples/s	Digit	0.09 mm^2/0.35 μm
Differential sensor[10]	± 2 °C	25 μW	Frequency	N/A/45 nm
Intel diode[2]	± 2 °C	N/A	Voltage	N/A/65 nm
AMD diode[3]	± 10 °C	10–100 μW	Voltage	N/A/90 nm
Our sensor	± 1.1 °C	0.09 μW@ 1 sample/s	Digit	0.0036 mm^2/0.13 μm

error. The error comes from two sources: the nonlinear portion of the delay-temperature curve and the discrete sampling value related to the resolution. The power consumption of Ring-oscillator-1 and Ring-oscillator-2 are 127 and 170 μW, respectively. Here, Ring-oscillator-2 consumes more power because in the cross-coupled structure the PMOS and NMOS work against each other. The power consumption of the whole sensor is about 1200 μW in active mode. If the sampling rate is limited to one sample per second, the power consumption can be minimized to less than 0.09 μW.

In Fig. 5 the temperature readout errors of the proposed and a traditional digital sensor are compared for different process and voltage corners, assuming that no calibration was done. Here, we design and simulate a traditional digital sensor using the system clock as described in Ref. [11]. The ring oscillator is the same as Ring-oscillator-1 in our sensor. The figures show the normalized errors of both sensors in different corners. The error values are normalized to the value of the tranditional sensor at 100 °C. The following conditions are shown: FF (fast PMOS, fast NMOS), SS (slow PMOS, slow NMOS), $0.9V_{DD}$, and $1.1V_{DD}$. We find that the error due to process variations is reduced to 23%, while the error due to voltage variations is reduced to 60% at high temperature. This is achieved by the compensation between the delay variations of two ring oscillators. When the process or voltage get worse (better), both two rings get slower (faster). In this way, we try to reduce the error in order to make a calibration of the sensor unnecessary, which will reduce the cost for the sensor.

A comparison of the proposed sensor with other sensors is given in Table 2. All the errors given are after calibration. The area and power consumption of the proposed sensor are smaller than for other sensors. The error of ±1.1 °C is good enough for industrial applications, as compared with Refs. [2, 3].

4. Conclusion

In this paper, we have found an innovative phenomenon of thermal independence for cascaded cross-coupled structures. A theoretical deduction is given. We proposed a temper-

ature sensor utilizing a cross-coupled ring oscillator instead of the system clock. Using this sensor, the errors caused by process and voltage sensitivities can be reduced. Higher resolution with good linearity and temperature insensitivity is realized by changing the channel widths of three inverters. Since no custom analog circuitry is used, the proposed sensor can be easily integrated into cell-based chips. The compact sensor structure also leads to a small area and a low power consumption. The sensor has been designed and post-layout simulated using TSMC13G technology. The accuracy was ±1.1 °C at a reduced process/voltage sensitivity.

Appendix: More accurate formula for T_{PLH} of the cross-coupled structure

In a more accurate way, we can reach the same conclusion for the temperature dependence of the cascaded cross-coupled structure. Due to the charge current I_{total}, the voltage on node OUT rises from zero to $V_{\mathrm{DD}}/2$ in two steps. At first, the voltage rises from zero to $-V_{\mathrm{TP}}$, while P1 is in saturation region and N2 is in linear region. We call this transition step T1. During this step, the I_{total} can be written as

$$I_{\mathrm{total1}} = \frac{1}{2}K_{\mathrm{P1}}(V_{\mathrm{DD}} + V_{\mathrm{TP}})^2 - \frac{1}{2}K_{\mathrm{N2}}\left[(V_{\mathrm{DD}} - V_{\mathrm{TN}})^2 - (V_{\mathrm{DD}} - V_{\mathrm{OUT}} - V_{\mathrm{TN}})^2\right]. \quad \text{(A1)}$$

Moreover, the current can lead to a change of the load voltage,

$$I_{\mathrm{total1}} = C_{\mathrm{L}}\frac{\mathrm{d}V_{\mathrm{OUT}}}{\mathrm{d}t}, \quad \text{(A2)}$$

where C_{L} is the load capacitance on node OUT. By calculating the integral of the current in Eq. (A1), T_1 can be derived as

$$T_1 = \frac{-2C_{\mathrm{L}}V_{\mathrm{TP}}}{K_{\mathrm{P1}}(V_{\mathrm{DD}} + V_{\mathrm{TP}})^2 - K_{\mathrm{N2}}(V_{\mathrm{DD}} - V_{\mathrm{TN}})^2}. \quad \text{(A3)}$$

In a second step, the voltage rises from $-V_{\mathrm{TP}}$ to $V_{\mathrm{DD}}/2$ with both P1 and N2 operating in the linear region. We call this transition step T_2. Similarly, we have I_{total2} as

$$I_{\mathrm{total2}} = \frac{1}{2}K_{\mathrm{P1}}\left[(V_{\mathrm{DD}} + V_{\mathrm{TP}})^2 - (V_{\mathrm{OUT}} + V_{\mathrm{TP}})^2\right] - \frac{1}{2}K_{\mathrm{N2}}\left[(V_{\mathrm{DD}} - V_{\mathrm{TN}})^2 - (V_{\mathrm{DD}} - V_{\mathrm{OUT}} - V_{\mathrm{TN}})^2\right]. \quad \text{(A4)}$$

Again, by calculating the integral of the current we get:

$$T_2 = \frac{C_{\mathrm{L}}}{\sqrt{K_{\mathrm{P1}} - K_{\mathrm{N2}}}}2a\ln\left|\frac{X+a}{X-a}\right|\Bigg|_{V_{\mathrm{out}}=-V_{\mathrm{TP}},V_{\mathrm{out}}=0.5V_{\mathrm{DD}}}, \quad \text{(A5)}$$

where,

$$X = \sqrt{K_{\mathrm{P1}} - K_{\mathrm{N2}}}\left(V_{\mathrm{out}} - \frac{K_{\mathrm{P1}}(V_{\mathrm{TP}} + V_{\mathrm{DD}}) - K_{\mathrm{N2}}V_{\mathrm{TN}}}{K_{\mathrm{P1}} - K_{\mathrm{N2}}}\right)$$

and

$$a = \sqrt{K_{\mathrm{N1}}\left[V_{\mathrm{TN}}^2 - (V_{\mathrm{DD}} - V_{\mathrm{TN}})^2\right] + \frac{[K_{\mathrm{P1}}(V_{\mathrm{DD}} + V_{\mathrm{TP}}) + K_{\mathrm{N2}}V_{\mathrm{TN}}]^2}{K_{\mathrm{P1}} - K_{\mathrm{N2}}}}.$$

Now T_{PLH} can be derived:

$$T_{\mathrm{PLH}} = T_1 + T_2. \quad \text{(A6)}$$

Like the analysis on the first-order expression, a similar deduction can be made from Eq. (A6). And by substituting the real SPICE parameters of the five mentioned technologies into Eq. (A6), the reversed temperature dependence phenomenon can be found. When W_{N2} or W_{P2} are set to zero, the terms of K_{N2} and K_{P2} become zero and the formula simplifies to Eq. (3).

For Eq. (11), we can have a more accurate expression. For the duration of OUT being charged, I_{P1} becomes smaller since its drain-source voltage is reduced, and at the same time I_{N2} becomes larger than zero. Therefore, the most critical situation happens when V_{OUT} reaches $V_{\mathrm{DD}}/2$. Using the full current expression in the linear region, we get to a similar conclusion as Eq. (11):

$$\frac{W_{\mathrm{P1}}}{W_{\mathrm{N2}}} > \frac{\mu_{\mathrm{N}}}{\mu_{\mathrm{P}}}\frac{3V_{\mathrm{DD}} - 4V_{\mathrm{TN}}}{3V_{\mathrm{DD}} + 4V_{\mathrm{TP}}}. \quad \text{(A7)}$$

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