A 10-bit 50-MS/s sample-and-hold circuit with low distortion sampling switches*

Zhu Xubin(朱旭斌)†, Ni Weining(倪卫宁), and Shi Yin(石寅)

(Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China)

Abstract: A fully-differential switched-capacitor sample-and-hold (S/H) circuit used in a 10-bit 50-MS/s pipeline analog-to-digital converter (ADC) was designed and fabricated using a 0.35-μm CMOS process. Capacitor flip-around architecture was used in the S/H circuit to lower the power consumption. In addition, a gain-boosted operational transconductance amplifier (OTA) was designed with a DC gain of 94 dB and a unit gain bandwidth of 460 MHz at a phase margin of 63 degree, which matches the S/H circuit. A novel double-side bootstrapped switch was used, improving the precision of the whole circuit. The measured results have shown that the S/H circuit reaches a spurious free dynamic range (SFDR) of 67 dB and a signal-to-noise ratio (SNR) of 62.1 dB for a 2.5 MHz input signal with 50 MS/s sampling rate. The 0.12 mm^2 S/H circuit operates from a 3.3 V supply and consumes 13.6 mW.

Key words: CMOS analog integrated circuits; sample-and-hold circuit; double-side bootstrapped switch; gain-boosted operational transconductance amplifier

DOI: 10.1088/1674-4926/30/5/055011 **EEACC:** 1265H; 1280; 2570

1. Introduction

Analog-to-digital converters (ADCs) are very important building blocks in modern signal processing and communication systems. With advances in portable electronics, low power, high resolution and high speed ADCs are becoming more necessary. The pipeline ADC is a popular choice for high-speed data conversion because of its compact size and efficient power dissipation. Most pipeline ADCs have an on-chip S/H circuit in front of the pipeline stages to buffer the input signal. The precision and speed of the S/H circuit critically limit the performance of the pipeline ADC[1].

Early works on improving the precision of the S/H circuit concentrated mainly on improving the input switch. A differential topology was used to eliminate the effect of clock feedthrough, and the bottom-plate technique was applied to cancel the dependence of the charge injection on the input signal[2]. By using the bootstrapping technique, the nonlinearity of the switch on-resistance was reduced[3, 4]. However, when conventional bootstrapping techniques are used, clock feedthrough will no longer be eliminated by a differential topology.

This paper describes the design of a 10-bit 50-MS/s S/H circuit using a 0.35-μm CMOS process. To obtain low power consumption, the flip-around architecture is used. A folded cascode configuration OTA with gain-boosting is implemented to attain large bandwidth and high DC gain. To improve the linearity of the S/H circuit, a novel double-side bootstrapped switch containing a dummy switch is proposed, which results in low distortion without introducing clock feedthrough.

2. S/H circuit topology

Two CMOS S/H circuit architectures are used widely in pipeline ADC design. Both of them are fully differential circuits. The first one is referred to as charge-transferring S/H circuit, as shown in Fig. 1(a). The differential input signal is sampled into two input sampling capacitors during the sampling phase. Only the differential charge is afterwards transferred to the feedback capacitors during the holding phase[5].

The second architecture is the flip-around S/H circuit, as shown in Fig. 1(b). No charge transferring happens in this scheme. The differential input signal is sampled into the input capacitors in the same way as in the charge-transfer architecture during the sampling phase and flips the same capacitors to the output during the holding phase.

For the charge-transferring S/H circuit, the feedback factor β, which measures the portion of the output signal being fed back to the amplifier's input, is ideally 0.5, while the ideal β of the flip-around S/H circuit is 1, neglecting parasitic capacitances.

We chose the flip-around architecture for its three advantages. The first advantage is lower power consumption. Since its β is twice as high, the flip-around S/H circuit ideally needs only 50% of the gain bandwidth (GBW) to achieve the same closed-loop bandwidth. This results in significant power savings[6]. The second advantage is lower noise. The noise level of the flip-around S/H circuit is nearly 50% lower than that of the charge-transferring S/H circuit during the sampling phase as well as the holding phase. The third advantage is that it uses the bottom-plate technique, making the charge injection signal independent of the input signal[2].

3. Operational transconductance amplifier

The circuit schematic of the amplifier utilized in the S/H circuit is shown in Fig. 2. It uses a folded cascode configuration with an NMOS input pair. The gain-boosting technique is applied to enhance the open-loop DC gain of the amplifier

* Project supported by the National High Technology Research and Development Program of China (No. 2002AA1Z1200).

† Corresponding author. Email: zhuxubin@semi.ac.cn

Received 30 October 2008, revised manuscript received 13 January 2009

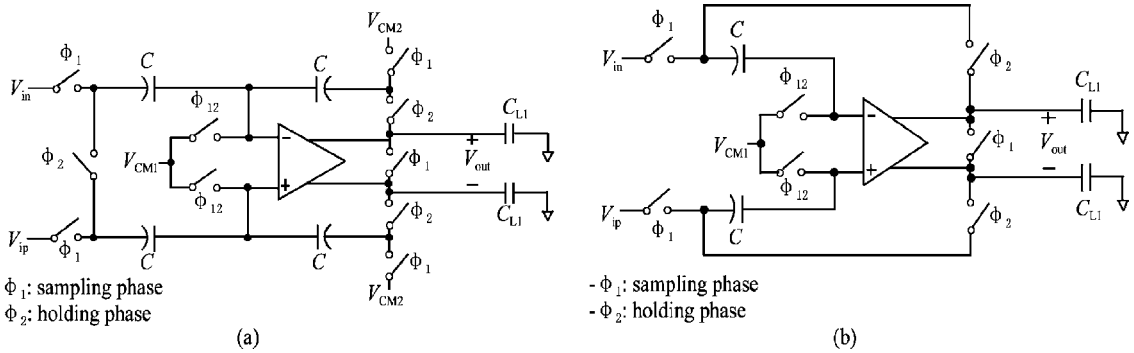

Fig. 1. (a) Charge-transferring S/H circuit; (b) Flip-around S/H circuit.

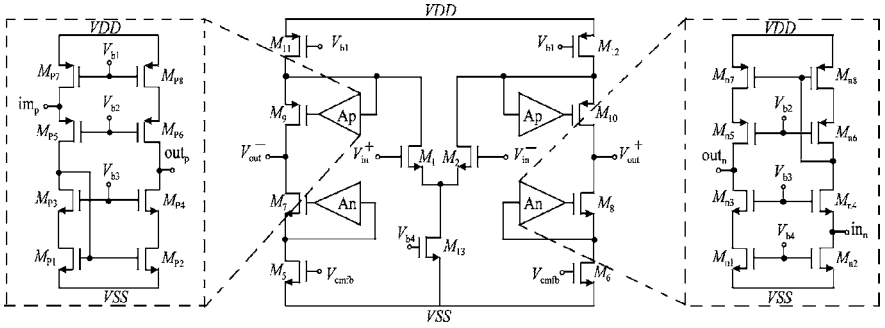

Fig. 2. Improved high-swing low-voltage folded cascode amplifier.

with complementary high-swing regulation, as shown in Fig. 2. Besides, the normalized gain frequencies of the improved gain stage are equal to those of the original gain stage.

The inputs of the regulation amplifiers are located at the source nodes of the transistors. These amplifiers operate with very low bias currents and can be constructed by transistors with almost minimum size in order to limit the reduction in GBW. Furthermore, the core amplifier and the regulation amplifiers may use the same bias circuit.

In contrast to many other regulation amplifier topologies, the output signal swing is not reduced since only a voltage of V_{ds} is required between the feedback amplifier inputs and the supply rails[7]. To attain an accurate settling behavior of the switched-capacitor (SC) gain stage, the feedback amplifiers are band limited by adding small capacitors to their outputs. The amplifier uses an SC common-mode feedback (CMFB) circuit[8], which is connected to the node V_{cmfb}.

Considering the stability of the OTA, a "safe" area for the unity-gain frequency ω_4 of the regulation amplifier is given by

$$\beta\omega_5 < \omega_4 < \omega_6, \tag{1}$$

where ω_6 is the second pole of the OTA, ω_5 is the unity-gain frequency of the core amplifier, and β is the feedback factor of the circuit[9].

The OTA is designed to satisfy Eq. (1). According to an HSPICE simulation for the slowest case, the OTA has a DC gain of 94 dB. Its GBW is estimated to be 460 MHz at a phase margin of 63 degree with a capacitive load of 2 pF. These characteristics provide enough margin for designing a 10-bit 50-MS/s S/H circuit.

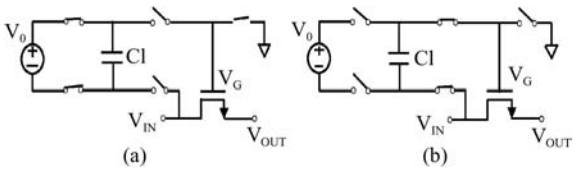

Fig. 3. Bootstrapped switch: (a) Open; (b) Closed.

4. Switches

Channel charge injection and clock feedthrough are the major sources of errors when the switch is turned off, and their effect can be limited by using the bottom-plate technique and a differential configuration.

However, there are other distortion sources inherently in the circuit configuration, mainly due to the dependency of the gate-source voltage of the switch on the input signal. This causes non-linearity of the on-resistance of the switch and may lead to issues for high-frequency high-swing input signals. For a short channel device, R_{ON} is given by

$$R_{ON} = \left(1 + \frac{V_D - V_S}{E_C L}\right)\left\{C_{ox}\mu_{eff}\frac{W}{L}\left[V_G - \frac{V_S}{2} - \frac{V_D}{2} - V_{T0} - \gamma\left(\sqrt{V_S - V_B - 2\varphi_F} - \sqrt{2\varphi_F}\right)\right]\right\}^{-1}, \tag{2}$$

where V_G, V_S, V_D, and V_B are the voltages on the transistor's gate, source, drain, and bulk terminals. From Eq. (2), we can conclude that the dominant signal-dependent terms include three parts: (1) the gate-channel voltage $V_G - (V_S + V_D) / 2$ in the denominator; (2) the threshold voltage dependency on the source-bulk voltage modeled by the square root terms in the denominator; (3) the drain-source voltage $V_D - V_S$ in the numerator.

We applied the bootstrapped switches shown in Fig. 3. This architecture was used on both sides, that is, gate-to-

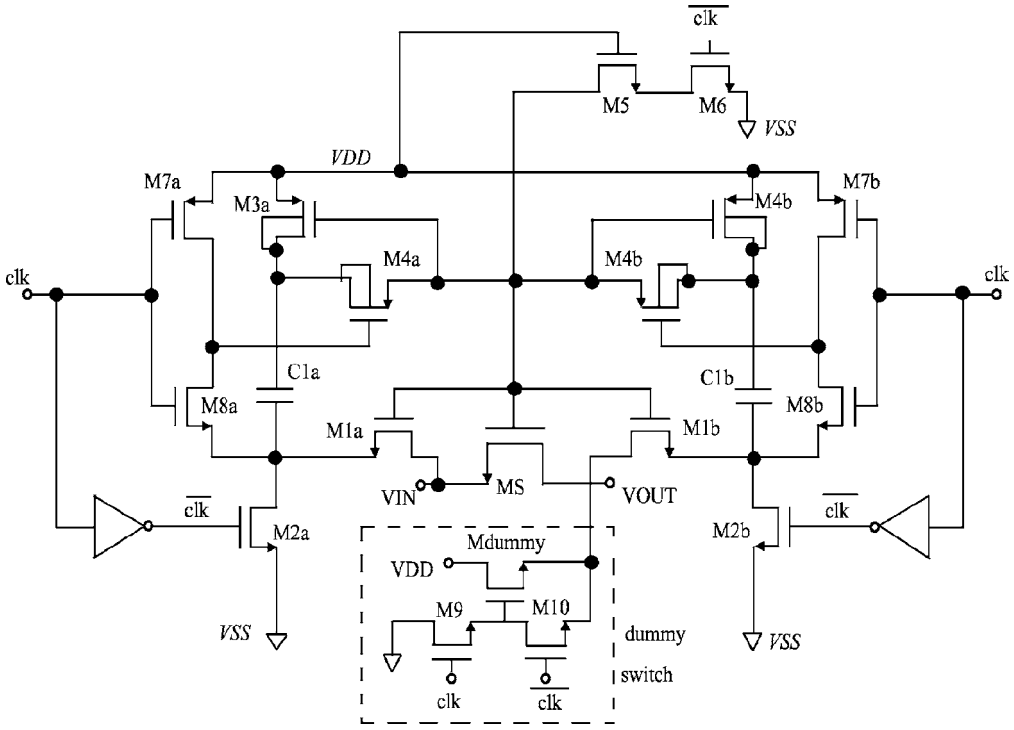

Fig. 4. Double-side bootstrapped switch.

source and gate-to-drain terminals, to ensure more linearization. This so-called double-side bootstrapped switch is shown in Fig. 4[10]. The circuit of Fig. 4 operates as follows: in the OFF mode, the main switch's (MS) gate is connected to V_{SS} through M5 and M6, while the capacitors C_{1a} and C_{1b} are being charged through M2(a,b) and M3(a,b). In the ON mode, the V_{DD}-charged capacitors will be connected simultaneously between the gate-drain and gate-source of the main switch MS through M1(a,b) and M4(a,b). Both, the gate-channel voltage ($V_G - (V_S + V_D) / 2$) and the drain–source voltage ($V_D - V_S$), are equal to V_{DD}, which improves the linearity of R_{ON} and, thus, improves the sampling switch linearity. However, there is another error source, which is introduced by the bootstrapped switch: the clock feedthrough given by

$$\Delta V = \frac{C_{GD} V_G}{C_{GD} + C_H}, \tag{3}$$

where V_G is equal to $V_{DD} + V_{IN}$ in the sampling mode. We used a dummy switch to minimize this error as shown in Fig. 4. The dummy transistor M_{dummy}, which has the same size as the MS, is always off. Switching from sampling to holding mode, the gate of the MS is changed from $V_{DD} + V_{IN}$ to ground, while the gate of M_{dummy} is changed from ground to V_{OUT}. Since V_{OUT} is equal to V_{IN}, this change leads to an exact compensation of the input-dependent clock feedthrough ($C_{GD}V_{IN} / (C_{GD} + C_H)$). The remaining input-independent clock feedthrough ($C_{GD}V_{DD} / (C_{GD} + C_H)$) can be cancelled out by using a differential topology.

The double-side bootstrapped switch containing a dummy switch was used only for the most critical switch; i.e., the sampling switch at the input level. This was done in order to minimize the power consumption and the complexity of the circuit.

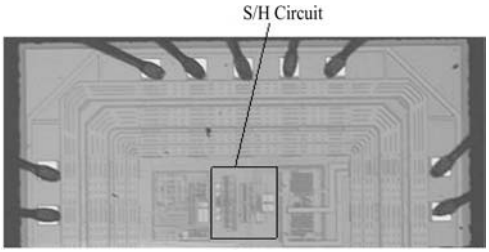

Fig. 5. Die photo of the fabricated S/H circuit.

5. Experimental results

The proposed S/H circuit was fabricated using a 0.35-μm double-poly five-metal CMOS process. The power consumption is 13.6 mW at a supply voltage of 3.3 V.

Figure 5 shows the die photomicrograph, with a total die area of 0.12 mm^2. The S/H circuit is laid out on the top of the chip. Additional circuits, such as clock generator circuit and a bandgap voltage reference, were implemented.

In the test setup, the clock signal was generated by a crystal oscillator and the sine wave input to the chip was generated by an Agilent 8648c waveform generator. The chip output signals were observed by using a Tektronix TDS30328 oscilloscope.

Figure 6 shows the output spectrum with 50 MHz sampling rate and 2.5 MHz analog input. The input range is 1.6 Vpp, and the achieved SFDR and SNR are 67 and 62.1 dB, respectively. Design results are summarized in Table 1.

6. Conclusion

A 50-MS/s 10-bit sample-and-hold amplifier in 0.35-μm CMOS has been designed and implemented. Capacitor flip-around architecture was used to lower the power consumption

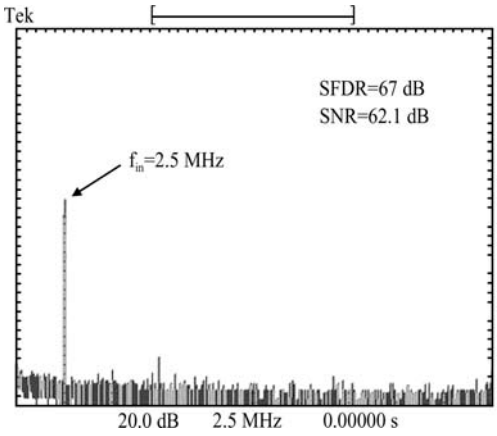

Fig. 6. Output spectrum with 50 MHz sampling rate and 2.5 MHz input sinewave.

Table 1. Measured performance.

Parameter	Value
Sampling rate	50 MS/s
Resolution	10 bits
SFDR @ 2.5 MHz	67 dB
SNR @ 2.5 MHz	62.1 dB
Input range	1.6 Vpp
Supply voltage	3.3 V
Power consumption	13.6 mW
Active area	0.12 mm^2
Process	0.35 μm CMOS

of the chip. By using the folded cascode configuration OTA and double-side bootstrapped switches, the S/H circuit reaches a high bandwidth and good linearity.

References

[1] Abo A. Design for reliabilty of low-voltage switched-capacitor circuits. PHD Thesis, University of California, Berkeley, 1999

[2] Chouia Y, El-Sankary K, Saleh A, et al. 14 b, 50 MS/s CMOS front-end sample and hold module dedicated to a pipelined ADC. IEEE Proc Int Symp Circuits and Systems, 2004, 1: 25

[3] Ali A M A, Dillon C, Sneed R, et al. A 14-bit 125 MS/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter. IEEE J Solid-State Circuits, 2006, 41: 1846

[4] Park J B, Yoo S M, Kim S W, et al. A 10-b 150-Msample/s 1.8-V 123-mW CMOS A/D converter with 400-MHz input bandwidth. IEEE J Solid-State Circuits, 2004, 39: 1335

[5] Lewis S, Gray P R. A pipelined 5-Msample/s 9-bit CMOS analog-to-digital converter. IEEE J Solid-State Circuits, 1987, SC-22: 954

[6] Yang W, Kelly D, Mehr I, et al. A 3-V 340 mW 14-b 75 Msample/s CMOS ADC with 85-dB SFDR at Nyquist input. IEEE J Solid-State Circuit, 2001, 36: 1931

[7] Sumanen L, Waltari M, Halonen K A I. A 10-bit 200-MS/s CMOS parallel pipeline A/D converter. IEEE J Solid-State Circuit, 2001, 36: 1048

[8] Senderowicz D, Dreyer S F, Huggins J H, et al. A family of differential NMOS analog circuits for a PCM codec filter chip. IEEE J Solid-State Circuits, 1982,17: 1014

[9] Bult K, Geelen G J G M. A fast-settling CMOS Op Amp for SC circuits with 90-dB dc gain. IEEE J Solid-State Circuits, 1990, 25: 1379

[10] Waltari M, Sumanen L, Korhonen T, et al. A selfcalibrated pipeline ADC with 200 MHz IF-sampling frontend. Digest of Technical Papers of IEEE International Solid-State Circuits Conference, 2002, 2: 250