Design of a 40-GHz LNA in 0.13-μm SiGe BiCMOS

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Abstract: A low-noise amplifier (LNA) operated at 40 GHz is designed. An improved cascode configuration is proposed and the design of matching networks is presented. Short-circuited coplanar waveguides (CPWs) were used as inductors to achieve a high Q-factor. The circuit was fabricated in a 0.13-μm SiGe BiCMOS technology with a transistor transit frequency f_T of 103 GHz. The chip area is 0.21 mm^2. The LNA has one cascode stage with a –3 dB bandwidth from 34 to 44 GHz. At 40 GHz, the measured gain is 8.6 dB; the input return loss, S_{11}, is –16.2 dB; and the simulated noise figure is 5 dB. The circuit draws a current of only 3 mA from a 2.5 V supply.

Key words: low-noise amplifier; BiCMOS; millimeter wave; coplanar waveguide; matching network
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1. Introduction

As wireless communication becomes more popular, the application frequency is moving towards a higher frequency range due to the spectrum congestion. The GHz frequency band has the advantages of wide bandwidth and small circuit size[1]. Since the low-noise amplifier (LNA) is the most important component for RF front-end receivers, many reports have been presented to investigate and demonstrate millimeter wave applications[1–8].

In the past, most millimeter wave LNAs were fabricated with the GaAs process because of its high performance and semi-insulating substrate. With the development of technology, LNAs are more often fabricated in silicon-based processes, such as SiGe BiCMOS or pure CMOS, due to its advantages of lower cost and higher integration degree.

On lossy silicon substrates, integrated passive devices of high quality are very important for millimeter wave applications. Since inductors are the key components for LNAs, it is necessary to improve their quality and precision.

This paper presents the design of the matching network of a 40-GHz LNA based on inductors formed by coplanar waveguides. The LNA is simulated and fabricated using IBM 0.13-μm SiGe BiCMOS technology. The f_T of the transistors is 103 GHz. The VBIC model, which overcomes a number of long recognized deficiencies in the standard Gummel-Poon model, is used. Since the LNA operates at the frequency limit of the process for amplifier design, the device model must be accurate. Moreover, the losses and parasitic effects should be carefully calculated with the help of circuit and full-wave electromagnetic simulators.

2. Device model and circuit structure

The small-signal, high-frequency equivalent circuit model of a bipolar transistor is shown in Fig. 1. The input capacitance C_π is composed of the base-charging capacitance and the emitter-base depletion layer capacitance[9]; C_{cs} is the collector-substrate capacitance, which is several tens of femto-Farads in SiGe process. These parasitic capacitances cannot be ignored at 40 GHz.

Although many different topologies have been proposed to implement LNAs, only two topologies are commonly used in SiGe processes, namely, the inductively-degenerated common-emitter stage and the Cascode (common-emitter-common–base) topology. In the inductively-degenerated common-emitter LNA, an emitter inductor L_e is used to generate the real part needed to match the LNA input to the preceding antenna or filter. In addition, a base inductor L_b is used to cancel the equivalent capacitance of the circuit. It can match the input without resistance and reduce the noise figure. For the small-signal model shown in Fig. 1, the input impedance of the inductively-degenerated common-emitter LNA is given by

$$\begin{aligned} Z_{in} = {} & r_b + r_\pi \left(\frac{\omega_T}{\omega\beta_0}\right)^2 + \omega_T L_e \\ & + j[\omega + \omega_\beta \beta(\omega)]L_e + j\omega L_b - j\frac{1}{\omega C_\pi}, \end{aligned} \tag{1}$$

where β_0 is the small signal current gain of the transistor.

$$\omega_\beta \approx \frac{1}{r_\pi C_\pi} \tag{2}$$

$$\beta(\omega) = \frac{\beta_0}{1 + j\omega/\omega_\beta} \tag{3}$$

$$\omega_T \approx \omega_\beta \beta_0 \approx \beta(\omega)\omega. \tag{4}$$

As the frequency increases, the capacitive part $-j\frac{1}{\omega C_\pi}$ in Eq. (1) decreases, and the value of L_b should be reduced.

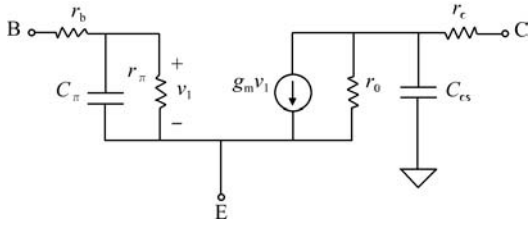

Fig. 1. Small-signal equivalent model of a bipolar transistor.

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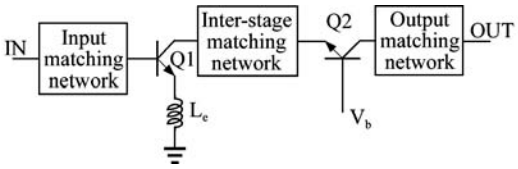

Fig. 2. Structure diagram of a 40-GHz LNA.

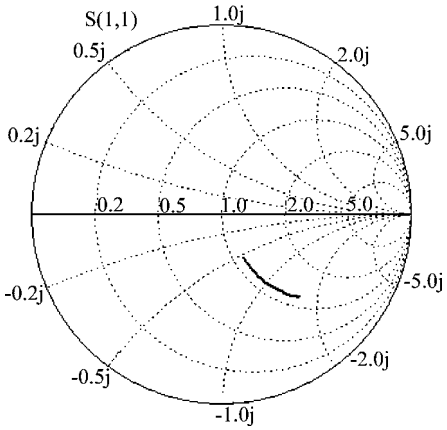

Fig. 3. Smith chart of simulated S_{11} from 20 to 60 GHz.

A cascode LNA is a common-emitter–common-base amplifier, and the transistor Q2 drastically reduces the Miller effect by ensuring a low impedance at the collector of the amplifying transistor Q1. In addition, the cascode improves the reverse isolation and increases the stability. The total noise figure of a cascode LNA is[10]

$$\mathrm{NF} = \mathrm{NF}_1 + \frac{\mathrm{NF}_2 - 1}{G_{\mathrm{A1}}}, \tag{5}$$

where NF_1 and G_{A1} are the noise figure and the gain of the first stage, respectively, and NF_2 is the noise figure of the second stage. Obviously, NF_1 and G_{A1} are the main factors for the total noise figure. If a proper matching network is designed between two stages, it can improve G_{A1} and reduce the noise of the whole circuit effectively.

Based on the discussion above, a general structure for an LNA is proposed in Fig. 2.

3. Circuit design

3.1. Matching networks

Using the design kit of IBM 0.13-μm SiGe BiCMOS process, the S-parameters of a single transistor with a proper bias are simulated in a range of 20 to 60 GHz. Figure 3 shows S_{11} plotted in a Smith chart.

As seen from Fig. 3, the real part of the input impedance is very close to 50 Ω for a frequency between 20 and 60 GHz. When using emitter-inductive-degeneration, L_e is very small and it can be neglected in the circuit. Therefore, the configuration of the circuit is simplified.

The input matching network is very important in LNA. It determines the gain and the noise of the first stage, which will affect the performance of the whole circuit. In most cases, the input matching network can not get both maximum gain and minimum noise figure simultaneously. According to its definition, the available power gain is

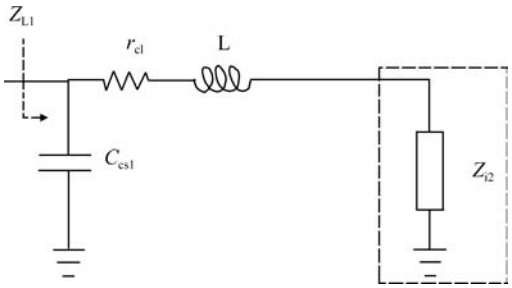

Fig. 4. Part of circuit with internal matching network.

$$G_{\mathrm{A}} = \frac{|S_{21}|^2 (1 - |\Gamma_{\mathrm{s}}|^2)}{\left(1 - \left|\dfrac{S_{22} - (\boldsymbol{\Delta})\Gamma_{\mathrm{s}}}{1 - S_{11}\Gamma_{\mathrm{s}}}\right|^2\right)|1 - S_{11}\Gamma_{\mathrm{s}}|^2}, \tag{6}$$

where $\boldsymbol{\Delta} = s_{11}s_{22} - s_{12}s_{21}$, and Γ_{s} is the voltage reflection coefficient at the source. The definition of noise figure is given by

$$\mathrm{NF} = \mathrm{NF}_{\min} + \frac{4r_{\mathrm{n}}\left|\Gamma_{\mathrm{s}} - \Gamma_{\mathrm{opt}}\right|^2}{(1 - |\Gamma_{\mathrm{s}}|^2)\left|1 + \Gamma_{\mathrm{opt}}\right|^2}, \tag{7}$$

where r_{n} is the normalized noise resistance, and Γ_{opt} is the optimal source reflection coefficient, which allows the noise figure to reach the minimum.

From Eqs. (6) and (7), both G_{A} and NF are functions of Γ. Thus, for the first stage, a series of constant gain circles and constant noise figure circles can be drawn in the Smith chart at 40 GHz. Considering that the noise is more important than the gain in an LNA, we make trade-offs in order to achieve a minimum NF and get a matching network composed of one series capacitance with a shunt inductor. The topology of the matching network is used not only as the input matching network but also as the DC bias network, where the series capacitance C can be reused as the DC block and the inductance L can damp the RF signal to DC.

If there is no network between the two stages, the circuit is a cascode configuration and the input impedance of the second stage (common-base) is low; thus, the gain of the first stage is also low. To improve the gain and to reduce noise, an inductance L can be added between the two stages, according to the small-signal equivalent model. The simplified part of a circuit with internal matching network is shown in Fig. 4.

In Fig. 4, Z_{L1} is the load impedance of the first stage and Z_{i2} is the input impedance of the second stage.

$$Z_{\mathrm{i2}} = \frac{1}{\mathrm{j}\omega C_\pi} // \frac{r_\pi}{1 + g_{\mathrm{m}} r_\pi} \approx \frac{1}{\mathrm{j}\omega C_\pi} // \frac{1}{g_{\mathrm{m}}}, \tag{8}$$

$$Z_{\mathrm{L1}} = \frac{1}{\mathrm{j}\omega C_{\mathrm{cs1}}} // \left(r_{\mathrm{c1}} + \mathrm{j}\omega L + Z_{\mathrm{i2}}\right). \tag{9}$$

According to Eq. (9), the load impedance of the first stage is improved by adding the inductance L. Therefore, the gain of the first stage is increased and NF is reduced, as derived from Eq. (5).

The output matching network is used to transform the system termination to the required conjugate-matched source,

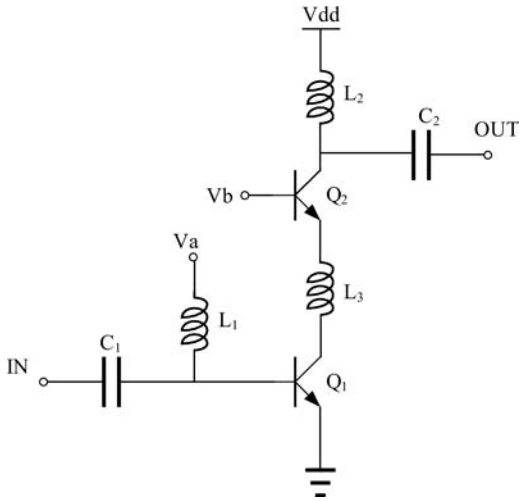

Fig. 5. Simplified schematic of the 40-GHz LNA.

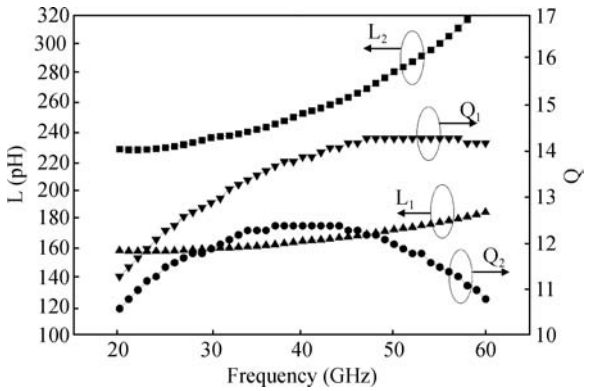

Fig. 6. Simulated inductance values and Q-factors.

so that the load can get as much power from the circuit as possible.

Connecting the designed input matching network and the interstage matching network to the circuit, then calculating the resulting output reflection coefficient Γ_{out} and transforming the actual system load termination to the complex conjugate of this new Γ_{out}, we can write Γ_{L} as follows:

$$\Gamma_{\text{L}} = \Gamma_{\text{OUT}}{}^{*} = \left(S_{22} + \frac{S_{21}S_{12}\Gamma_{\text{s}}}{1 - S_{11}\Gamma_{\text{s}}}\right)^{*}. \tag{10}$$

By using the Smith chart, the topology of the output matching network can be matched to the input network. The finally designed circuit is shown in Fig. 5.

3.2. Inductors

For most of the millimeter-wave IC designs, the adopted inductors are either microstrip transmission lines (MTLs) or coplanar waveguides (CPW). An MTL has a ground plane directly below the signal line in order to shield the electric and magnetic fields from penetrating into the substrate, and thus to reduce the losses. Since the inductance value of L_3 is not very small and the Q-factor of it has little impact on the circuit performance, a spiral inductor from the process design library is used to implement L_3. This inductor has only one turn over a trench isolation ground plane in order to maximize the self-resonant frequency.

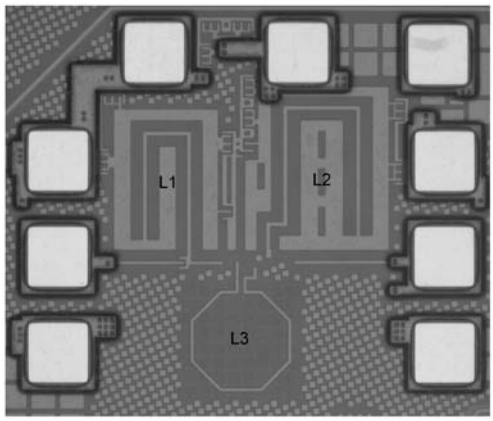

Fig. 7. Die photograph.

Compared to the microstrip line, the CPW inductor has a better quality factor and small parasitic capacitances in the millimeter-wave frequency range, which result in a much higher first resonant frequency. In the proposed design, short-circuited coplanar waveguides, which are equivalent to inductances, are used as inductors L_1 and L_2 in the matching networks.

In order to build up a high-Q inductor, the series resistance must be low, and the shunt parasitic capacitance must be small. Because of its high conductivity, a top metal is used to build up the CPW inductors. Moreover, the skin effect causes the series resistance to increase at high frequencies. By using the full-wave electromagnetic simulator HFSS, an optimum line width of 4 μm is derived. Figure 6 shows the simulated results of two CPW inductors.

In matching networks, L_1 is 165 pH and L_2 is 250 pH at a frequency of 40 GHz. The impedance Z_{11} can be extracted from the electromagnetic simulation. The inductance and Q-factor are calculated as

$$L = \frac{\text{Im}(Z_{11})}{\omega}, \tag{11}$$

$$Q = \frac{\text{Im}(Z_{11})}{\text{Re}(Z_{11})}. \tag{12}$$

4. Layout and results

The LNA has been designed and fabricated in IBM 0.13-μm SiGe BiCMOS technology. Figure 7 shows the micrograph of the die, which has a size of 0.21 mm^2. It can be seen that the die is dominated by the passive components. Two inductors, L_1 and L_2, are CPW inductors and are carefully placed, in order to reduce their dimensions. A top metal is used to realize the air bridges, which cross over the signal line at the bend corner. L_3 is a spiral transmission line inductor, which follows the model provided by the foundry. A trench isolation ground shield is used beneath the inductor to reduce substrate coupling and increase the self-resonant frequency. Several on-chip capacitances with different values are used to provide supply decoupling. Several substrate contacts, placed around the transistors, were used to minimize the emitter inductance. ESD diodes were placed between I/O pad and ground pad to protect the circuit.

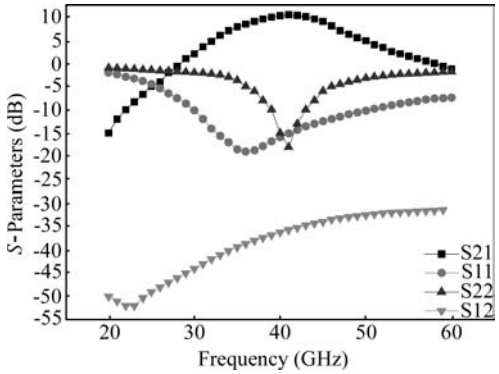

Fig. 8. Post-simulated S-parameters of the LNA.

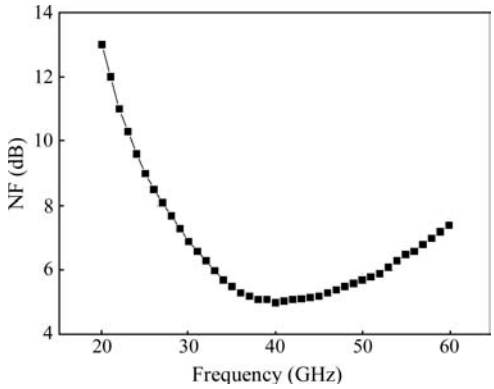

Fig. 9. Post-simulated NF of the LNA.

The parasitic parameters of the layout were extracted and simulated by Cadence Spectre-RF. Figure 8 shows the post-simulated S-parameters. S_{21} is 10.2 dB at 40 GHz, the −3 dB bandwidth ranges from 34 to 44 GHz, and the input return loss S_{11} is less than −15 dB from 33 to 41 GHz. As shown in Fig. 9, NF is 5 dB at 40 GHz.

The S-parameters of the LNA were measured using an Agilent vector network analyzer E8363B, which can measure the maximum frequency at 40 GHz. The measured results are shown in Fig. 10. The LNA has a flat gain and S_{21} is 8.6 dB at 40 GHz, which is smaller than the simulated result of 10.2 dB. S_{11} is −16.2 dB and S_{22} is −14.6 dB at 40 GHz. S_{12} is less than −35 dB in the frequency range from 20 to 40 GHz. The NF is not measured due to limitations in the test conditions. The DC current is only 3 mA when using a 2.5 V supply.

5. Conclusion

A millimeter-wave LNA based on CPW inductors, simulated and then implemented in a 0.13-μm SiGe BiCMOS technology, has been presented. The configuration of the LNA has been investigated based on a device model and an improved cascode structure is proposed, which has a series

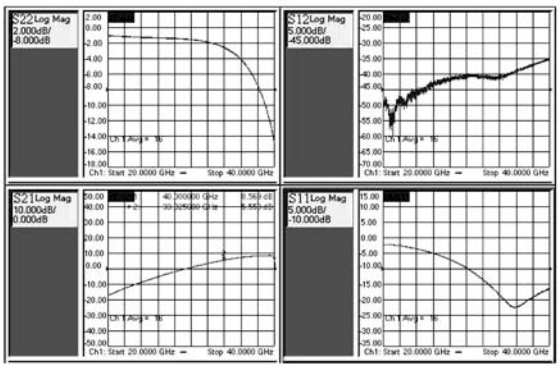

Fig. 10. Measured S-parameters of the 40-GHz LNA.

inductor placed between two transistors. The proposed topology can improve the gain effectively. The matching networks have been carefully designed and the CPW inductors were simulated by a full-wave electromagnetic tool.

The chip has a small area and low power consumption. The measured results agree well with the simulated results and show that the center frequency of this LNA is at 40 GHz. In addition, the experimental results imply that the CPW inductors were accurately designed and the proposed configuration is fit for millimeter-wave LNAs.

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