Temperature dependence of charge sharing and MBU sensitivity induced by a heavy ion*

Liu Biwei(刘必慰)†, Chen Shuming(陈书明), and Liang Bin(梁斌)

(School of Computer, National University of Defense Technology, Changsha 410073, China)

Abstract: The temperature dependence of charge sharing in a 130 nm CMOS technology has been investigated over a temperature range of 200 to 420 K. Device simulation results show that the charge sharing collection increases by 66%–325% when the temperature rises. The LET_{th} of a MBU in two SRAM cells and one DICE cell is also quantified. Besides charge sharing, the circuit response's temperature dependence also has a significant influence on the LET_{th}.

Key words: charge sharing; temperature dependence; parasitic bipolar; MBU
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1. Introduction

With the feature size of integrated circuits continuously scaling down, charge sharing has become a major single event effect (SEE) issue for deep-submicron technologies due to the reduced nodal charge and the reduced spacing between devices. It has been reported that one ion hit can lead to a multiple bit upset (MBU) in DRAMs and SRAMs by lateral diffusion[1, 2]. Also radiation hardening by design (RHBD) storage cells (HIT cell, DICE cell, *et al.*) are found to be upset by single ion strikes[3–5], which is also due to diffusion induced charge sharing. Except diffusion, the bipolar effect may also induce charge sharing between adjacent devices[6–8]. The study of charge sharing in a 130 nm technology shows that the PMOS device shows a high parasitic bipolar amplification compared to the NMOS device due to a voltage perturbation in the n-well during the charge collection process[9]. And the well contacts can effectively migrate the charge sharing because of the bipolar effect[9–11]. Recently, Amusan[12] reported that the DICE cells upset LET_{th} and the cross-section is heavily dependent on the direction of the incident ions in 90 nm CMOS. Gasiot[13] studied the MBU's dependence on well engineering, and found that the triple well will enhance the bipolar effect in a P-well.

On the other hand, the on-board temperature may range widely from less than 0 to higher than 100 °C in a space environment, which causes the temperature to be an important factor in radiation hardening. Many works have demonstrated that SEE is strongly dependent on temperature. Heavy ion tests and TCAD simulations show that the single event latch-up (SEL) threshold LET varies significantly when the temperature increases[14]. Single event upset (SEU) test results for Harris 64 and 256 K RHD1 SOI SRAMs showed that SEU LET_{th} decreases when the temperature increases from 25 to 125 °C, due to the increasing bipolar gain of the SOI transistors[15]. Truyen[16] found that, although the PN charge collection is highly influenced by the temperature, the temperature has a negligible effect on the SEU sensitivity in the range from 218 to 418 K. Guo, Laird, and Chen[17–19] all reported that temperature has an important effect on a single event transient (SET).

However, to our best knowledge, there is still no study, which has involved the temperature effect on charge sharing. In this paper, three dimension device simulations are performed in the temperature range of 200 to 420 K using a 130 nm CMOS technology. The impact of the temperature on both the charge sharing collected and the upset sensitivity in multiple SRAM cells and DICE cell are evaluated. Simulation results will be discussed to explain the charge sharing dependency on the temperature. This paper will specify the relative contributions of diffusion, the bipolar effect, and the circuit response versus the temperature.

2. Experimental setup

The Sentaurus TCAD vA-2007.12-SP1 from Synopsys was adopted in our work to perform the structure building and device simulation. A three-dimension device model was utilized. The device structure to the simulate charge sharing between two PMOS is presented in Fig. 1. The transistor size is $W_p : L_P$ = 800 nm : 130 nm. The distance between the pair of devices is 0.3 μm. A well contact band is placed near the two transistors within a distance of 0.6 μm. Between the two transistors, STI is used to separate them. The junction depth is about 0.15 μm. Between the channel and the source/drain, a lightly doped drain–source (LDD) is inserted. The parameters of the NMOS device in the simulation are similar with those

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† Corresponding author. Email: wwwkeke@163.com

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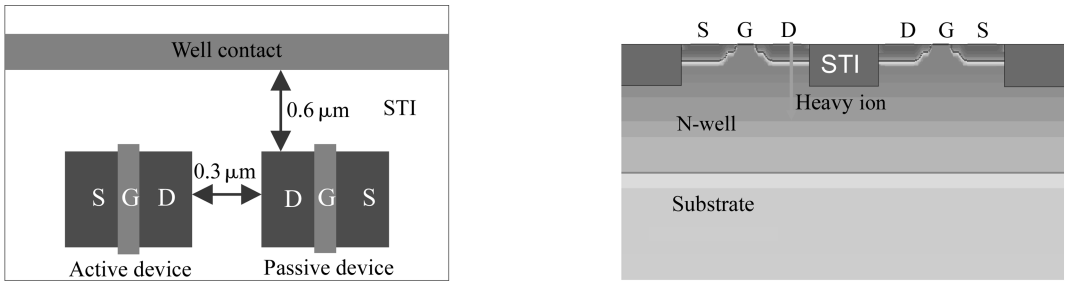

Fig. 1. Device structure of two PMOS for charge sharing simulation.

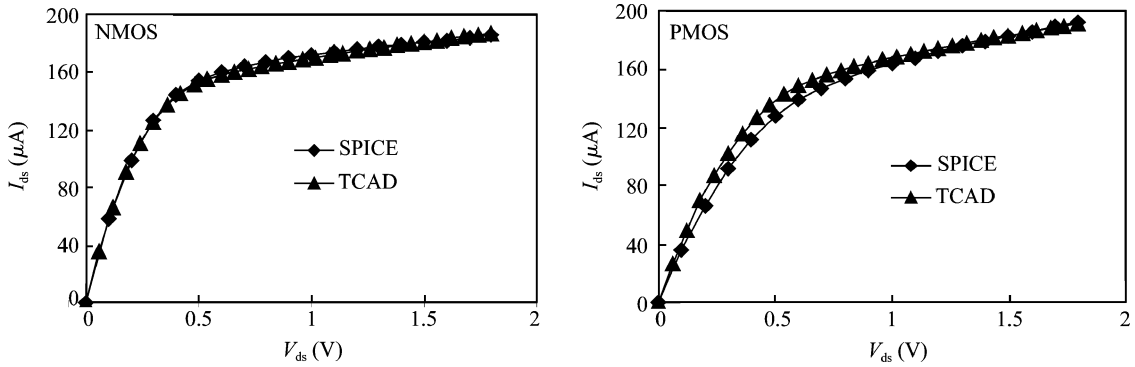

Fig. 2. Calibration of I_{ds}–V_{ds} of the device model with SPICE.

in the PMOS device model, except that W_n : L_n = 300 nm : 130 nm. The supply voltage is set to be 1.2 V.

The twin well process was used in our simulation. A single mask was used and a P-well was put everywhere there is no N-well. The NMOS transistor was generated in an implanted P-well, while the PMOS transistor was generated in an implanted N-well with a well depth of about 0.9 μm. The three-dimensional model was calibrated to SMIC's 0.13 μm Logic 1P8M Salicide Process used in China by the process simulation and an inverse modeling approach, in the 200–420 K range. The *I*–*V* characteristics of the device model and by using SPICE are presented in Fig. 2. They agree with each other very well. In the 3-D device model, the thickness of the gate oxide is set according to the SPICE model, so that the gate capacitance agrees with real value. The areas of the source and the drain of the 3-D NMOS model are set according to the layout of the standard cell, so that the junction capacitance between the drain/source and the bulk agrees with value found in real devices.

Heavy ion striking is simulated with an electron–hole pair column with its trace as its axis. The ion used in the simulation has an LET of 40 MeV·cm^2/mg. The LET value is kept constant along the heavy ion's track. The length and radius of the ion track is 5 and 0.1 μm, respectively. We assume the ion strikes at the center of the drain to the left of the transistor. The ion strikes orthogonal to the surface of the structure; hence, angular effects are not discussed in this paper. The temperature ranges from 200 to 420 K.

In the following discussion, we use the terms defined in Ref. [9], i.e., the device that was hit directly by the ion is called the active device, while the adjacent device is called the passive device.

All simulations are conducted using the YINHE computing cluster with a CPU frequency of 3.0 GHz in the National University of Defense Technology in China. The whole device model has a size of $6 \times 6 \times 6$ μm^3, and the device model contains about 150 000 to 210 000 grid points. The average duration of the 3-D simulation was two days using eight threads.

The following physical models are used: (1) Fermi-Dirac statistics, (2) band-gap narrowing effect, (3) doping dependent SRH recombination and Auger recombination, (4) temperature, doping, electric field, and carrier-carrier-scattering impacts on the mobility, and (5) incident heavy ions were modeled using a Gaussian radial profile with a characteristic 1/e radius of 0.1 μm and a Gaussian temporal profile with a characteristic decay time of 0.25 ps. A hydrodynamic model is used for the carrier transport. Unless otherwise specified, the default models and parameters provided by Sentaurus TCAD vA-2007.12- SP1 are used.

In the circuit domain, the BSIM3V3 compact model is used. Both the NMOS and PMOS transistors have a minimum channel length of L = 130 nm, a width of W = 0.3 μm for NMOS and of W = 0.8 μm for the PMOS. The other important dimensions (such as the source/drain area, the P-well contact width, the distance from the P-well contact to the active area, etc.) are set according to the layout design rules provided by SMIC.

3. Temperature dependence of charge collection

3.1. Current pulse shape variation versus temperature

The temperature dependence of transient currents has

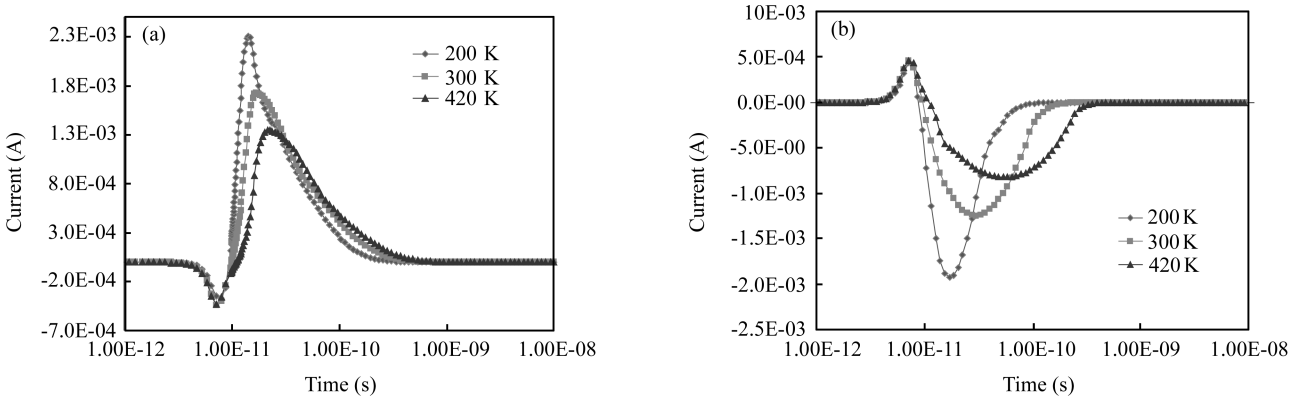

Fig. 3. Current shape at different temperatures: (a) Current shape in a passive NMOS; (b) Current shape in a passive PMOS.

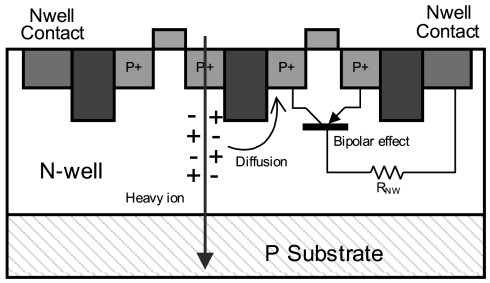

Fig. 4. Two mechanisms of charge sharing. One is diffusion and the other is the bipolar effect.

been investigated, assuming that heavy-ions strike at the center of the reverse biased drain. In Fig. 3, the drain current of a NMOS and a PMOS is plotted as a function of time at three temperatures when the device is struck by a 40 MeV·cm^2/mg heavy ion. The temperature plays a significant role in the shape of transient currents. When the temperature increases from 200 to 420 K, the peak value of the drain current decreases from 2.3 to 1.3 mA for a NMOS and from 2.0 to 0.8 mA for a PMOS. We define the duration as the time from the start of current pulse to the time it first reaches 1×10^{-6} A. Unlike the peak value, the duration of the transient current increases when the temperature increases. It is shown that the drain current pulse duration increases from 383 to 962 ps for NMOS and from 123 to 405 ps for PMOS when the temperature increases from 200 to 420 K.

It has been reported that charge sharing for devices in different wells is not prominent[9]. The reason is that charge sharing for devices in different wells needs the majority carriers in one kind of well to diffuse across the well boundary and become minority carriers in another kind of well. But the build-in electric field at the well boundary is opposed to this kind of diffusion. Our simulations verified this conclusion. The charge sharing in different wells is smaller than 10% in the same well, irrespective if the NMOS is active and the PMOS is active. So, in the following, we will only discuss charge sharing in the same wells.

3.2. Charge sharing collection variation versus temperature

There are two kinds of charge sharing mechanisms, as Figure 4 shows. One is diffusion. The charges on the ion track at the active device are transported to the passive device and collected by the electrical field in the reverse biased PN junction. The other is bipolar amplification. Charge on the ion track will make the drain/well junction or the well/substrate junction collapse, and will result in the electric potential of the body to be disturbed. The parasitic bipolar transistor will turn on and induce a bipolar current.

It is important to distinguish the temperature dependency of each mechanism. Two groups of 3-D TCAD simulations are conducted in the temperature range of 200 to 420 K. In one group, the normal transistor is simulated. In the other group, the source junction (emitter of the lateral parasitic bipolar transistor) of the transistor is physically removed (only a PN junction); thus, only diffusion is left. Thus, no minority carriers are injected from the source.

Figure 5 shows the amount of charge collected by the passive device versus temperature for a spacing from the active device of 0.3 μm. It is obvious that the temperature strongly influences the charge sharing. For a NMOS without a source, the charge sharing collected at the passive device increases by almost 66% (from 67.7 to 112.1 fC) when the temperature increases from 200 to 420 K. For a PMOS without a source, the charge sharing on the passive device also increases from 3.13 to 13.3 fC. The charge sharing in a PMOS without a source is much smaller than that in a NMOS. One reason is the difference of the diffusion constant D. A PMOS collects holes while a NMOS collects electrons. The diffusion constant D for holes is nearly 1/3 that of electrons. The other reason is the shunt effect between multiple junctions. Because the N-well/Substrate is also reverse biased, a large amount of charge on the ion track will be collected by the N-well/Substrate junction. Thus, the charge that diffuses to the passive device decrease greatly.

Similarly, in the transistors with a source, the charge sharing also increases significantly when the temperature is rising, as shown in Fig. 5(b). For an NMOS, the charge sharing collected at the passive device increases from 79.5 to 138.6 fC when the temperature increases from 200 to 420 K; in increase of almost 74%. For a PMOS with a source, the charge sharing on the passive device also increases from 45.0 to 134.1

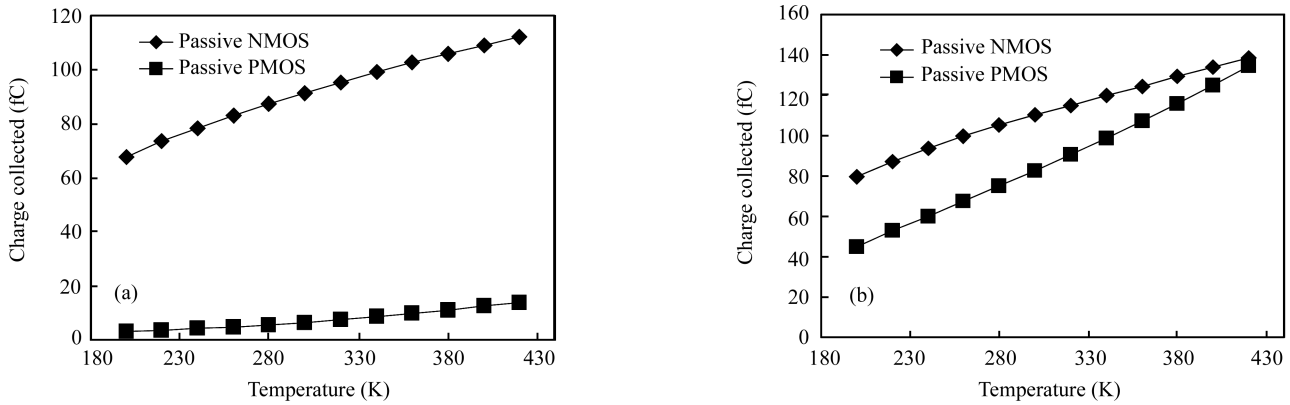

Fig. 5. Charge sharing collection on the passive device at different temperatures: (a) Device without source; (b) Device with source.

fC, i.e., by almost 168%.

The charge collection in a NMOS with a source increases by about 20% compared to a NMOS without a source. The increase is due to the bipolar effect, which is relatively small. So, in a NMOS the diffusion is the main mechanism. However, the bipolar effect is dominant in a PMOS. When an ion hits, it penetrates not only into the drain and the N-well but also into the substrate. The N-well potential is disturbed both by the drain and the substrate. So, the bipolar current is more significant in a PMOS than in a NMOS. The charge collection in a PMOS with a source increases about 10 times comparing to a PMOS without a source, as Figures 4 and 5 show.

4. Discussion

It is surprising that in our experiments the charge sharing on the passive device increases with temperature, because it have been reported that the charge collection decreases with temperature in a single device[16]. So, we suppose that there should be some difference between charge sharing and the single device charge, which is collected. In this section, we will discuss the factors, which may affect the temperature dependency of the charge sharing.

4.1. Temperature dependence of charge generation

The charge deposited increases as the temperature rises because of band-gap narrowing. The band-gap narrowing of silicon is modeled in Sentaurus TCAD as:

$$E_{\mathrm{g}} = E_{\mathrm{g}}(0) - \alpha T^2/(T+\beta), \tag{1}$$

where T is the absolute temperature, $E_{\mathrm{g}}(0)$ is the band-gap energy at 0 K, and α and β are material parameters. The average energy per ionized electron-hole pair in silicon is:

$$\varepsilon = 2.2E_{\mathrm{g}}(T) + 0.96E_{\mathrm{g}}^{1.5}(T)\exp[0.75E_{\mathrm{g}}(T)/T]. \tag{2}$$

According to Eqs. (1) and (2), the charge deposition variation as a function of the temperature increase from 200 to 420 K can be estimated. The average energy needed to ionize one electron-hole pair in silicon decreases from 3.70 to 3.50 eV, i.e., by roughly 5%. The increment deposited charge is relatively small. So, the temperature dependence of the electron–hole pair generation may not affect the charge sharing significantly.

4.2. Temperature dependence in devices without a source

In a NMOS, the charge sharing mainly depends on the diffusion of minority carriers. The minority carrier concentration is mainly decided by the diffusion constant D. With a large D, the charge will diffuse to the passive device quickly. D can be described using Einstein's relationship as:

$$D = \mu kT/q, \tag{3}$$

where μ is the carrier mobility, T is the temperature, and k and q are constants. μ also depends on the temperature. When the temperature rises, the lattice scattering will increase, which causes the mobility decrease. The relationship can be presented as

$$\mu = \mu_0\left(\frac{T}{T_0}\right)^{-\xi} \quad . \tag{4}$$

For electrons, ξ usually is 2.5, and for hole ξ usually is 2.2. So, the temperature dependence of D for electrons is given by $T^{-1.5}$, while for holes it is given by $T^{-1.2}$. However, the charge collection is increased. So, the temperature dependency of the charge sharing can not be explained by D.

Note that the charge sharing on the passive device is not independent. It is heavily influenced by the charge collection on the active device. Only the charge escaping from the active device may diffuse to the passive device, which can be expressed as

$$Q_{\mathrm{passive}} \propto Q_{\mathrm{total}} - Q_{\mathrm{active}}.$$

So, charge collected on the passive device will have a reverse trend as compared to charge collection on the active device.

In the active device, the funnel assistant drift is the main mechanism of charge collection. Drift is dependent on the mobility μ. By Eq. (4), we know μ decreases when the temperature rising, which will decrease charge collection on the active device. By Eq. (3), we know μ decreases faster than D. Although the diffusion effect gets weak, the charge that

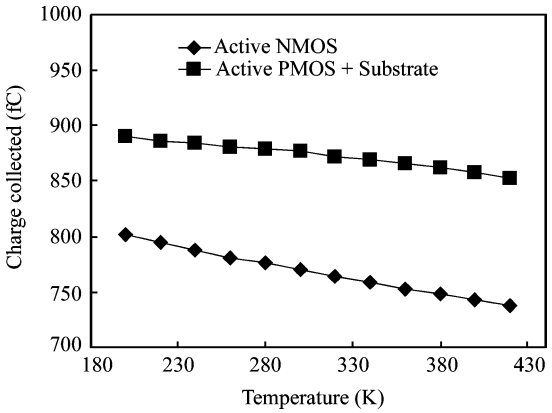

Fig. 6. Charge collection on the active device without a source.

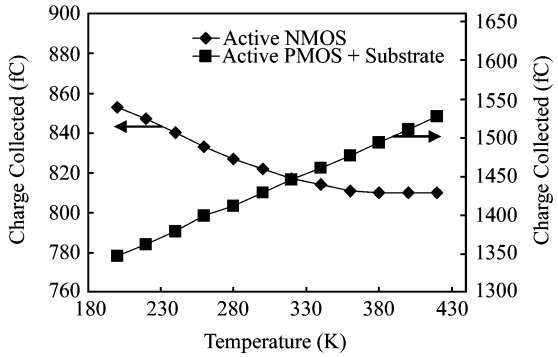

Fig. 7. Charge collection on the active device with a source.

escapes from the collection process by the active device still rises with temperature.

The decrease of the charge collection on the active device is shown in Fig. 6. When the temperature increases, the collected charge decreases from 802 to 738 pC for an NMOS. For a PMOS, the charge is collected not only by the active device, but also by the substrate because of the shunt effect. The sum of them also decreases from 890 to 853 pC. This demonstrates that the charge escape increases. Therefore, with the carrier concentration diffusion to the passive increasing, charge sharing becomes more significant.

4.3. Temperature dependence in devices with a source

Although the charge sharing between transistors without sources can be explained by the increase of the charges escape from the drifting collection in the active device, charge sharing between transistors with sources still can not be explained. As Figure 7 shows, the charge collection at an active NMOS nearly remains the same when the temperature increases from 380 to 420 K, while the charge sharing on the passive NMOS still increases. The charge collection in the PMOS case is more remarkable, which exhibits an increasing trend on both the active device and the passive device.

In transistors with sources, especially a PMOS with a source, bipolar amplification becomes a major charge sharing mechanism. So, we should analyze how the temperature affects bipolar amplification. The parasitic bipolar is triggered by the disturbing of the well potential. The well potential is

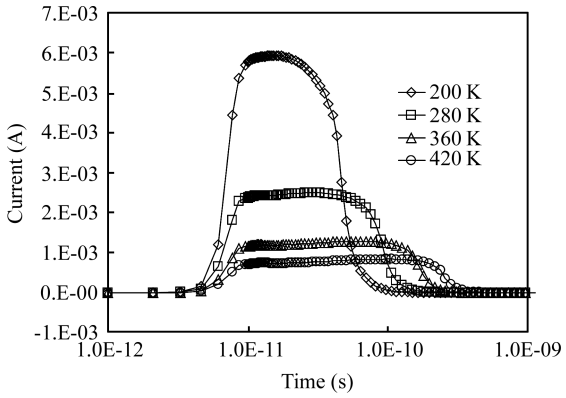

Fig. 8. Current pulses at the N-well contact at different temperatures.

determined by the *I*–*R* drop of the majority-carrier flow to contact. As shown in Fig. 4, the resistor between the base of the bipolar and the N-well contact, R_{NW}, can be expressed as

$$R_{\mathrm{NW}} \propto \frac{1}{qn\mu}.$$

Equation (4) indicates that μ decreases when the temperature rises. So, when the temperature increases, the R_{NW} will increases, and the majority-carrier current to the N-well contact can be too small to obtain the same *I*–*R* drop. With the same amount of majority-carriers and a smaller current, the time of the current to the N-well contact can persist longer, and the parasitic bipolar transistor can conduct longer.

To verify the analysis above, we plot the current of the N-well contact at different temperatures. As Figure 8 shows, the contact current reaches 5.93 mA at a temperature of 200 K, but it only persists 46.8 ps. However, at a temperature of 420 K, the contact current is smaller than 0.84 mA, but it persists 274 ps. With a longer working time of the parasitic bipolar, more charges will be injected from the source at higher temperatures. Thus, the charges collected on both the active PMOS and the passive PMOS increase with temperature. Alles[15] also reported that bipolar amplification increases with temperature, which agrees with our results, except if it is an SOI device.

The bipolar effect can also explain the charge collection curves of an NMOS between 200 and 420 K shown in Fig. 7. When the temperature is between 200 and 380 K, the main charge collection mechanism is the drift at the active device. So, the charge collection decreases as the temperature rises. However, when the temperature is between 380 and 420 K, the bipolar effect becomes comparable to the drift. The increase of bipolar charge compensates the decrease of the drift charge. So, the total charge is nearly the same. For the passive device, because both the diffusion charge and the bipolar charge increase, the charge sharing increases between 200 and 420 K.

4.4. Temperature dependence of recombination and incomplete ionization

The carrier lifetime may affect the charge collection at the passive junction. If the lifetime is too short, carriers will recombine before they reach the passive device. There is no

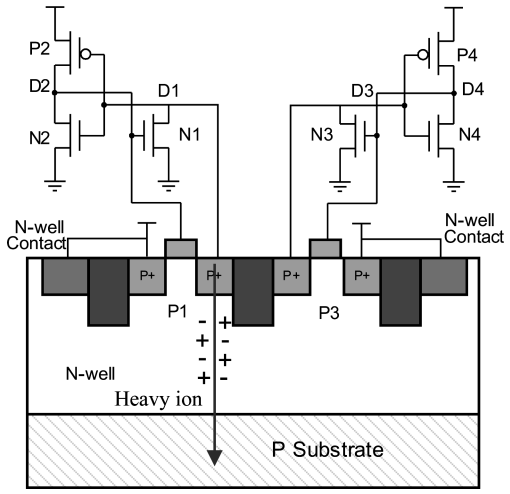

Fig. 9. 3D device/circuit mix-mode simulation structure for the MBU sensitivity simulation in two SRAM cells.

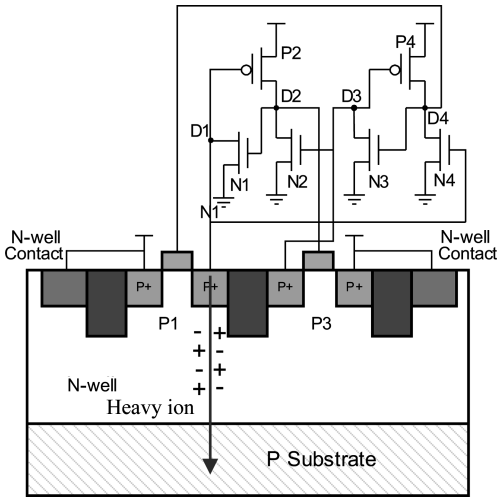

Fig. 10. 3D device/circuit mix-mode simulation structure for the upset sensitivity simulation in a DICE cell.

generally acceptable law to describe its temperature dependence. A power law[20] claims τ is described as

$$\tau(T) = \tau_0 \left(\frac{T}{300}\right)^{\alpha}.$$

However, τ estimated by the parameters given in Ref. [21], is more than 6.04×10^{-8} s in the range of 200–420 K, e.g., much longer than the charge sharing process, which is completed in 1×10^{-9} s. So, we can assume that the recombination in the charge sharing is very small and can be ignored. We have verified this assumption by closing all recombination switches in Sentaurus TCAD. The current shapes remain nearly the same as that in Fig. 3.

When the temperature is low enough, the impurity may ionize incompletely, which is know as the freeze-out effect. The freeze-out effect causes the carrier concentration to decrease, and then $R_{\rm NW}$ increases. However, the freeze-out effect is only significant below 120 K. When the temperature is higher than 200 K, the impurity can be regarded as fully ionized. So, the freeze-out effect can be ignored.

5. Temperature dependency of the storage cell's upset sensitivity

5.1. Simulation results

Charge sharing may induce the upset of multiple storage cells synchronously. 3-D device/circuit mixed simulations are carried out to examine the MBU sensitivity of two standard SRAM cells. The structure used to examine the MBU in the case of charge sharing between the PMOS is shown in Fig. 9. One cell consists of the transistors N1, N2, P1, and P2, and the other consists of the transistors N3, N4, P3, and P4. P1 and P3 are modeled on the device level with a distance of 0.6 μm between them. Other transistors are modeled on the circuit level. Ion strikes at the drain of P1. The MBU sensitivity is evaluated by $\rm LET_{th}$, which is defined as the minimum LET needed to upset the passive cell. The structure to examine the MBU between the NMOS is similar, except that N1 and N3 are modeled on the device level and other transistors are modeled on the circuit level. The temperature of both, the device level and the circuit level, is changed from 200 K to 420 K.

RHBD storage cells, such as a DICE cell and a HIT cell, can recover from a single node upset. However, the charge sharing may induce a multiple nodes upset in RHBD storage cells, and causes an upset of the whole cell. So, we will also examine the upset sensitivity of the DICE cell[3] at different temperatures by a mix mode simulation. The structure to examine the upset sensitivity due to charge sharing between the PMOS is shown in Fig. 10. P1 and P3 are modeled on the device level with a distance of 0.6 μm between them. Other transistors are modeled on the circuit level. The structure to examine the upset sensitivity due to the charge sharing between the NMOS is similar, except that N1 and N3 are modeled on the device level and other transistors are modeled on the circuit level.

The $\rm LET_{th}$ of the MBU of the SRAM cells versus the temperature is presented in Fig. 11, as the "All transistors" line. The $\rm LET_{th}$ decreases when the temperature rises. For charge sharing between the NMOS, the $\rm LET_{th}$ at 200 K is 19.4 MeV·cm^2/mg , while it decreases to 14.6 MeV·cm^2/mg at 420 K. For charge sharing between the PMOS, the $\rm LET_{th}$ at 200 K is 27.8 MeV·cm^2/mg , while it decreases to 17.7 MeV·cm^2/mg at 420 K.

However, the curve for the $\rm LET_{th}$ of the DICE cell versus temperature is not monotone, which is presented as the "All transistors" plotted in Fig. 12. When the temperature rises, the $\rm LET_{th}$ first increases, but then decreases. For the charge sharing between the NMOS, the largest $\rm LET_{th}$, which is 8.3 MeV·cm^2/mg, appears at 380 K, while the smallest LET appears at 200 K, which is 6.7 MeV·cm^2/mg . For charge sharing between the PMOS, the largest $\rm LET_{th}$ appears at 260 K, which is 16.5 MeV·cm^2/mg, while the smallest $\rm LET_{th}$ appears at 420 K, which is 13.0 MeV·cm^2/mg.

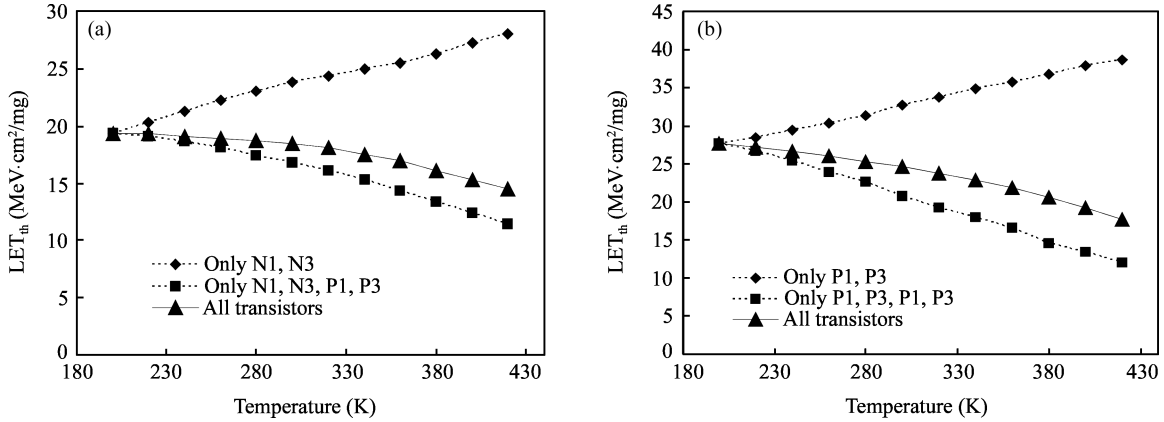

Fig. 11. 3D device/circuit mix-mode simulation structure for the upset sensitivity simulation in a DICE cell.

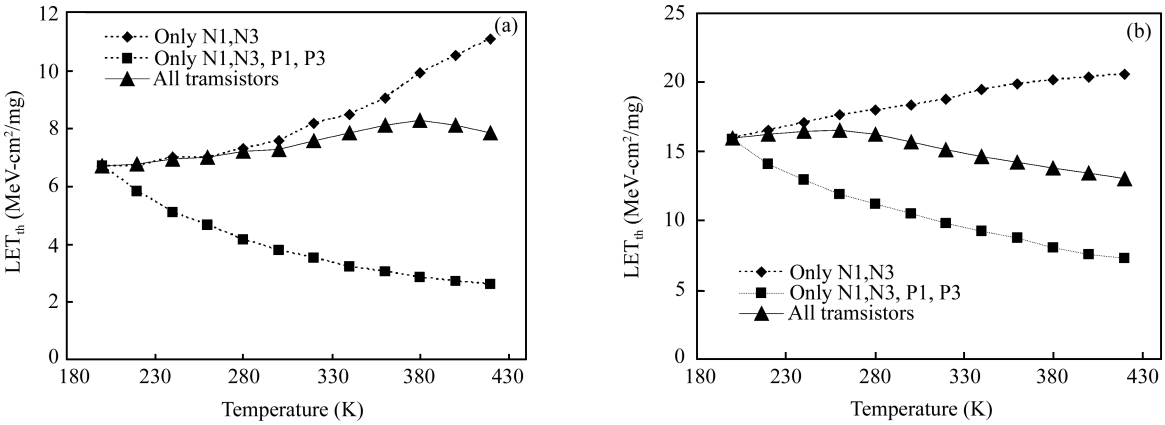

Fig. 12. 3D device/circuit mix-mode simulation structure for the upset sensitivity simulation in a DICE cell.

5.2. Discussion

Truyen[16] has also reported a parabolic relationship between the LET_{th} and the temperature. He explained this by the fact that the charge collection decrease competes with the shift of the operating point. Besides the charge collection devices, the electrical characteristics of other transistors are also temperature dependent. Because each transistor's effect on LET_{th} is different, we change the temperature of different transistors step by step to evaluate each transistor's effect.

Firstly, we evaluated the temperature dependency of the charge sharing collected by changing only the temperature on the device level (N1, N3 for charge sharing between NMOS; P1, P3 for charge sharing between PMOS) from 200 to 420 K, while keeping the temperature on the circuit level at 200 K. The result is presented in Figs. 11 and 12, as the "Only N1, N3" curve and "Only P1, P3" curve. For both the SRAM cell and the DICE cell, no matter if there is charge sharing in the NMOS or the PMOS, the LET_{th} increases when the temperature rises, because the peak value of the transient current decreases. The results agree with that in Ref. [16].

Secondly, the temperature on the device level and on the complementary transistors is changed. Corresponding to the structure in Figs. 9 and 10, the temperature on N1, P1, N3, P3 is changed. The complementary transistor can significantly influence the charge collection and the charge sharing. Because collected charges must be transported through the complementary transistor to reach the VDD or GND, the drain current I_D of the complementary transistor determines the charge collection efficiency at the active device. I_D can be expressed as

$$I_D = \frac{Z}{L}\mu C_{OX}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right].$$

When the temperature rises, μ will decrease, so that I_D will decrease. Therefore, the charge collected by the active device will decrease and the charge collected by the passive device will increase. On the other hand, when the temperature rises, I_D of the complementary transistor of the passive device will also decreases, so that the drain voltage of the passive device may be more easily disturbed. Both of the two effects will induce LET_{th} to decrease. The result is presented in Figs. 11 and 12, as the "Only N1, N3, P1, P3" line. As we can see, in this case, the LET_{th} decreases greatly compared to when only the temperature on the device level of the transistor is changed.

Finally, we discuss the effect of other transistors (N2, P2, N4, P4) on LET_{th}. These transistors have no direct effect on the charge collection and the charge sharing. However, when the temperature rises, the response speed of these transistors will decrease, so that the voltage disturbance will propagate to all nodes for a longer time. As Figures 9 and 10 show, the upset on D1 and D3 will propagate to D2 and D4 for a longer time. Therefore, the upset will be more severe for both the SRAM cells and the DICE cells. As shown in Figs. 11 and 12, the LET_{th} in the "All transistors" line increases significantly

compared to the "Only N1, P1, N3, P3" line.

In summary, we conclude that the temperature dependency of LET_{th} is determined by three factors: the peak value of the transient current, the recovery current by the complementary transistors, and the response speed of other transistors. Because of the interaction of these three factors, the LET_{th}'s temperature dependency is very complicated.

6. Conclusion

In this paper, the temperature dependence of the charge sharing has been investigated in a 130 nm technology. We find that the charge sharing collection and the MBU sensitivity heavily depend on the temperature.

In the simulation, the charge sharing collection increases with the temperature rise. The charge sharing collection varies by 66%–325% when the temperature ranges from 200 to 420 K. For an NMOS, the main reason is that with the decrease of the charge collection on the active NMOS, the charge diffusion to the passive NMOS increases. For a PMOS, the main reason is that the resistor to the well contact increases when the temperature rises.

The MBUs in two SRAM cells and a DICE cell were also investigated. The LET_{th} is affected by the temperature through three factors: the peak value of the transient current, the recovery current by the complementary transistors, and the response speed of other transistors. So, the temperature dependency is very complicated. For a SRAM cell, the LET_{th} decreases when the temperature rises, while for a DICE cell, the LET_{th} first increases and then decreases.

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