An approach to the optical interconnect made in standard CMOS process*

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Abstract: A standard CMOS optical interconnect is proposed, including an octagonal-annular emitter, a field oxide, metal 1-PSG/BPSG–metal 2 dual waveguide, and an ultra high-sensitivity optical receiver integrated with a fingered P+/N-well/P-sub dual photodiode detector. The optical interconnect is implemented in a Chartered 3.3-V 0.35-μm standard analog CMOS process with two schemes for the research of the substrate noise coupling effect on the optical interconnect performance: with or without a GND-guardring around the emitter. The experiment results show that the optical interconnect can work at 100 kHz, and it is feasible to implement optical interconnects in standard CMOS processes.

Key words: optical interconnect; standard CMOS; emitter; waveguide; ultra high-sensitivity
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1. Introduction

With the scaling of technology towards the nanometer regime, current metallic interconnect systems will not be sufficient to provide the ultimate solution to the increasing performance mismatch between devices and interconnects and to ensure the required performance projected in the semiconductor roadmap, due to the limitations posed by resistive losses, frequency dependent losses, dielectric loss from the substrate material, inter-line crosstalk, latency, connectivity, power consumption, and so on. This realization that the need is beyond the traditional metal/dielectric system has led to investigations into new interconnect concepts to be able to continue developing IC technology according to Moore's law[1]. Among the future interconnect technologies that have been heavily researched, one of the most promising to overcome predicted interconnect limitations are optical interconnects[2–4] identified by the international technology roadmap for semiconductors (ITRS), which have the advantage of not being affected by the electromagnetic wave phenomena, distance independence of performance, frequency independence, architecture facility, timing simplicity, and so on.

In today's semiconductor technologies, the communication bottleneck has been identified as one of the important challenges in the progress of silicon computation, while individual logic elements have become significantly faster, computational speed is limited by the communication between different parts of a processor[5]. To outperform electrical wires and to ultimately solve the communication bottleneck in high-performance integrated circuits, optical interconnects should be monolithically fabricated using CMOS compatible silicon-based materials and processes. Over the past few years, significant progress has been made in the development of silicon-based building blocks for on-chip optical interconnects[6, 7], and several fully silicon-based optical interconnects have been reported[8–10]. However, which optical interconnect to use in standard CMOS processes remains an open question.

This paper presents a simple intra-chip optical interconnect system, shown in Fig. 1. It includes a light source (emitter/LED), a waveguide, and an optical receiver integrated with a photodetector. The optical interconnect is fabricated in a Chartered 3.3-V 0.35-μm standard analog CMOS process.

2. Standard CMOS light emitter

The phenomena of light emission by a silicon PN junction was firstly reported by Newman[11]. Then, several other silicon-based light emission schemes were also investigated[12, 13]. However, using silicon-based material systems for light emission in optical interconnects still requires major breakthroughs due to the laser's low light emission efficiency for current CMOS techniques.

This section presents a silicon-based standard CMOS light emitter utilizing the PN-junction's reverse avalanche breakdown effect for light emission. The planform of the light emitter is shown in Fig. 2. It is comprised of several octagonal-annular N+ regions and octagonal-annular P+ regions encircling each other within a rectangular N-well region to form several octagonal-annular PN-junction regions, with an octagonal N+ region as the centre.

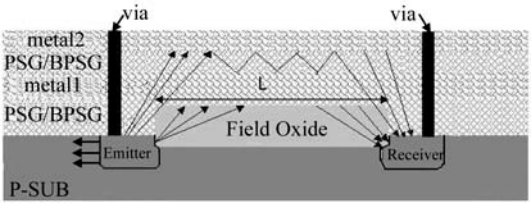

Fig. 1. Standard CMOS intra-chip optical interconnect system.

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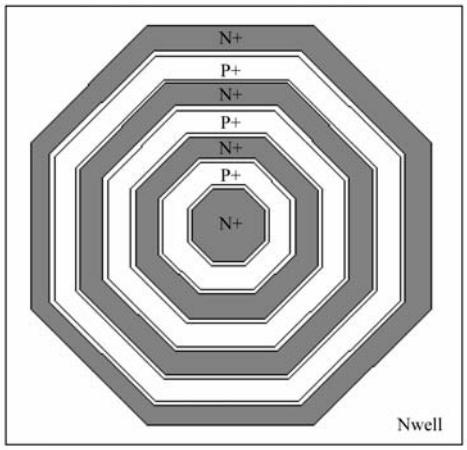

Fig. 2. Planform of a standard CMOS P+/N+/N-well light emitter.

Fig. 3. Photograph showing the light emission from a 2×2 P+/N+ /N-well light emitter array.

The advantages of this type of light emitter are:

(a) The PN-junction area is increased greatly. As a result, the carrier recovery probability is improved a lot.

(b) The light emission area is enlarged for the maximized PN-junction area, and a larger emission optic power can be acquired.

(c) The electric field is mainly concentrated to the sharp-angled regions of the P+ and N+ regions. Therefore, the avalanche multiplication effect will primarily occur in these areas due to a much bigger carrier accelerate rate. As a result, the breakdown voltage is reduced.

Figure 3 is a photograph showing the light emission from a 2×2 P+/N+/N-well light emitter array under a 10 V reverse bias, where the area of a light emitter is 46×46 μm^2. Figures 4(a) and 4(b) are the reverse breakdown characteristics of the P+/N+ junction and the N-well/P-sub junction, respectively. The pictures show that the reverse breakdown voltages are 8.5 and 18 V, respectively, confirming that the light emission of the emitter is generated by its P+/N+ junction.

3. Standard CMOS waveguide

Recently, a lot of research has been conducted on silicon-based waveguides[14], especially the SOI waveguide[15]. However, none of these waveguides is compatible with standard CMOS processes. This section proposes a simple silicon-based standard CMOS waveguide. Its cross section is shown in Fig. 1.

The waveguide is actually comprised of two types of waveguide. One is a field oxide waveguide, utilizing a field oxide as the core material and PSG/BPSG upon the field oxide and the silicon substrate as the coating material. The other is a metal 1–PSB/BPSG–metal 2 waveguide, utilizing PSG/BPSG between metal 1 and metal 2 as the core material, and metal 1 and metal 2 as the coating material. In standard CMOS processes, the refractive index of the field oxide, the PSG/BPSG, the silicon, and the metal are 1.5, 1.47, 3.5, and 1.39, respectively. Therefore, the light propagation efficiency of this type of waveguide may be too low because of the small refractive index difference between the core material and the coating material, and the big absorption loss in the metal (about 400 dB/cm). However, it provides an idea of the implementation of an optical waveguide in standard CMOS processes.

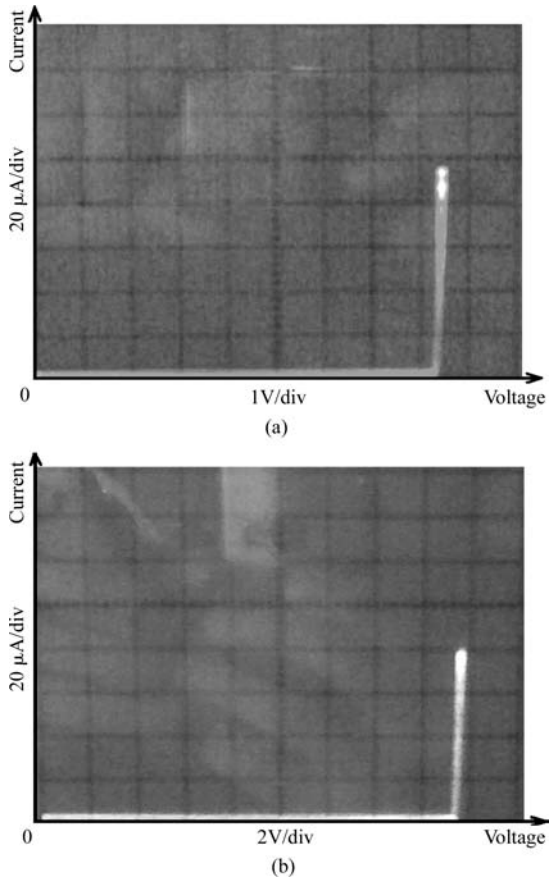

Fig. 4. Reversed breakdown characteristic: (a) P+/N+ junction; (b) N-well/P-sub junction.

4. Ultra high-sensitivity standard CMOS opto-electronic integrated receiver

Due to the low light emission efficiency of standard CMOS light emitters and the low light propagation efficiency of standard CMOS waveguides, an ultra high-sensitivity opto-electronic integrated receiver is needed.

Generally, high sensitivity can be achieved by high-responsivity photodetectors. In standard CMOS processes, the N-well/P-sub photodetector can satisfy this requirement, whose responsivity is about 0.3 A/W[16]. However, to avoid the substrate carrier crosstalk effect during light propagation and to ensure that the photodetector correctly responses to light radiation signals of the emitter, a fingered P+/N-well/P-sub dual photodiode detector is applied here,

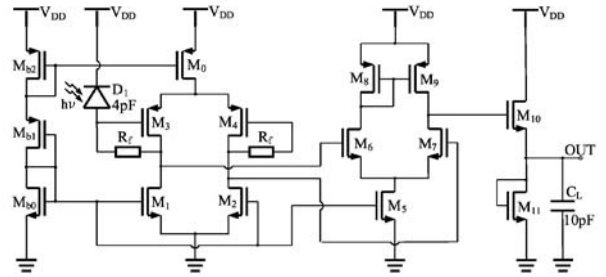

Fig. 5. An ultra high-sensitivity optoelectronic integrated receiver.

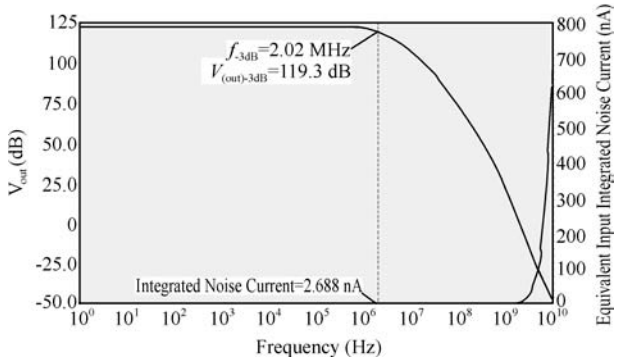

Fig. 6. Simulated frequency response and noise characteristic.

in which an N-well/P-sub diode is formed to shield substrate carriers out of the zone of the operation diode (P+/N-well diode) and to eliminate noise interferes. But the photodector′s responsivity of 0.0378 A/W is much lower compared to a previous N-well/P-sub photodetector[17]. Therefore, ultra-high sensitivity should be achieved by the design of an optical receiving circuit, meaning that an ultra high-resistance feedback resistor R_f and an ultra low noise transimpedance amplifier should be applied.

Figure 5 shows the ultra high-sensitivity optoelectronic integrated receiver proposed in this paper, where the area of the fingered P+/N-well/P-sub dual photodiode detector is 83 × 83 μm^2, the junction capacitance of the photodetector is about 4 pF, the resistance of R_f is 104 kΩ, the W/L of the two input PMOS (M1 and M2) is 320 μm / 0.4 μm, and the load capacitance is 10 pF. Figure 6 displays the simulated frequency response and the noise characteristic. It shows that the receiver achieves a 122.3-dBΩ transimpedance gain and a 3-dB bandwidth at 2.02 MHz, and its equivalent input integrated noise current from zero up to –3 dB frequency is 2.688 nA. The average minimum receiving optic power is about 497.78 nW, corresponding to a –33.03 dBm sensitivity (The calculation of the optical sensitivity is described in detail in Ref. [18]).

5. Experimental results

The proposed optical interconnect is implemented in a Chartered 3.3-V 0.35-μm standard analog CMOS process, where the waveguide length is about 8.5 μm. To study the substrate noise coupling effect on the performance of the optical interconnect, two schemes are designed, shown in Figs. 7(a) and 7(b), respectively. In Fig. 7(b), there is a GND-guardring

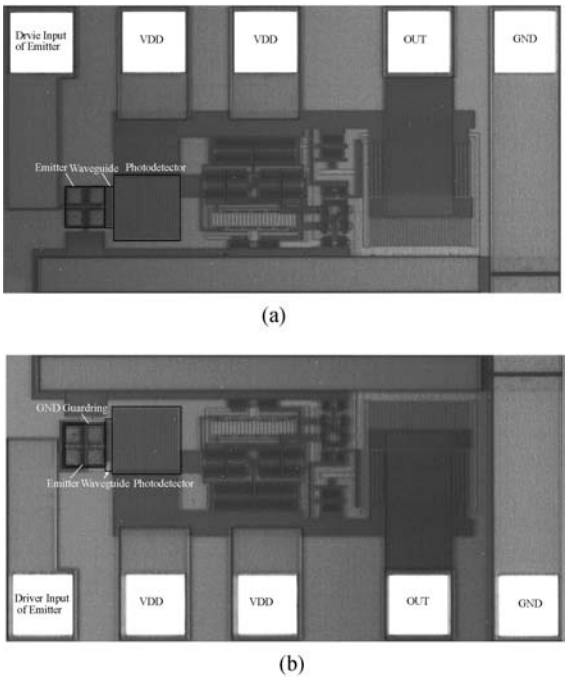

Fig. 7. Photographs of the optical interconnect: (a) Without GND-guardring around the emitter; (b) With GND-guardring around the emitter.

around the emitter to eliminate substrate noise and to isolate the emitter from the photodetector, while this is not the case in Fig. 7(a).

To analyze the optical interconnect, a square-wave voltage with a 13-V amplitude (less than the breakdown voltage of the N-well/P-sub junction) and a 35% on/off ratio was added to drive the emitter. Meantime, an oscilloscope was used to observe the output response. Figure 8 shows the experimental results at 1 and 100 kHz. It is obvious that the response shown in Fig. 8(b) is very noisy because of the substrate noise and other coupling noises between the emitter and the photodetector. But in Fig. 8(c), these noises are reduced by the addition of an isolation ring (GND-guardring) around the emitter. We also observed that the response amplitude of Fig. 8(c) was smaller than that of Fig. 8(b) because the isolation ring also blocked carriers generated in the emitter region directly coupling to the photodetector.

The experiment results show that the optical interconnect achieves a 100 kHz response frequency. Though the frequency is a bit low, it is validated that the optical interconnect works. The factors contributing to this phenomena are complicated, and the main factors maybe the low light emission efficiency, the low modulation speed of the standard CMOS light emitter, and the large coupling loss of the standard CMOS waveguide.

6. Conclusion

A standard CMOS optical interconnect is proposed and implemented in a Chartered 3.3-V 0.35-μm standard analog CMOS process in this paper. To verify that the response of the optical receiver comes from the radiated light of the emitter, a GND-guardring is added around the emitter to isolate the emitter and the photodetector and to eliminate the noise cou-

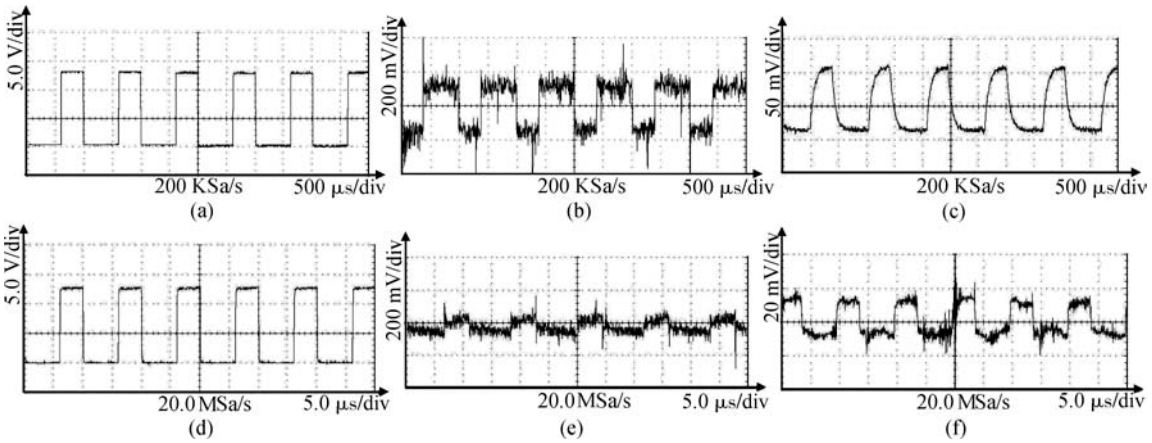

Fig. 8. Experimental results of the optical interconnect: (a), (d) 1 and 100 kHz drive signals for the emitter, respectively; (b), (e) Output signals of the optical interconnect without GND-guardring around the emitter (Fig.7(a)); (c), (f) Output signals of the optical interconnect with GND-guardring around the emitter (Fig.7(b)).

pling. The experimental results demonstrate that the optical interconnect works well at 100 kHz.

References

[1] Kshirsagar G, Chowdhury M H. Optical interconnect technology: photons based signal communication. IEEE Asia Pacific Conference on Circuits and Systems, 2006: 1426

[2] Miller D A B. Optical interconnects to silicon. IEEE J Sel Topics Quantum Electron, 2000, 6(6): 1312

[3] Scandurra A, Lenzi M, Guerra R, et al. Optical interconnects for network on chip. 1st International Conference on Nano-Networks and Workshops, 2006: 1

[4] Kash J A, Doany F, Kuchta D, et al. Terabus: a chip-to-chip parallel optical interconnect. The 18th Annual Meeting of the IEEE Lasers and Electro-Optics Society, 2005: 363

[5] Haurylau M, Chen G, Chen H, et al. On-chip optical interconnect roadmap: challenges and critical directions. IEEE J Sel Topics Quantum Electron, 2006, 12(6): 1699

[6] Van Thourhout D, Roelkens G, van Campenhout J, et al. Technologies for on-chip optical interconnects. The 18th Annual Meeting of the IEEE Lasers and Electro-Optics Society, 2005: 204

[7] O'Connor I, Tissafi-Drissi F, Navarro D, et al. Integrated optical interconnect for on-chip data transport. IEEE North-East Workshop on Circuits and Systems, 2006: 209

[8] Keeler G A, Agarwal D, Debaes C, et al. Optical pump-probe measurements of the latency of silicon CMOS optical interconnects. IEEE Photonics Technol Lett, 2002, 14(8): 1214

[9] Chatterjee A, Mongkolkachit P, Bhuva B, et al. All Si-based optical interconnect for interchip signal transmission. IEEE Photonic Technol Lett, 2003, 15(11): 1663

[10] Lazarouk S K, Jaguiro P V, Leshok A A, et al. Reverse biased porous silicon light-emitting diodes for optical intra-chip interconnects. Physica E: Low-dimensional Systems and Nanostructures, 2003, 16(3/4): 495

[11] Newman R. Visible light from a silicon p-n junction. Phys Rev, 1955, 100(2): 700

[12] Ng W L, Lourenco M A, Gwilliam R M, et al. An efficient room-temperature silicon-based light-emitting diode. Nature, 2001, 410(6825): 192

[13] Rong H, Jones R, Liu A, et al. A continuous-wave Raman silicon laser. Nature, 2005, 433(7027): 725

[14] Bogalecki A W. Design of a waveguide based optoelectronic integrated circuit in silicon 0.8 micron BiCMOS technology. 10th Mediterranean Electrotechnical Conference, 2000: 1206

[15] Png C E, Reed G T, Atta R M H, et al. Development of small silicon modulators in silicon-on-insulator. Proceedings of SPIE on Photonics Packaging and Integration III, 2003, 4997: 190

[16] Woodward T K, Krishnamoorthy A V. 1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies. IEEE J Sel Topics Quantum Electron, 1999, 5(2): 146

[17] Yu Changliang, Mao Luhong, Song Ruiliang, et al. Design and implementation of an optoelectronic integrated receiver in standard CMOS process. Chinese Journal of Semiconductors, 2007, 28(8): 1198

[18] Das M B, Chen J W, John E. Designing optoelectronic integrated circuit (OEIC) receivers for high sensitivity and maximally flat frequency response. IEEE J Lightwave Technol, 1995, 13(9): 1876