Adaptive digital calibration techniques for narrow band low-IF receivers with on-chip PLL

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Abstract: Digital calibration and control techniques for narrow band integrated low-IF receivers with on-chip frequency synthesizer are presented. The calibration and control system, which is adopted to ensure an achievable signal-to-noise ratio and bit error rate, consists of a digitally controlled, high resolution dB-linear automatic gain control (AGC), an inphase (I) and quadrature (Q) gain and phase mismatch calibration, and an automatic frequency calibration (AFC) of a wideband voltage-controlled oscillator in a PLL based frequency synthesizer. The calibration system has a low design complexity with little power and small die area. Simulation results show that the calibration system can enlarge the dynamic range to 72 dB and minimize the phase and amplitude imbalance between I and Q to 0.08 ° and 0.024 dB, respectively, which means the image rejection ratio is better than 60 dB. In addition, the calibration time of the AFC is 1.12 μs only with a reference clock of 100 MHz.

Key words: short range device; AGC; AFC; receiver; I/Q calibration
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1. Introduction

With the increasing emphasis on the integration, cost and power consumption, quadrature low-IF receivers, which combine the advantages of both the heterodyne receiver and the zero-IF receiver, are widely used in modern wireless communication systems. CMOS technology makes a low-cost integration of radio frequency (RF) circuits and digital functions on a single chip possible. Nowadays, lots of full-CMOS monolithic transceivers are being explored[1−3]. A typical low-IF direct conversion monolithic receiver with an on-chip frequency synthesizer is shown in Fig. 1. The received RF signal is amplified by a variable-gain low noise amplifier (LNA) and then down converted directly with an on-chip frequency synthesizer into inphase (I) and quadrature (Q) baseband signals. Then, the polyphase filter is used to provide sufficient attenuation to the image signal and the adjacent channel that transforms into an interferer due to aliasing from analog-to-digital converter (ADC) sampling. Following that, variable gain amplifier (VGA) further amplified the filtered signal to the optimal signal loading of the ADC.

However, the nonideal factors of the receiver, which may deteriorate the receiver's bit error rate (BER), mainly lie in the following three aspects. First, the amplitude of the incoming RF signal can vary over a wide dynamic range. To relax the requirement of the input dynamic range of an ADC, automatic gain control (AGC) is needed to adjust the signal channel gains before the ADC[4, 5]. Second, as shown in Fig. 1, the quadrature down-conversion is widely used for most modulation schemes in modern digital communications. However, all components in each channel will contribute an amplitude and phase imbalance between I and Q channels. To meet the requirement of performance, I/Q gain and phase imbalance calibrations have to be used[6−8]. Finally, in submicron CMOS technologies, the supply voltage is scaled down, which leads to a smaller tuning voltage range. However, a wide tuning range is usually needed to cover desired frequency bands and to compensate the process, voltage, and temperature variations. The above two reasons lead to a large VCO gain, which degrades the phase noise of a PLL and, hence, the receiver. Consequently, AFC is indispensable[9].

The above mentioned adaptive digital calibration techniques are embedded in a monolithic transceiver for short range devices (SRDs) that meet the ETSI EN300 200 standard requirement to verify their effectiveness. The proposed AGC system is described and analyzed. A phase and amplitude imbalance calibration technique and AFC are also discussed.

2. AGC

The AGC plays a critical part in the wireless receiver because the power received through the wireless channel is unpredictable. The received signal will be converted to a digital signal and demodulated at the digital baseband. The signal-to-noise ratio (SNR) of an ADC under the condition of full-scale power can be expressed as

$$\mathrm{SNR} = 6.02N + 1.76 \ [\mathrm{dB}]. \tag{1}$$

However, a receiver with fixed gain cannot make the signal strength at the ADC input reach the requirement of full-scale power. Assuming that the full-scale power and the actual signal power is V_f and V_r, respectively, the SNR of the ADC is reduced to

$$\mathrm{SNR} = 6.02N + 1.76 - 20\lg\frac{V_\mathrm{f}}{V_\mathrm{r}} \ [\mathrm{dB}]. \tag{2}$$

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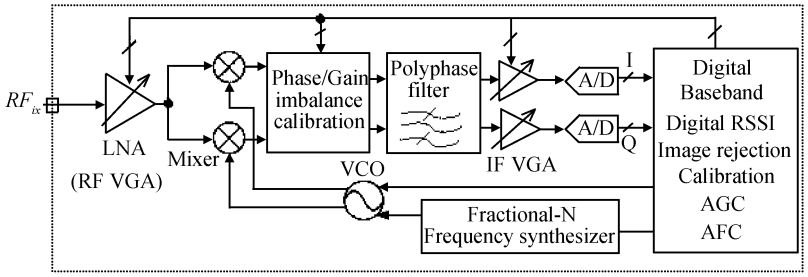


Fig. 1. Block diagram of the receiver with an on-chip frequency synthesizer.

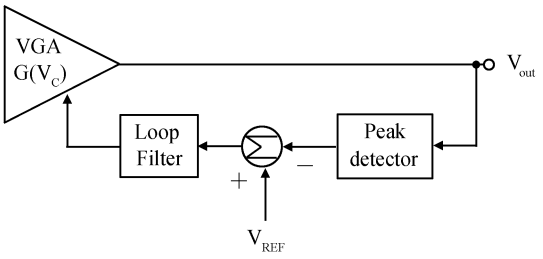


Fig. 2. Block diagram of the analog AGC.

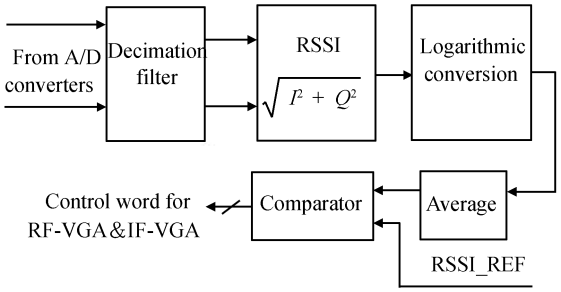


Fig. 3. Block diagram of the digital AGC.

Consequently, an AGC with wide dynamic range is essential in the receiver.

The power at the receiver P_r can be expressed in Eq. (3) when the power at the transmitter antenna P_t is known.

$$P_r = \frac{G_t G_r c}{f\,(4\pi r)^2} P_t, \tag{3}$$

where G_t, G_r are the transmitter and receiver antenna gain, respectively, c is the speed of light in vacuum, f is the operating frequency, and r is the transmission range. As specified in the standard, the transmission range is from 1 to 100 m, consequently the signal strength variation range is 40 dB. In this case, the dynamic range of the receiver must be higher than 60 dB to ensure a SNR better than 20 dB[13].

The AGC is typically an adaptive feedback system to adjust the gain of the receiver so as to provide a constant output signal level to the ADC with variable input signal strength. Several approaches for an AGC have been proposed[4, 5]. The analog type, which is realized by analog devices[4], is shown in Fig. 2. The input signal is amplified by the VGA. The comparator compares the signals extracted from the strength of the output by the peak detector with a reference voltage to set analog control signals in the output for the VGA. The main drawback of this method is that a relatively high power and a large die area are needed. In addition, the noise performance and the precision are poor due to process and temperature variations. In Ref. [5], the AGCs required extra digital-to-analog converters (DACs) to control the gain in the analog domain, which increases the power consumption.

A fully digitally controlled AGC is introduced in this paper, as shown in Fig. 3. The control part including a received signal strength indicator (RSSI), a comparator, and a loop filter is implemented by digital circuits. The detailed AGC algorithm is illustrated as follows. The quantized output data of ADC in I and Q channels are first filtered by a digital decimation filter with a decimation factor of eight to remove the unwanted frequency component and to reduce the data rate. Assuming that the signals in I and Q channels after the filter are (I, Q), in which I is an in-phase component and Q is a quadrature component. The absolute magnitude can be determined from (I, Q). Then a 7-bit digital RSSI is used to present the signal strength, in which the highest bit is the sign-bit. The amplitude of the quadrature components can be expressed as $R = \sqrt{I^2 + Q^2}$[10]. However, it is time and hardware consuming to perform the multiplication and square root operations. Thus, $\max(|I|, |Q|) + \frac{1}{4}\min(|I|, |Q|)$, which only requires comparisons of the largest and the smallest of the magnitude of I and Q; a shift of two bits to the right to implement in a divide-by-four operation, and an addition is used to approximate the function $R = \sqrt{I^2 + Q^2}$.

In order to enlarge the dynamic range and enhance the operation speed of the AGC, the value in the RSSI register is converted into logarithmic scaling expressed as $R_{dB} = 4\log_2 R$. Since the relation between log base 10 and log base 2 is

$$20\log_{10} R = 20\frac{\log_2 R}{\log_2 10} \approx 6\log_2 R \approx 1.5R_{dB}, \tag{4}$$

resulting in a power having decimal value given by $1.5R_{dB}$ and a least significant bit (LSB) of 1.5 dB.

After conversion, the value is calculated over 2^n symbol periods in which n = 0, 1, 2, 3. The selection of the sample symbol period is a trade off between speed and accuracy. Then the value after the averaging is compared with a reference value $RSSI_{ref}$. When the power difference is within the range of $RSSI_{offset}$, the gain control is ended. Otherwise, the control word is increased if the sign-bit in the RSSI register is 1 and vice versa.

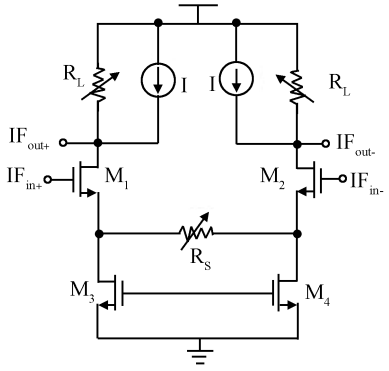


Fig. 4. Circuit of the VGA core.

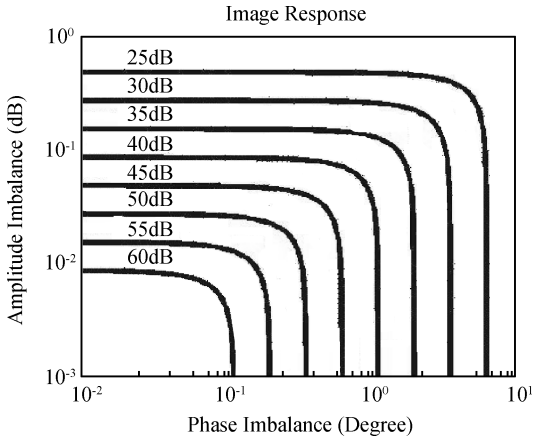


Fig. 5. Image responses versus amplitude and phase imbalance.

The block diagram of the VGA core is shown in Fig. 4[9]. It consists of three variable gain stages. The gain of an individual amplifier is from 6 to 24 dB with 6-dB per step. By changing the degeneration resistance combined with the load resistance, different gains can be realized. The channel of input transistors is set relatively long to improve matching and to reduce flicker noise. A large resistive load for a fixed current will limit the available margin. A current source load will degrade the linearity and introduce noise. In order to maintain the compromise among gain, linearity, and noise, a parallel combination of a current source with a resistor is used.

Because the gain of a VGA is adjustable in steps of approximately 6 dB, the signal strength at the input of the receiver referred from the value in the RSSI register and the reference value can be expressed as

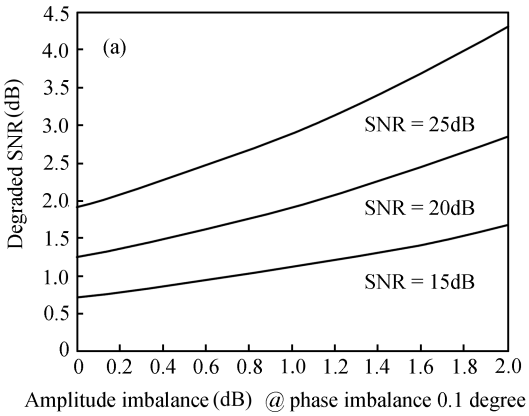
$$P|_{\mathrm{dB}} = 1.5R_{\mathrm{dB}} - \mathrm{RSSI}_{\mathrm{offset}} - 6\mathrm{VGA}_{\mathrm{control}}. \quad (5)$$

3. I/Q imbalance calibration

The level of phase and gain imbalance determines the image rejection ability, which is given by a image rejection ratio (IRR), as shown in Eq. (6).

$$\mathrm{IRR} = 20\lg\frac{A_{\mathrm{d}}}{A_{\mathrm{im}}}, \quad (6)$$

where A_{d}, A_{im} are the power of the desired signal and the image signal, respectively.



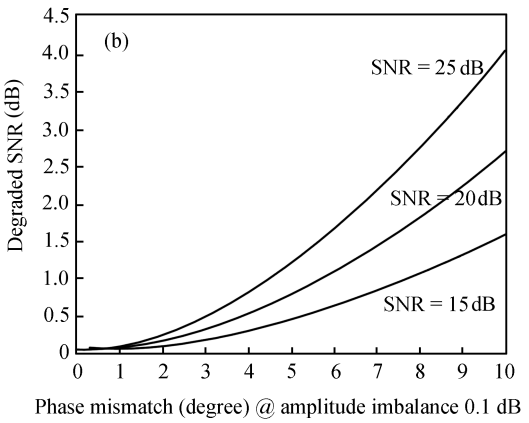


Fig. 6. (a) SNR degradation versus amplitude imbalance @ phase imbalance of 0.1 degree for different SNRs; (b) SNR degradation versus phase imbalance @ amplitude imbalance of 0.1 dB for different SNRs.

The requirement of IRR is determined by the selection of the IF and the applications. The image interference is an adjacent channel interference when a low-IF architecture is employed for SRDs. Consequently, the minimum requirement for IRR can be expressed as

$$\begin{aligned}\mathrm{IRR} &> C/I|_{\mathrm{dB}} + \left(P_{\mathrm{image}}\big|_{\mathrm{dBm}} - P_{\mathrm{desiredsignal}}\big|_{\mathrm{dBm}}\right)\\ &= 12 + \left(P_{\mathrm{image}}\big|_{\mathrm{dBm}} - P_{\mathrm{desiredsignal}}\big|_{\mathrm{dBm}}\right)\\ &= 12 + 34\ [\mathrm{dB}] = 46\ [\mathrm{dB}]. \end{aligned} \quad (7)$$

The relationship between I/Q gain and phase imbalance is shown in Fig. 5. As shown in Fig. 5, for an IRR of 46 dB, the gain and phase imbalance must be smaller than 0.045 dB and 0.58 °. The SNR degradation versus the phase imbalance for different SNR in the presence of an amplitude imbalance is set to 0.1 dB, as shown in Fig. 6(a). Similarly, the SNR degradation versus the phase imbalance for different SNR in the presence of a phase imbalance is set to 0.1 °, as shown in Fig. 6(b).

Several approaches for the detection and the compensation for an I/Q gain and a phase imbalance have been proposed. The mixed-signal calibration approach using a least mean square (LMS) algorithm was reported in Ref. [6]. The analog calibration method introduced in Ref. [7] uses a negative-feedback loop. The main disadvantage of these two proposed

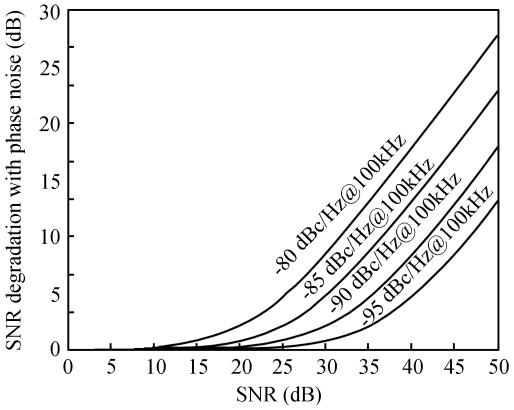


Fig. 7. SNR degradation versus SNR for different phase noises.

techniques is that two additional mixers are needed in both I and Q paths, which leads to a higher power consumption and requires a larger area. The receiver in Ref. [8] proposed a DSP-based calibration technique. The major drawback is that large calculations are needed since the correction coefficients are obtained in the frequency domain by a discrete Fourier transformation (DFT). A mixed-signal calibration structure with little power and area consumption and a high resolution is proposed in this paper to raise the BER. The details about the phase and gain imbalance calibration circuits are described in Ref. [9].

Assume that two vectors I and Q have equal amplitudes and a phase error of ε. For the purpose of discussion and without loss of generality, the down-converted signal with a phase imbalance can be expressed as

$$\begin{aligned} I &= \cos(\omega_{\mathrm{IF}} t), \\ Q &= \sin(\omega_{\mathrm{IF}} t + \varepsilon), \end{aligned} \tag{8}$$

where ω_{IF} is the intermediate frequency. The new vectors I' and Q' could be orthogonal through the addition and subtraction of the I and Q with proper coefficients (α_i, i = 1, 2, 3, and 4), which can be expressed as

$$\begin{aligned} I' &= \alpha_1 I + \alpha_3 Q, \\ Q' &= \alpha_2 Q - \alpha_4 I. \end{aligned} \tag{9}$$

By substituting Eq. (8) into Eq. (9), we have:

$$\begin{aligned} I' &= \alpha_1 I + \alpha_3 Q = \alpha_1 \cos(\omega_{\mathrm{IF}} t) + \alpha_3 (1+\delta) \sin(\omega_{\mathrm{IF}} t - \varepsilon) \\ &= \sqrt{\alpha_1^2 + \alpha_3^2 (1+\delta)^2 + 2\alpha_1 \alpha_3 (1+\delta) \sin\varepsilon}\, \cos(\omega_{\mathrm{IF}} t - \Delta_I), \\ Q' &= \alpha_2 Q - \alpha_4 I = \alpha_2 (1+\delta) \sin(\omega_{\mathrm{IF}} t - \varepsilon) + \alpha_4 \cos(\omega_{\mathrm{IF}} t) \\ &= -\sqrt{\alpha_4^2 + \alpha_2^2 (1+\delta)^2 + 2\alpha_2 \alpha_4 (1+\delta) \sin\varepsilon}\, \cos(\omega_{\mathrm{IF}} t + \Delta_Q), \end{aligned} \tag{10}$$

where $\Delta I = \tan^{-1} \dfrac{\alpha_3 (1+\delta) \cos\varepsilon}{\alpha_1 + \alpha_3 (1+\delta) \sin\varepsilon}$ and $\Delta Q = \tan^{-1} \dfrac{\alpha_2 (1+\delta) \cos\varepsilon}{\alpha_4 + \alpha_2 (1+\delta) \sin\varepsilon}$.

Thus, orthogonality can be ensured when $\Delta I + \Delta Q = \frac{\pi}{2}$, that is

$$\tan^{-1} \frac{\alpha_3 (1+\delta) \cos\varepsilon}{\alpha_1 + \alpha_3 (1+\delta) \sin\varepsilon} + \tan^{-1} \frac{\alpha_2 (1+\delta) \cos\varepsilon}{\alpha_4 + \alpha_2 (1+\delta) \sin\varepsilon} - \frac{\pi}{2} = 0. \tag{11}$$

Since the imbalances δ and ε are quite small, Equation (11) can be expressed as

$$\tan^{-1} \frac{\alpha_3}{\alpha_1} + \tan^{-1} \frac{\alpha_2}{\alpha_4} - \frac{\pi}{2} = 0. \tag{12}$$

As a result, by compensating a series of coefficients, the phase imbalance between vectors I and Q can be eliminated.

From Eq. (10), we can find that only a partial gain imbalance is compensated in the phase imbalance compensation block, and it can be expressed in decibel as

$$\begin{aligned} &10 \lg \left(\frac{\alpha_1^2 + \alpha_3^2 (1+\delta)^2 + 2\alpha_1 \alpha_3 (1+\delta) \sin\varepsilon}{\alpha_4^2 + \alpha_2^2 (1+\delta)^2 + 2\alpha_2 \alpha_4 (1+\delta) \sin\varepsilon} \right) \\ &\approx 10 \lg \left(\frac{\alpha_1^2 + \alpha_3^2}{\alpha_4^2 + \alpha_2^2} \right). \end{aligned} \tag{13}$$

Hence, a gain calibration after the phase imbalance calibration is needed. Based on I' and Q', the new vectors I'' and Q'' will have an equal amplitude when two new coefficients α_5 and α_6 are introduced as follows:

$$\begin{cases} I'' = \alpha_5 \sqrt{\alpha_1^2 + \alpha_3^2 (1+\delta)^2 + 2\alpha_1 \alpha_4 (1+\delta) \sin\varepsilon} \\ \qquad \times \cos[\omega_{\mathrm{IF}} t + \theta(t) - \Delta_{\mathrm{I}}], \\ Q'' = \alpha_6 \sqrt{\alpha_4^2 + \alpha_2^2 (1+\delta)^2 + 2\alpha_2 \alpha_4 (1+\delta) \sin\varepsilon} \\ \qquad \times \cos[\omega_{\mathrm{IF}} t + \theta(t) + \Delta_{\mathrm{Q}}]. \end{cases} \tag{14}$$

So, the gain calibration expressed in decibel is

$$20 \lg \left(\frac{\alpha_5}{\alpha_6} \right) + 10 \lg \left(\frac{\alpha_1^2 + \alpha_3^2}{\alpha_4^2 + \alpha_2^2} \right). \tag{15}$$

The operation procedures are outlined as follows. In the calibration mode, a signal at the image frequency ($2f_{\mathrm{IF}}$ below the desired channel frequency) is applied at the RF input. For a perfect phase and gain match of I and Q paths, the values in the digital RSSI register are zero. Correspondingly, I and Q phase and gain differences can be fine-tuned by two 8-bit DACs for minimum RSSI value.

4. AFC

The VCO phase noise has a great effect on the performance of a receiver. Assuming that the input signal of the receiver consists of a desired small signal and an undesired large interfering signal whose frequency is close to that of the desired signal. When the two signals are down-converted by the mixer, the LO's noise is also down-converted by the large interfering signal. For a SRD receiver with a bandwidth of 400 kHz, the SNR degradation versus SNR with different phase-noises is shown in Fig. 7.

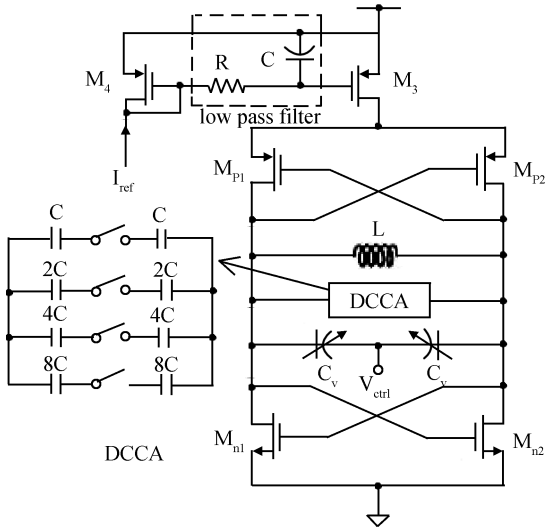


Fig. 8. Circuit of the VCO core.

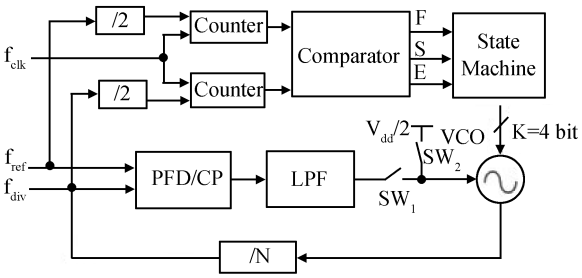


Fig. 9. Block diagram of AFC.

Many VCO calibration techniques have been proposed to search for the optimum sub-band frequency[11,12]. A phase based calibration technique is introduced in Ref. [8]. However, long counts are needed in case of an error, which is introduced by an uncertainty of an initial phase difference of the two inputs of the reference and divided VCO signal. Therefore, an open-loop automatic VCO calibration technique based on a period comparison is adopted and implemented full-digitally to speed up the calibration procedure while saving area and power.

The wide-band differential LC VCO core is shown in Fig. 8. To keep a small VCO gain and to ensure a wide overall tuning range (1 GHz in this design), a digital controlled capacitor array (DCCA) with a 4-bit control word in parallel with an LC tank is added. Both switches and MIM capacitors are binary weighted according to the control word.

The block diagram of the wideband frequency synthesizer with an AFC block, which is used to control the DCCA in the VCO, is depicted in Fig. 9. The AFC block is made up of phase detectors and a state machine. The operation is described as follows. Firstly, the switch SW_1 is turned off and SW_2 is turned on so that the PLL loop is an open loop and the VCO tuning voltage is set to $V_{dd}/2$ to fix the VCO output frequency. Then, both the reference clock (fref) and the divided VCO signal (fdiv) are firstly fed into divide-by-two circuits (DTCs), the period's information can be obtained from the count numbers during a high or low level of the output of the DTCs. Thus, the comparison result of the count numbers

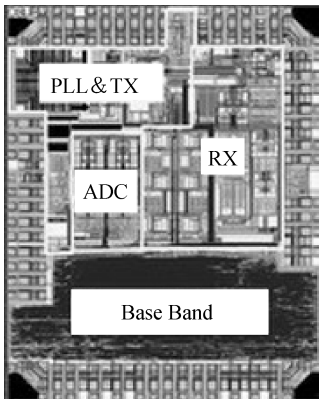


Fig. 10. Layout of the transceiver.

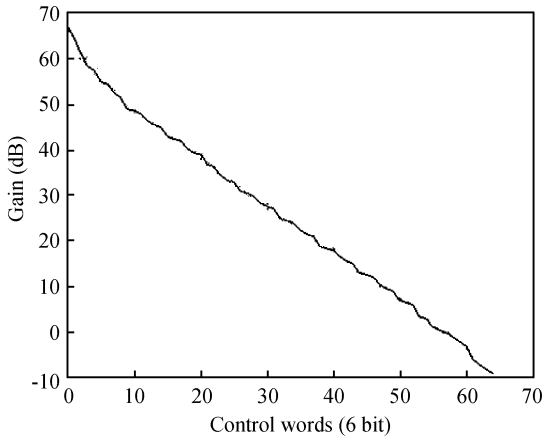


Fig. 11. Simulation result of the relation between control word and gain.

represents that of the frequencies of the two inputs, which can be used to drive the state-machine properly to produce the control word for the DCCA of VCO. The state machine adopted here is based on a 3-bit binary search algorithm and is set to 100 at the start, which is equal to the middle of the frequency bands of the VCO. Finally, the PLL loop returns to the closed loop condition. The target frequency is within the tuning range of the AFC code, and the remaining frequency deviation is adjusted.

5. Simulation results

A fully integrated transceiver for SRDs is implemented in 0.35 μm CMOS technology. All of the above mentioned calibration circuits haven been applied in this system. The total die area including the pads is 3.1×3.8 mm^2. The calibration technique is realized in digital circuits, and the chip area introduced by the calibration techniques is about 0.11 mm^2, which is ignorable. The dynamic current consumed by the calibration is about 520 μA. As the calibration circuits are pull down after the calibration is done, the power introduced by the calibration circuits is minimal. Figure 10 shows the layout of the transceiver. Figure 11 shows the gain tuning curve of the VGA block. Its gain changes from –7 to 67 dB when the control word changes from 0 to 2^6 and operates linearly in decibels, which is enough for the specification (60 dB). The calibration results of the phase and gain imbalances are shown in

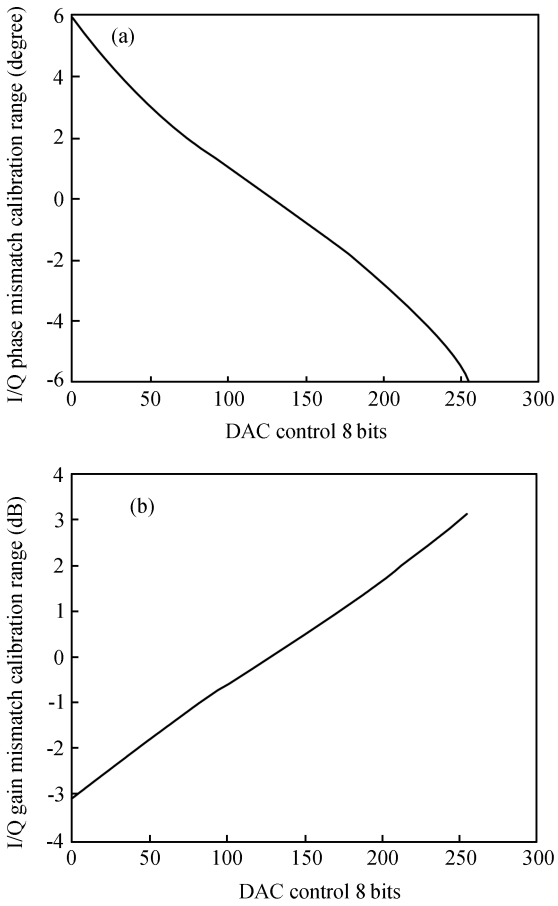


Fig. 12. (a) Simulation result of I/Q phase calibration range; (b) Simulation result of I/Q gain calibration range.

Figs. 12(a) and 12(b), respectively. The maximum compensable phase deviation is about ±6°, and the phase mismatch after calibration can be compensated to a level below ±0.08°. The maximum compensable gain deviation is about ±3 dB, and the gain deviation after calibration will be below ±0.024 dB. From the plot in Fig. 5, we find that the IRR after calibration can reach 60 dB, which satisfies the requirement of a large margin. In addition, from Fig. 6(a), we also can find that the SNR degradation due to an I/Q imbalance is only 0.01 dB.

In this work, the VCO is designed to have a frequency tuning range of 1.1–2.1 GHz with a control voltage of the varactor tuned from 0.6 to 2 V to cover the desired band with adequate margin, as shown in Fig. 13. Sixteen transfer characteristic curves of the VCO and the AFC are obtained because a 4-bit DCCA is adopted in the LC-tank of the VCO. To verify the AFC, the initial frequency setting code in the state machine is set to 111 (decimal code is 7), which is the worst case and corresponds to the lowest VCO frequency band. By using a clock of 100 MHz, the calibration time in the worst case is only 1.12 μs, as shown in Fig. 14.

6. Conclusion

A fully integrated low-IF receiver with on-chip frequency synthesizer is implemented in 0.35 μm mixed signal CMOS technology. On-chip digital calibration is introduced to improve the system's performance with little added power and area.

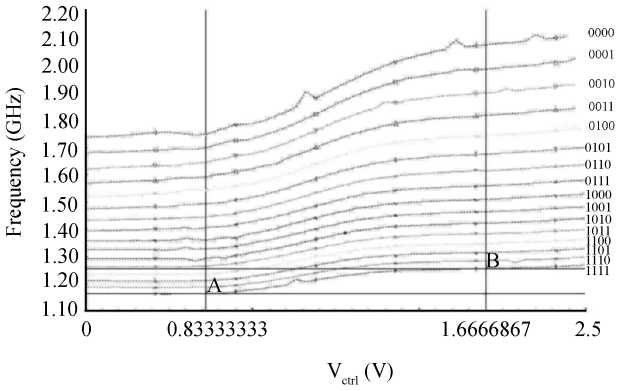


Fig. 13. Simulation results of the frequency tuning characteristic of the VCO.

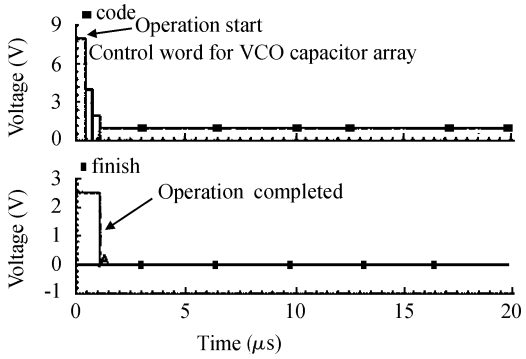


Fig. 14. Simulation results of the calibration time.

The digitally-controlled AGC with a 72 dB dynamic range controlled by 6-bit control word, which eliminates the problem of high-power consumption, is proposed to enlarge the dynamic range so as to improve the BER. A simple structure for extracting the phase and gain imbalances signal digitally and for compensating the imbalance in the analog domain has been proposed to improve the IRR and, hence, the BER performance of a low-IF receiver. After calibration, the SNR degradation caused by the imbalance is only 0.01 dB. The proposed structure enables a vary fast detection and compensation with negligible additional power dissipation and area usage. A fully digital AFC based on period calibration is utilized to correct the wide-band VCO. By using a clock of 100 MHz, the calibration time in the worst case is only 1.12 μm. Both analysis and computation have demonstrated the effectiveness of the method. The AGC, AFC and imbalance calibration technique is not only useful in SRDs, but also applicable in other wireless communication standards. Moreover, the proposed technique is not only useful in a low-IF receiver, but also applicable in the double low-IF architecture.

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