Memory characteristics of an MOS capacitor structure with double-layer semiconductor and metal heterogeneous nanocrystals*

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Abstract: An MOS (metal oxide semiconductor) capacitor structure with double-layer heterogeneous nanocrystals consisting of semiconductor and metal embedded in a gate oxide for nonvolatile memory applications has been fabricated and characterized. By combining vacuum electron-beam co-evaporated Si nanocrystals and self-assembled Ni nanocrystals in a SiO_2 matrix, an MOS capacitor with double-layer heterogeneous nanocrystals can have larger charge storage capacity and improved retention characteristics compared to one with single-layer nanocrystals. The upper metal nanocrystals as an additional charge trap layer enable the direct tunneling mechanism to enhance the flat voltage shift and prolong the retention time.

Key words: nonvolatile memory; nanocrystal memory; MOS capacitor
DOI: 10.1088/1674-4926/30/11/114003 **PACC:** 6170A; 7360; 7340Q

1. Introduction

Recently, nonvolatile memory (NVM) devices utilizing discrete nanocrystals as floating gate have received considerable attention due to their excellent memory performance and high scalability. In nanocrystal floating gate memory devices, nanocrystals such as semiconductor[1,2], metal[3], compound[4,5] or hetero-nanocrystal[6] are embedded between the control oxide layer and the tunneling oxide as charge storage nodes to replace the continuous floating gate layer used in the conventional NVM. Nanocrystal memories with ultrathin ($\leqslant$ 3 nm) tunneling oxide can promise low-voltage operation, fast program/erase (P/E) time, and good endurance characteristics through the direct tunneling charging/discharging mechanism[7–9]. For semiconductor nanocrystals, the intrinsic charge storage capacity is rather small with short retention characteristics using a direct tunneling oxide, due to the same energy band structures of the substrate and the nanocrystals[9]. A Si self-aligned doubly stacked dot memory has been proposed by Ohba *et al.*[10], in which it is experimentally shown that the double dot memory shows excellent charge retention. However, deep trapping at the interface would rather influence the retention characteristic of Si nanocrystal memory devices[11]. For metal nanocrystal memory devices, selectable work functions in metal nanocrystals create a deeper potential well to offers large charge storage capacity and good retention characteristics without sacrificing injection efficiency[12]. Traps are screened out due to the large density of states in metals[13]. In this paper, we propose an MOS capacitor structure with double-layer semiconductor and metal heterogeneous nanocrystals embedded in a gate oxide, which can offer even better memory characteristics. Charge injection goes across a direct tunneling oxide to the semiconductor and metal nanocrystals. On one hand, the upper metal nanocrystal layer offers a large storage capacity and enables stable operations independent of trap annealing. On the other hand, due to the Si conduction band being higher than that of Ni, the Ni nanocrystal layer as an additional memory node provides a deeper distributed potential well for a longer retention time.

2. Experiments

Schematic cross-sectional structures of MOS capacitors with single- and double-layer heterogeneous nanocrystals are shown in Fig. 1. After chemically cleaning the (100) p-type silicon wafer (14–25 Ω·cm), to ensure the direct tunneling mechanism, a 3 nm tunneling SiO_2 layer was thermally grown by dry oxidation at 750 °C. In order to reduce the interface states and defects between Si and SiO_2, subsequent annealing was

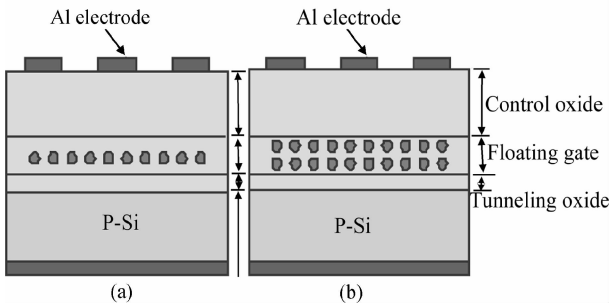

Fig. 1. Schematic cross-sectional structures of (a) MOS capacitor with single-layer semiconductor/metal nanocrystals and (b) MOS capacitor with double-layer semiconductor and metal nanocrystals.

* Project supported by the National Natural Science Foundation of China (No. 60776058), and the State Key Development Program for Basic Research of China (Nos. 2007CB935400, 2006CB302700).
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Received 19 January 2009, revised manuscript received 15 July 2009

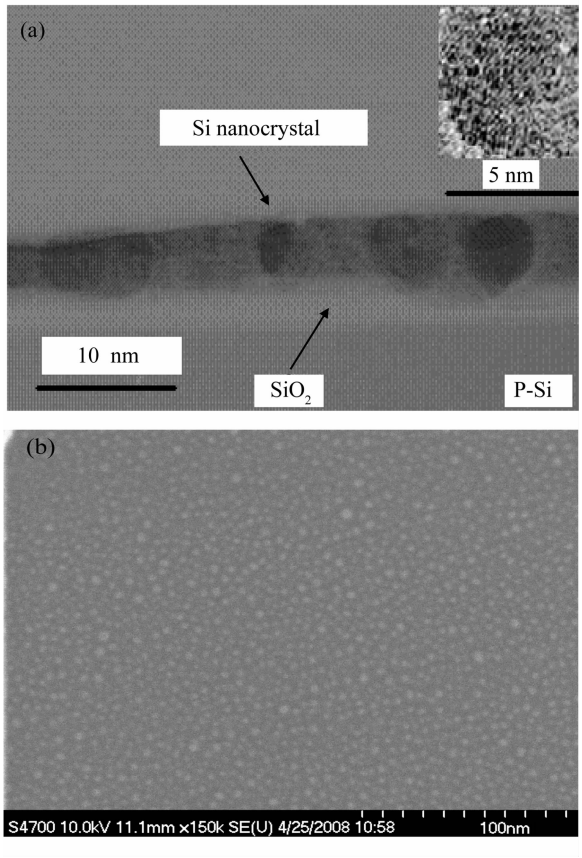

Fig. 2. (a) Typical TEM image of the MOS capacitor with single-layer Si nanocrystals; (b) Top view SEM image of Ni nanocrystals.

performed in N_2 for 30 min up to 900 °C. Then, Si and SiO_2 were co-evaporated simultaneously by two electron guns in a high vacuum chamber at room temperature (about 25 °C). The total deposition rate of Si and SiO_2 controlled by a quartz crystal monitor was 3 /s (Si : SiO_2 = 1 : 4), and the film thickness was 5 nm. Subsequently, a 3 nm SiO_2 layer was deposited by e-beam evaporation as a middle insulation layer. After deposition, the sample was annealed to make Si crystallize in N_2 ambient at 900 °C for 60 min. After this step, the top Ni nanocrystals were formed by self assembly in which 2 nm wetting layers were deposited by electron beam evaporation. The thickness of the thin metal layer was monitored by a quartz crystal oscillator. RTA (rapid thermal annealing) under a certain temperature was carried out in N_2 ambient to induce the formation of Ni nanocrystals. Figure 2(a) shows a plan view transmission electron microscopy (TEM) micrograph of the sample with single-layer Si nanocrystals annealed in N_2 at 900 °C for 60 min. The inset shows the clear lattice fringes of the Si nanocrystals, indicating that the crystallinity of the nanocrystals is good and Si nanocrystals with the grain size of about 6 nm are uniformly dispersed in the amorphous matrix (SiO_2). Figure 2(b) shows a top view scanning electron microscopy (SEM, Hitachi S-4700) image of the Ni nanocrystals on the tunneling oxide before the subsequent gate stack processes. The number density is approximately 2×10^{12} cm^{-2} and the average size is 5 nm. Then a layer of 30 nm SiO_2 as control oxide was deposited by e-beam evaporation. Finally, 300 nm aluminum top electrodes were evaporated by a

Table 1. Design of experiments for a heterogeneous nanocrystal MOS capacitor.

MOS capacitor	Tunneling oxide (nm)	Nanocrystal	Control oxide (nm)
a	3	-	30
b	3	Si	30
c	3	Ni	30
d	3	Si and Ni	30

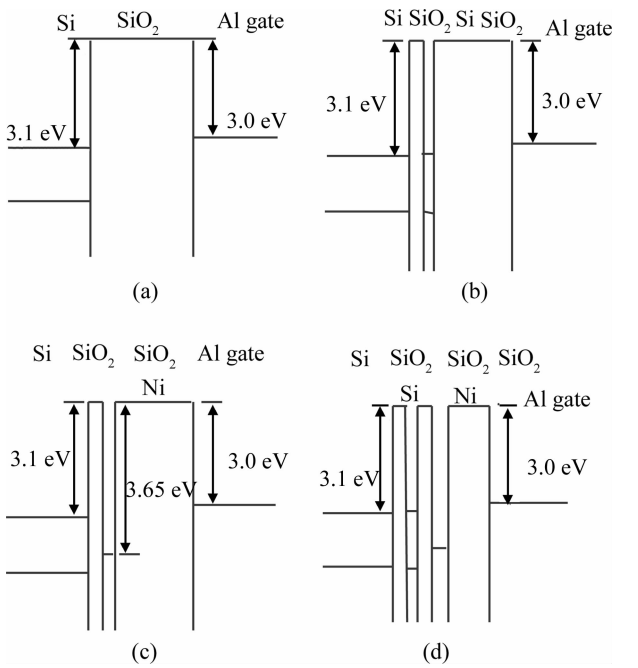

Fig. 3. Energy band diagrams of (a) control oxide, (b) Si nanocrystals, (c) Ni nanocrystals, and (d) Ni and Si nanocrystals.

circle-shaped shadow mask and bottom electrode on the backside. The gate area is 2×10^{-3} cm^{-2}. The control samples without nanocrystals and with single-layer Ni/Si nanocrystals were fabricated by the same process. Capacitance versus voltage measurements were made with a semiconductor parameter analyzer (HP 4284A). The charge retention performance was also studied through transient capacitance (*C–t*) testing techniques.

3. Results and discussion

Four MOS capacitor structures were fabricated in the design of the experiments: (a) control oxide without nanocrystals, (b) with Si nanocrystals, (c) with Ni nanocrystals, and (d) with Si and Ni nanocrystals, as shown in Table 1. Energy band diagrams are illustrated in Fig. 3, where the conduction band offsets of Si and Ni nanocrystals from SiO_2 are estimated to be 3.1 eV and 3.65 eV, respectively. The dominant charge injection mechanism to the Si and Ni nanocrystals is direct tunneling through the thin oxide in Fig. 3.

The *C–V* curves obtained at different and the same scanning voltage ranges are respectively shown in Figs. 4(a) and 4(b). The hysteresis loops follow a counter-clockwise direction, because charge transfer can only happen across the

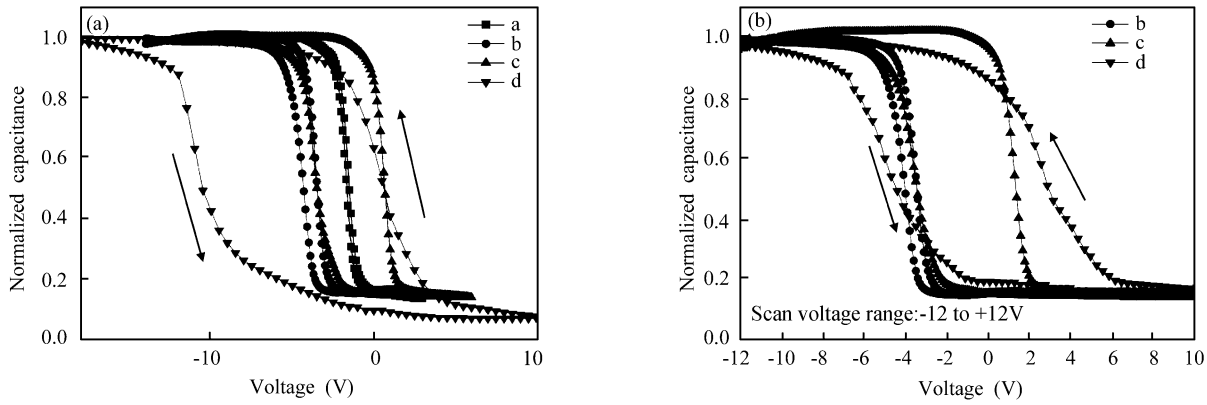

Fig. 4. High frequency *C*–*V* curves of MOS capacitors a–d in Table 1 at (a) different scanning voltage ranges and (b) the same scanning voltage ranges.

Table 2. Charge characteristics of different MOS capacitor structures under different scan voltage ranges.

	MOS (b)	MOS (c)	MOS (d)
ΔV_{FB} (V)	1.2	5.1	10.2
Stored charge (C/cm^2)	1.43×10^{-7}	2.12×10^{-7}	5.52×10^{-7}
Electrode area (cm^2)	2×10^{-3}	2×10^{-3}	2×10^{-3}

Table 3. Comparision of stored charges for MOS capacitance with double-layer homogeneous Si nanocrystals and Au nanocrystals embedded with our sample.

Nc	Nc size	Tunneling barrier and interlayer barrier	Control barrier	Stored charges (10^{-7}C/cm^2)
Si[16]	10 nm for upper layer and 5 nm lower layer	5 nm and 5 nm SiN_x	30 nm SiN_x	3.69
Au[15]	7 nm for the upper and lower layer	2–3 nm and 5 nm SiO_2	32 nm SiO_2	2.81
Si and Ni	5 nm for upper layer and 6 nm lower layer	3 nm and 3 nm SiO_2	30 nm SiO_2	5.52

tunneling oxide, not the control oxide in our samples. As shown in Fig. 4(a), the *C*–*V* curve of the control sample (a) exhibits negligible hysteresis, which confirms the good quality of the oxide. Therefore, it is conjectured that the memory effect of the design splits mainly results from charge injection into the nanocrystals. The MOS capacitor with embedded Si nanocrystals (b) shows a flat band voltage shift (ΔV_{FB}) in the scanning voltage range of –14 to +2 V, where ΔV_{FB} is around 1.2 V. Compared to the MOS capacitor (b), the MOS capacitor with embedded Ni nanocrystals (c) exhibits better charge storage capacity, where ΔV_{FB} in the scanning voltage range of –10 to +6 V is 5.1 V. This is attributed to the thin tunneling oxide, the enhanced electric field[14], the deep potential well, and the large tunneling cross section of Ni nanocrystals. Moreover, ΔV_{FB} of the MOS capacitor with embedded double-layer heterogeneous nanocrystals of Si and Ni can be further increased to 10.2 V by an additional Ni nanocrystal layer in the scanning voltage range of –18 to +10 V. By increasing the scanning voltage range, the charges can be delivered to Ni nanocrystals through direct tunneling. The ratios of the flat band shift to the absolute value of the scanning voltage range ($\Delta V_{FB}/|\Delta V_G|$) are b < c < d. Moreover, the charge density in the nanocrystal layer can be extracted and compared in Table 2 by the relation:

$$\Delta V_{FB} \approx \frac{Q_t}{C_{ox}}, \tag{1}$$

where Q_t is the trap charge density, and C_{ox} is estimated directly from the measured accumulation capacitance. Furthermore, as shown in Fig. 4(b), the flat band shifts under a ±12 V bi-director sweep are also b < c < d, and are 1, 5, and 8 V, respectively. These results both confirm that the MOS capacitor with double-layer heterogeneous nanocrystals can trap more charges, which is advantageous for nonvolatile memory applications. When compared with the stored charges for the MOS capacitor with double-layer homogeneous Si nanocrystals and Au nanocrystals embedded with our sample[15, 16], the charge storage capacity of the MOS capacitor structure with double-layer heterogeneous nanocrystals consisting of Si and Ni metal embedded is enhanced, as summarized in Table 3. All the measurements are performed at room temperature. With comparable device parameters, the MOS capacitor with double-layer heterogeneous nanocrystals embedded in this work shows a better charge storage capacity than that with double-layer homogeneous nanocrystals embedded, which is probably due to the higher number density of nanocrystals of our sample, which is related to the amount of stored charges in a

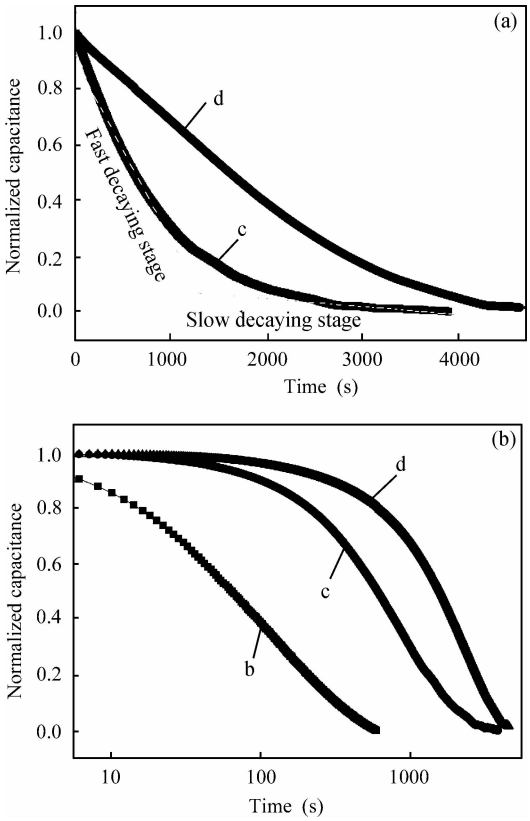

Fig. 5. Normalized capacitance versus time for MOS capacitor structures c and d in Table 1, where (a) and (b) correspond to linear and semi-logarithmic plots.

given area.

In order to investigate the charge retention capacity of the MOS capacitor with double-layer heterogeneous nanocrystals, a capacitance versus time (C–t) measurement was performed. The MOS capacitors b, c and d in Table 1 were first charged for 60 s at a bias voltage of 12 V. Then, the capacitance decay measurements were carried out at flat band bias voltage of –1 V for the samples with single-layer Si/Ni nanocrystals and double-layer Si and Ni nanocrystals. Figure 5 displays the normalized capacitance-time curves. As shown in Fig. 5(a), after a period of time, the capacitances of the two MOS capacitors c and d are reduced by some certain, suggesting that the electrical state of the MOS capacitor is altered. Since a higher capacitance corresponds to the electron charged state of the nanocrystals and a lower capacitance corresponds to the electron discharged state, the diminishing trend of the C–t curve can be translated into the charge decaying behavior of the nanocrystals. Note that the C–t plot shows obvious two-stage behavior: the initial fast decaying stage and the subsequent slow decaying stage, which can be understood as follows: when the programming process is finished at time t = 0, the charge density in the nanocrystals has its maximum value. The electrical field in the tunneling dielectrics is then strongest. As a result, the discharging current is largest and the charge loss rate is fastest at the initial stage of the retention period. With electrons tunneling out of nanocrystals, the charge density as well as the electrical field decreases. Thus, the process of charge loss becomes slower and slower. The

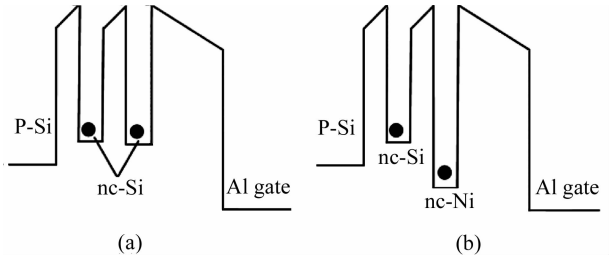

Fig. 6. Energy band diagrams of MOS capacitors with double-layer (a) homogeneous Si nanocrystals and (b) heterogenous Si and Ni nanocrystals under retention.

retention time is defined as the time taken for the capacitance to decrease to 50% of the initial value and all the data are based on the same normalized methods: $(C_t–C_s)/(C_0–C_s)C_0$ and C_s are the capacitances at the start and end of the test, respectively. From Fig. 5(b), one can see that the retention times of the MOS capacitors (b), (c) and (d) are 90 s, 600 s and 900 s, respectively. It is obvious that the retention performance of the MOS capacitors with Ni nanocrystals (c) and (d) have relatively longer retention times. Figures 6(a) and 6(b) are energy band diagrams of MOS capacitors with double-layer homogeneous Si nanocrystals and heterogeneous Si and Ni nanocrystals under retention respectively. Also,the dominant charge injection mechanism for the Si nanocrystals and Ni nanocrystals is direct tunneling through the thin oxide and interlayer oxide. On one hand, due to the thicker tunneling oxide of upper nanocrystals, direct tunneling from the upper Ni nanocrystals to the substrate is suppressed, and because the 3D confined spherical nanocrystals are isotropic, Coulomb blockade and energy level quantization limits the leakage mechanism that is tunneling to the closest lower nanocrystals[15]. On the other hand, the Ni conduction band in Fig. 3(d) has a barrier height (0.55 eV) greater than that of Si, so for sample d direct tunneling from the upper Ni nanocrystals to the lower Si nanocrystals becomes more difficult with respect to the MOS capacitor with homogeneous double-layer Si nanocrystals under retention, as shown in Fig. 6. Therefore, it can be seen that double-layer heterogeneous nanocrystals are advantageous in the retention characteristic.

4. Conclusion

An MOS capacitor employing Ni and Si nanocrystals as a floating gate, prepared by electron beam evaporation combined with annealing, has been fabricated for nonvolatile memory applications. From the comparison of four MOS capacitor structure design splits, (a) control oxide without nanocrystals; (b) with Si nanocrystals; (c) with Ni nanocrystals; (d) with Si and Ni nanocrystals, the role of Ni nanocrystals in larger flat voltage shifts and longer retention times can be clearly observed.

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