Method of simulation of low dose rate for total dose effect in 0.18 μm CMOS technology

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Abstract: Three methods for simulating low dose rate irradiation are presented and experimentally verified by using 0.18 μm CMOS transistors. The results show that it is the best way to use a series of high dose rate irradiations, with 100 °C annealing steps in-between irradiation steps, to simulate a continuous low dose rate irradiation. This approach can reduce the low dose rate testing time by as much as a factor of 45 with respect to the actual 0.5 rad (Si)/s dose rate irradiation. The procedure also provides detailed information on the behavior of the test devices in a low dose rate environment.

Key words: off-state leakage current; total dose effect; low dose rate; simulation method

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1. Introduction

Because the radiation effect at low dose rates is a slow progress if the low dose rate testing is done in the ground laboratory, the test is time consuming and expensive. So, in order to reduce the overall testing time, in this paper three methods for simulating low dose rates are studied by the application of analytical techniques coupled with simple measurements and by comparing the simulation results with an actual continuous low dose rate irradiation.

2. Experimental approach

The radiation samples used in this work are SMIC 0.18 μm process CMOS transistors, which employ shallow trench isolation technology. Two types of transistors were chosen: type A has a 4 nm gate oxide with W/L = 5/0.5, and type B has a 4 nm gate oxide with W/L = 10/10. All irradiations were performed using ^{60}Co sources at the Northwest Institute of Nuclear Technology, China. Four dose rates were chosen: 0.01, 0.5, 5, and 50 rad(Si)/s. The test devices were irradiated under a bias of +1.8 V on the gate and with all other terminals grounded. The samples were removed from the ^{60}Co sources for electrical measurements, and I–V curves were collected with a computer controlled HP4156A precision semiconductor parameter analyzer. The 100 °C anneal tests after high dose rate irradiation were performed under a bias in an oven.

3. Experimental results

Representative subthreshold current characteristics for a transistor from the 0.18 μm process are shown in Fig. 1 following various total dose levels. The irradiation was performed at a high dose rate (50 rad(Si)/s) with the gate biased at 1.8 V with respect to the other terminals, and the I–V characteristics were measured at V_D = 0.1 V. The lack of a parallel shift or a stretchout of the I–V characteristics as a function of the dose

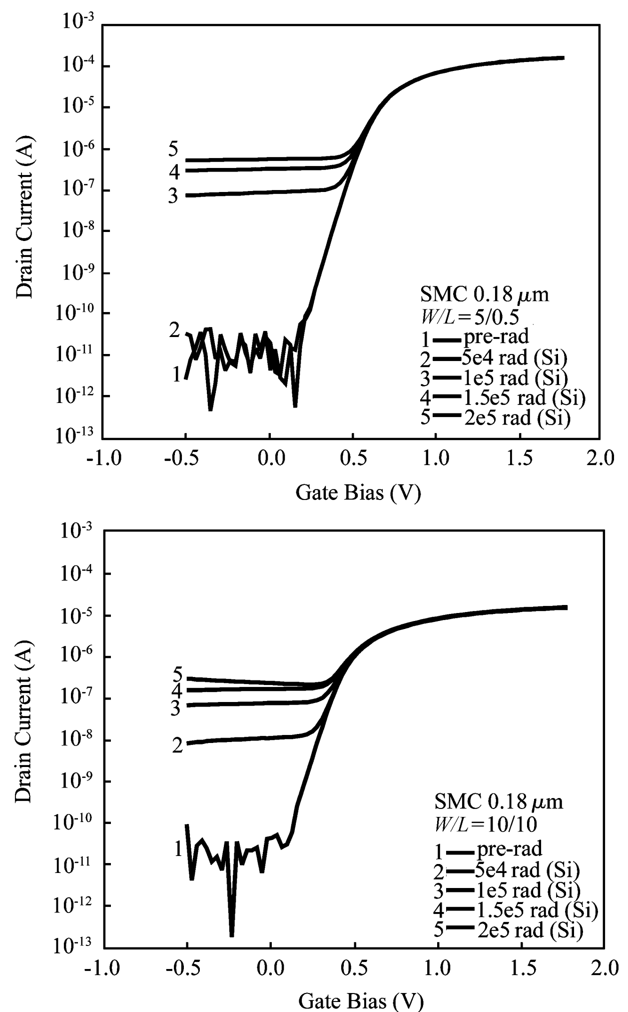

Fig. 1. Dependence of subthreshold current characteristics on the total dose for a 0.18 μm device.

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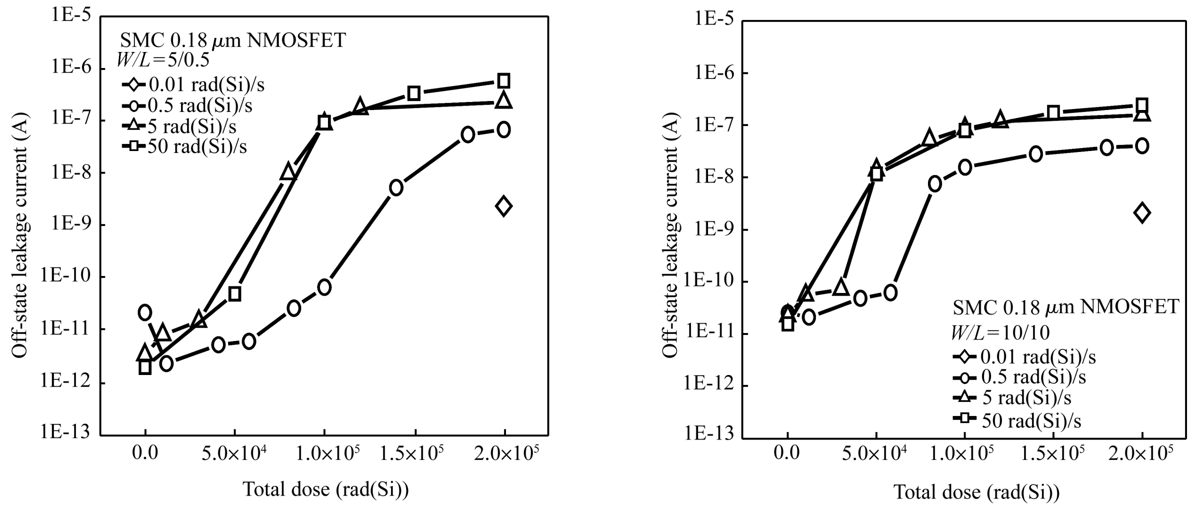

Fig. 2. Off-state leakage current versus total dose under different dose rate irradiations.

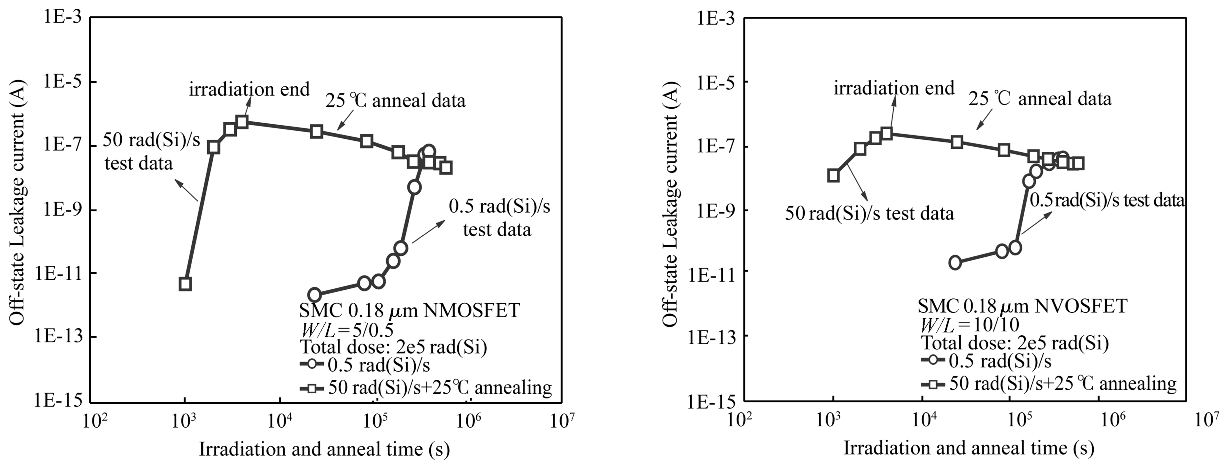

Fig. 3. Comparison of single HDR + room temperature annealing with continuous low dose rate irradiation at 0.5 rad(Si)/s.

indicates a negligible buildup of oxide-trapped charge or interface traps in the thin gate oxide[1]. This means that the radiation-induced threshold voltage has essentially vanished. This leaves field oxide isolation structures as the main remaining total dose problem. A gate bias of 0 V corresponds to the off-state operation of the transistor. Radiation-induced charge buildup in the field oxide causes the off-state leakage current to increase sharply. This leakage current is the focus of this work.

Figure 2 compares the off-state leakage currents of n-channel transistors from the 0.18 μm process for different dose rates. The radiation responses of different dose rates are different under the same absorbed dose. This demonstrates that the interaction of oxide trap generation, oxide trap annealing, and interface state formation have a significant effect on the off-state leakage current as a function of the dose rate. The failure dose at low dose rates would occur at a much higher total dose than at high dose rate irradiation. How to quantify this improvement is one of the objectives of this paper.

4. Simulation results

In order to reduce the overall testing time and the ^{60}Co pool occupation, we considered three methods of simulating the low dose rate by the application of analytical techniques coupled with simple measurements[2, 3] in this paper. The methods were: (a) Single high dose rate (HDR) irradiation followed by room temperature annealing; (b) Single high dose rate (HDR) irradiation followed by 168 h 100 °C annealing, for example the MIL-STD-883F 1019.6 method[4, 5]; (c) Multiple small total dose and high dose rate (HDR) irradiation followed by 100 °C annealing. This paper takes the 0.5 rad(Si)/s irradiation effect as an example to explain the simulation process, and the simulation results from three methods are compared to the actual continuous low dose rate irradiation.

4.1. Single HDR and room temperature annealing method

Radiation testing is often performed using ^{60}Co sources with a dose rate in the range from 50 to 300 rad(Si)/s. The question arises of whether testing performed at specific dose rates in this range can yield useful information on test device responses in a lower dose rate environments. To address this question, it is necessary to properly take into account the effects of annealing on the device response. Figure 3 shows the simulation results from two different irradiation procedures. One approach is a continuous low dose rate irradiation at a

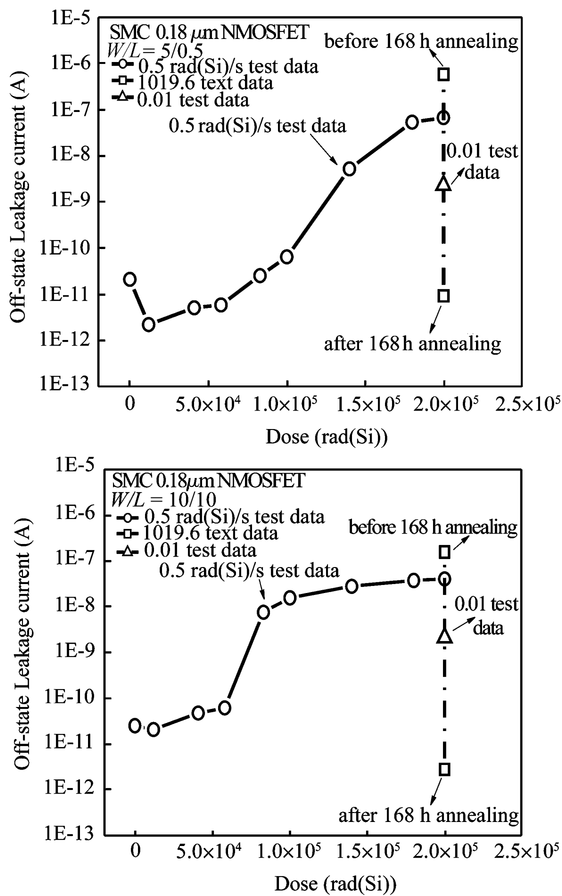

Fig. 4. Comparison of single HDR + 100 °C 168 h annealing with continuous low dose rate irradiation at 0.5 rad(Si)/s.

total dose of 0.5 rad(Si)/s to 2×10^5 rad(Si). The second approach is a single high dose rate irradiation using a total dose of 2×10^5 rad(Si) followed by room temperature annealing. Figure 3 demonstrates that, if the absorbed dose is the same, the consumption time of single high dose rate (HDR) irradiation followed by room temperature annealing is the same as that of a continuous low dose rate irradiation.

The single HDR and room temperature annealing method only reduces the ^{60}Co pool occupation time; it does not shorten the experimental period. It takes as much time as an actual low dose rate irradiation.

4.2. Single HDR + 100 °C 168 h annealing method

The MIL-STD-883F method 1019.6[4, 5] is a standard test sequence to evaluate the radiation response of CMOS devices and circuits for use in a space environment in the absence of a detailed knowledge about likely failure mechanisms. The procedure includes separate test sequences for the effects of radiation-induced oxide-trapped charge and interface traps on the device performance. The interface traps tends to moderately increase the edge-leakage current associated with the positive oxide-trapped charge. The procedure does not provide detailed time dependent response information, but just gives a conservative result. Figure 4 shows the test data for 0.5 and 0.01 rad(Si)/s irradiations with the simulation result from a single HDR and 100 °C 168 h annealing method. From the figure, we see that the pre-anneal and post-anneal off-state leakage currents bracket the actual low dose rate values. Furthermore, the post-anneal data are smaller than those from the 0.5 and 0.01 rad(Si)/s irradiations. Thus, the single HDR and 100 °C 168 h anneal method will underestimate the off-state leakage current of test devices in a low dose rate irradiation environment. This method will greatly overestimate the ability of test devices to tolerate irradiation at low dose rates.

The test period for this method is very fast, but it does not provide a complete sensitive parameter-versus-dose curve. It can only provide a conservative estimate of the low dose rate response. There is a discrepancy between the simulation result of this method and an actual low dose rate irradiation.

4.3. Multiple small total dose, high dose rate (HDR), + 100 °C annealing method

It is necessary to confirm the times of the 100 °C annealing before making use of this method to simulate the low dose rate irradiation effects. The 100 °C annealing times are derived in the following way: two samples from 0.18 μm process CMOS transistors, which had each been treated by a 5×10^4 rad(Si) total dose at a 50 rad(Si)/s high dose rate irradiation, were annealed. One sample was annealed at 25 °C, and the other was annealed at 100 °C. During the annealing process, the off-state leakage current versus the time was recorded and plotted. For a continuous low dose rate irradiation of 0.5 rad(Si)/s, it takes 28 h to reach a total dose of 5×10^4 rad(Si). Comparing the sample, which was annealed at 25 °C for 28 h (the same off-state leakage current as the continuous low dose rate irradiation), to the sample annealed at 100 °C, the result shows that the same off-state leakage current occurred within 20 min of the 100 °C annealing. Thus, an annealing factor of 20 min per 5×10^4 rad(Si) was chosen.

Figure 5 compares the off-state leakage current for low dose rate irradiation at 0.5 rad(Si)/s to the off-state leakage current for a stepwise 5×10^4 rad(Si) high dose rate (50 rad(Si)/s) irradiation with the 20 min 100 °C annealing after each radiation. The curves match very well. Thus, this is a viable simulation method. This approach saves significant time, i.e., 2.44 h versus 111 h for a 2×10^5 rad(Si) irradiation. Before the low dose rate simulation is run, a short experiment must be performed to determine the optimum high temperature annealing time step. Small dose steps correspond to smaller time steps in this simulation. A high temperature annealing between irradiation steps reduces the time required for the simulation. The total dose step may be almost any size in this method.

The period of this simulation method is very short; furthermore, it can provide a complete sensitive parameter-versus-dose curve. The authors propose this method to simulate low dose rate irradiation.

5. Conclusion

Three methods of simulating low dose rate irradiation effects in 0.18 μm CMOS technology were studied in this pa-

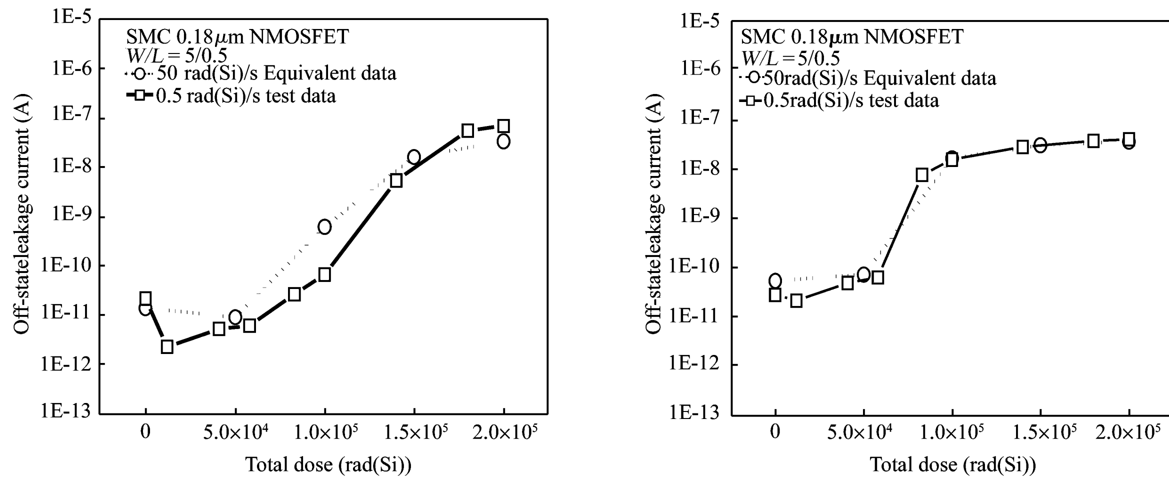

Fig. 5. Comparison of multiple small total dose, high dose rate (HDR), + 100 °C annealing with continuous low dose rate irradiation at 0.5 rad(Si)/s.

per and verified by continuous low dose rate irradiation at 0.5 rad(Si)/s. The results show that a series of high dose rate irradiation followed by a high temperature annealing method not only reduces the overall testing time and the ^{60}Co pool occupation, but also provides the detailed time dependent response information on sensitive parameters. The time saving is significant, 45 : 1, for example, 2.44 h versus 111 h for 2×10^5 rad(Si) total dose irradiation. The authors propose this method to simulate low dose rate irradiation.

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