Modeling and analysis of single-event transients in charge pumps*

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Abstract: It has been shown that charge pumps (CPs) dominate single-event transient (SET) responses of phase-locked loops (PLLs). Using a pulse to represent a single event hit on CPs, the SET analysis model is established and the characteristics of SET generation and propagation in PLLs are revealed. An analysis of single event transients in PLLs demonstrates that the settling time of the voltage-controlled oscillators (VCOs) control voltage after a single event strike is strongly dependent on the peak control voltage deviation, the SET pulse width, and the settling time constant. And the peak control voltage disturbance decreases with the SET strength or the filter resistance. Furthermore, the analysis in the proposed PLL model is confirmed by simulation results using MATLAB and HSPICE, respectively.

Key words: single event transient; charge pump; phase-locked loop
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1. Introduction

The radiation-induced single-event transient (SET) phenomenon has been identified as the primary failure mechanism behind several spacecraft malfunctions in recent years. SET is a kind of single-event effect, caused by the strike of a single energetic particle originating from sources including galaxies, the sun, the natural decay of trans-uranic materials, and so on. The energy deposited by a particle strike in a critical region of the device PN junction generates electron–hole pairs, which are transported and collected at the junction, leading to a transient current pulse on the struck node. As technology feature sizes decrease, SETs start to dominate the radiation effects of microcircuits while circuits become sufficiently fast, power supplies become sufficiently low, node capacitances become sufficiently small and clock frequencies become sufficiently high[1].

Previous works have shown that a single ion striking a phase-locked loop (PLL) can deposit enough charge to change the PLL output significantly[2−5]. Charge pumps (CPs) and voltage-controlled oscillators (VCOs) are critical blocks in PLLs and are most sensitive to single event transients[2−7]. Laser tests show that the maximum number of faulty (missing or additional) clock pulses in the output of the PLL due to strikes in CPs is at least one order of magnitude greater than that induced by strikes occurring in any other PLL block[3].

In space applications, CP circuits are exposed to radiation, which can have a significant effect on the system. A single event strike in the output of the charge pump may produce a large voltage swing on the loop filter (LPF). A disturbance of the voltage can cause phase and frequency shifts, resulting in the loss of the PLL frequency lock. Though the PLL can eventually recover through the feedback loop, this takes up to several microseconds, leading to data loss in communication links and function interrupts in microprocessors.

The purpose of this paper is to investigate the impact of single-event transients on the PLL operation through both theoretical analysis and simulations. An SET analysis model is established to show the resulting PLL behaviors due to single event strikes. The results of the analysis and simulations, which reveal the effects on PLL loop parameters and the SET pulse strength on the SET responses, are presented. This work will guide the design of radiation-harden PLLs.

2. Theoretical modeling and analysis of SETs

2.1. SET analysis model

The main function of a PLL is to generate a clock signal with a specific frequency. A typical PLL, as shown in Fig. 1, consists of a phase frequency detector (PFD), a CP, an LPF, and a VCO. The output of the VCO is compared with the reference clock in the PFD, and the tri-state phase detector compares the phases of the reference signal and the feedback signal to generate an error signal. The charge pump then converts the error signal pulses into analog current pulses, which are
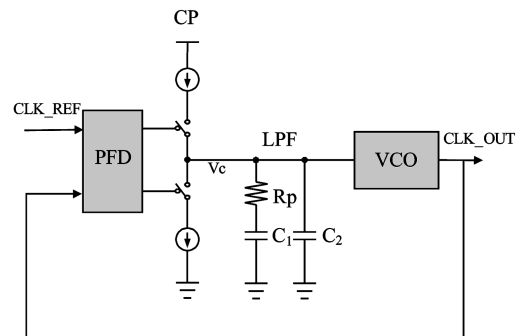

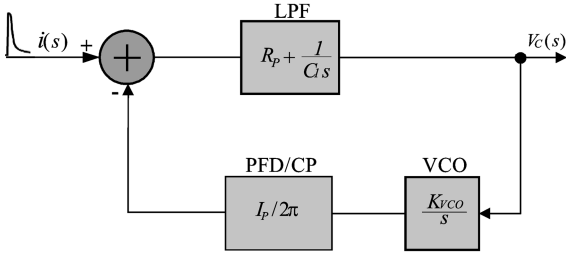Fig. 1. General block diagram of the charge pump PLL.

Fig. 2. Proposed PLL model for single event strike characterization.

averaged over time and converted to a voltage value by the passive loop filter. This voltage drives the VCO to generate a specific frequency clock.

In this work, the PLL behavior is obtained by observing the VCO control voltage V_C instead of the phase error. In fact, an instantaneous ion strike in the CP causes excess CP current, resulting in an abrupt change of V_C to influence the whole loop. And Equation (1) indicates that the response of the closed-loop system can be described by a phase change rate, a frequency change rate, or V_C versus the input frequency ω_{in}. It also reveals that it is reasonable to monitor V_C to analyze the SET response of the closed-loop PLL system, while it is difficult to simulate or measure the phase or frequency shift.

$$H(s) = \frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{\omega_{out}}{\omega_{in}}(s) = K_{VCO}\frac{V_C}{\omega_{in}}(s). \quad (1)$$

Correspondingly, the traditional PLL model is altered to reflect this emphasis. Given that all the components are linear when the PLL is locked, the CP output is taken as the input and the VCO control voltage as the output of the system to re-build the PLL loop. This new PLL model is shown in Fig. 2, where transfer function of each block is listed. $i(s)$ is the SET induced current on the output of the CP, and I_P, K_{VCO}, R_P, and C_1 are the charge pump current, VCO gain, loop filter resistance, and the loop filter capacitance, respectively. If the second capacitance C_2 is far below C_1, the closed-loop time and the frequency responses would remain relatively unchanged. So, C_2 can be neglected for simplicity.

According to the PLL structure in Fig. 2, the transfer function of the control voltage $V_C(s)$ as a function of the single event strike $i(s)$ is derived as

$$H(s) = \frac{V_C(s)}{i(s)} = \frac{\frac{1}{C_1}s(R_P C_1 s + 1)}{s^2 + \frac{I_P K_{VCO}}{2\pi C_1}R_P C_1 s + \frac{I_P K_{VCO}}{2\pi C_1}}. \quad (2)$$

When rewriting the denominator in a familiar form used in control system theory, the final transfer function of this proposed model is:

$$H(s) = \frac{\frac{1}{C_1}s(R_P C_1 s + 1)}{s^2 + 2\omega_n\zeta s + \omega_n^2}, \quad (3)$$

where the natural frequency ω_n and the damping ratio ζ are:

$$\omega_n = \sqrt{\frac{I_P K_{VCO}}{2\pi C_1}}, \quad \zeta = \frac{R_P}{2}\sqrt{\frac{I_P C_1 K_{VCO}}{2\pi}}. \quad (4)$$

2.2. Pulse response

In order to demonstrate the responses of PLLs, the SET current can be modeled as an impulse or a pulse function. Since an SET is a large-magnitude, short-duration signal, an impulse function (Dirac delta function) is a good approximation[8]. However, the impulse model cannot examine the impact of the single event strength on the PLL behavior. To achieve a more actual SET current, a rectangular current pulse with amplitude T and width I_{set} can be used to model the current[9]. The total charge deposited by a single event pulse is $I_{set}T$. And the SET current can be modeled by the difference of two identical step responses as

$$i(t) = I_{set}[u(t) - u(t - T)]. \quad (5)$$

After transforming it from the time domain to the frequency domain by applying the Laplace transformation, we get:

$$i(s) = I_{set}(1/s - e^{-Ts}/s). \quad (6)$$

Then combine Eqs. (3) and (6), we get:

$$V_C(s) = H(s)i(s) = \frac{\frac{1}{C_1}s(R_P C_1 s + 1)}{s^2 + 2\omega_n\zeta s + \omega_n^2}I_{set}(1/s - e^{-Ts}/s). \quad (7)$$

The time domain response of V_C is derived by applying the inverse Laplace transformation. Since the value of ζ can affect the poles of the system, the time domain response of V_C is dependent on ζ. In this work, the damping ratio ζ is chosen to be larger than 0.707 to ensure the stability of the PLLs. So, the real range of ζ is $\zeta \geqslant 0.707$.

Derive the SET responses in detail. If $\zeta = 1$, the time domain response is

$$V_C(t) = I_{set}R_P \left\{ e^{-\omega_n t}(1 - \frac{\omega_n C_1 - 1/R_P}{C_1}t)u(t) \right.$$
$$\left. -e^{-\omega_n(t-T)}\left[1 - \frac{\omega_n C_1 - 1/R_P}{C_1}(t - T)\right]u(t - T)\right\}. \quad (8)$$

And if $\zeta > 1$,

$$V_C(t) = I_{set}e^{-\zeta\omega_n t}[R_P\cosh(At) + B\sinh(At)]u(t) -$$
$$I_{set}e^{-\zeta\omega_n(t-T)}[R_P\cosh(A(t-T)) + B\sinh(A(t-T))]u(t-T), \quad (9)$$

where $A = 1/\left(C_1\sqrt{C_1^2\omega_n^2(\zeta^2 - 1)}\right)$ and $B = AC_1(1 - R_P C_1\zeta\omega_n)$.

At last, if $\zeta < 1$,

$$V_C(t) = I_{set}R_P D\left\{e^{-\zeta\omega_n t}\sin(\omega_d t + \theta)u(t)\right.$$
$$\left. -e^{-\zeta\omega_n(t-T)}\sin[\omega_d(t - T) + \theta]u(t - T)\right\}, \quad (10)$$

where $D = \dfrac{\sqrt{1/R_P^2 - (2\omega_n\zeta C_1)/R_P + \omega_n^2 C_1^2}}{\omega_n C_1\sqrt{1 - \zeta^2}}$ and $\omega_d = \omega_n\sqrt{1 - \zeta^2}$.
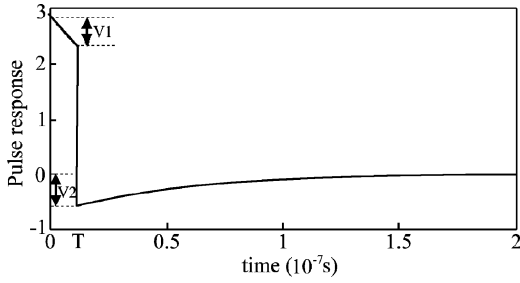
Fig. 3. Pulse SET response of the control voltage V_C.

Combining Eqs. (8)–(10), we obtain the uniform time domain response of V_C as follows.

$$V_C(t) = I_{set}R_P \left(e^{-\zeta\omega_n t} f_\zeta(t) - e^{-\zeta\omega_n(t-T)} f_\zeta(t-T) \right), \qquad (11)$$

where the expression $f_\zeta(t)$ varies with the value of ζ.

2.3. Analysis of the SET response

Equation (11) indicates that the time domain response of V_C depends on the constant $I_{set}R_P$, the exponential decay term $e^{-\zeta\omega_n t}$, the function $f_\zeta(t)$ and the interval T between two current steps.

A typical pulse response of the control voltage V_C is shown in Fig. 3. When $t = 0$, V_C achieved the peak voltage deviation ($\zeta < 1$) or almost achieved the peak ($0.707 \leqslant \zeta < 1$). And within the duration of $0 \leqslant t < T$, only one current step acts on the control voltage, whose time domain response is $I_{set}R_P e^{-\zeta\omega_n t} f_\zeta(t)$. V_C decays at a rate of $e^{-\zeta\omega_n t} f_\zeta(t)$ from the peak voltage. When $t = T$, the second current step influences V_C as the difference of the two current steps, and V_C falls to the minimum voltage V_{C_MIN}. After that, the PLL locks again with V_C recovering to its initial value.

According to Eqs. (8)–(10), if $\zeta \geqslant 1$, $f_{\zeta \geqslant 1}(0) = 1$ and $f_{\zeta \geqslant 1}(-T) = 0$; and if $0.707 \leqslant \zeta < 1$, $f_{0.707 \leqslant \zeta < 1}(0) \approx 1$ and $f_{0.707 \leqslant \zeta < 1}(-T) = 0$. Therefore, the peak voltage deviation of V_C is $V_{C\_MAX} \approx V_C(0) \approx I_{set}R_P$, implying that V_{C_MAX} is dominated by the SET pulse amplitude I_{set} and the loop filter resistance R_P. Similarly, V_{C_MIN} can be calculated as $V_{C\_MIN} \approx V_C(T) \approx I_{set}R_P \left(e^{-\zeta\omega_n T} f_\zeta(T) - 1 \right)$, where I_{set} and R_P both impact V_{C_MIN}.

The settling time of the control voltage disturbance, during which V_C recovers to its final value and the PLL reobtains its lock, is an important factor for radiation-harden PLLs. The whole disturbing duration of V_C can be divided into two decay stages. In the first stage, V_C decays from V_{C_MAX} to V_{C_MIN} within the time T and in the second stage V_C decays from V_{C_MIN} to the final value. The initial values of the two stages are subjected to $I_{set}R_P$. Therefore, as V_{C_MAX} increases, the settling time of V_C will increase. The pulse width T affects the settling time in two ways. On the one hand, the increased T will prolong the duration of a single event. On the other hand, an increased T will increase the absolute value of V_{C_MIN}. So, the settling time will increase with T. In addition, the settling time is determined by $\zeta\omega_n$ because of the exponential decay term $e^{-\zeta\omega_n t}$. In other words, the larger the settling time constant $\zeta\omega_n$ is, the smaller the settling time will be.
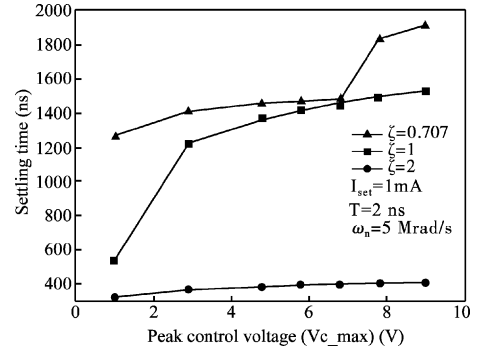

Fig. 4. Settling time versus peak control voltage deviation for $\zeta < 1$, $\zeta = 1$, and $\zeta > 1$.
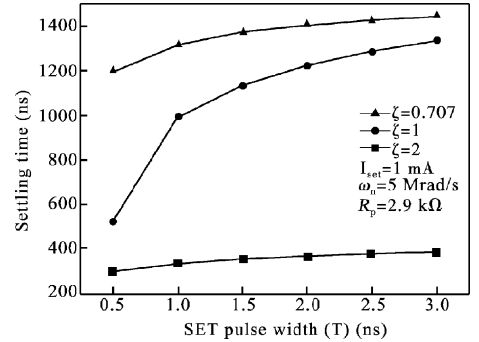

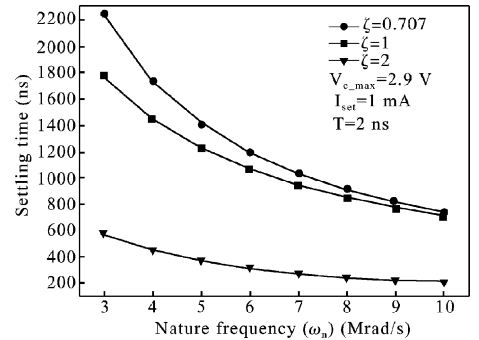Fig. 5. Settling time versus SET pulse width for $\zeta < 1$, $\zeta = 1$, and $\zeta > 1$.

Fig. 6. Settling time versus natural frequency for $\zeta < 1$, $\zeta = 1$, and $\zeta > 1$.

In a word, the settling time depends on the peak control voltage deviation V_{C_MAX}, the SET pulse width T, and the settling time constant $\zeta\omega_n$; V_{C_MAX} is dominated by the SET pulse amplitude I_{set} and the loop filter resistance R_P.

3. MATLAB simulation results

In order to validate the conclusions from the last section, transient V_C responses to SET are simulated with MATLAB. An SET response analysis program is developed, which does four steps: deriving the loop parameters, calculating the V_C time domain responses based on Eq. (7), calculating the V_C settling time, and formatting the output results. The functions of the settling time versus the loop parameters and the SET strength are obtained as described below.

The settling time of the VCO control voltage caused by a single event strike as calculated using Eq. (7) is plotted in Fig. 4 to Fig. 6. Settling time is a function of the peak control
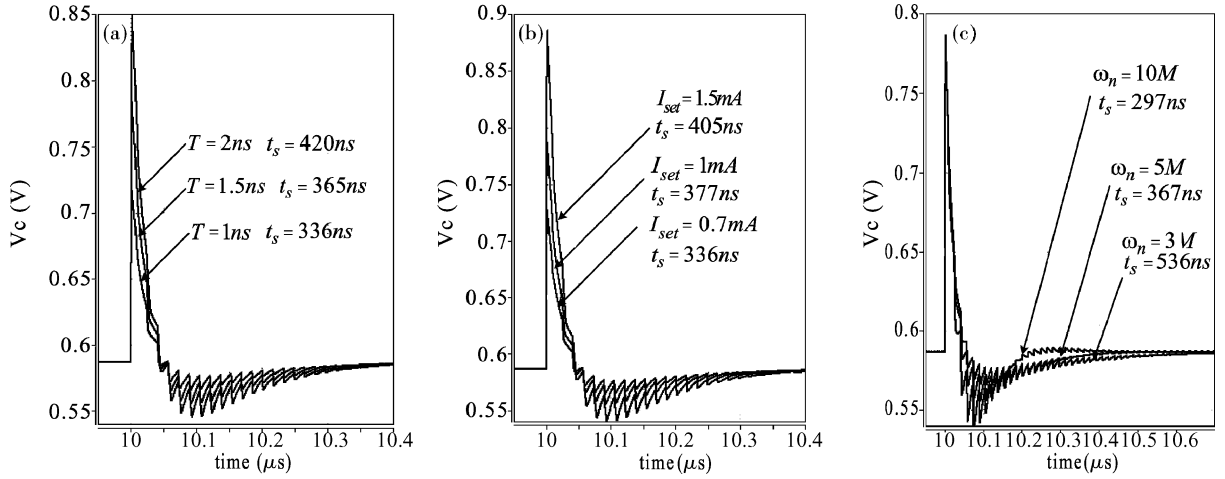
Fig. 7. (a) Transient V_C response obtained by circuit simulation as a function of SET pulse width T; (b) Transient V_C response obtained by circuit simulation as a function of SET pulse amplitude I_{set}; (c) Transient V_C response obtained by circuit simulation as a function of settling time constant $\zeta\omega_n$.

voltage deviation with fixed I_{set}, T, and ω_n, as shown in Fig. 4. In each single curve ($\zeta < 1$, $\zeta = 1$ and $\zeta > 1$), the settling time increases with the peak voltage. In addition, for the same peak control voltage, the settling time varies with different ζ. Obviously, the settling time is smaller for a larger ζ. And the change rate of the settling time falls to the smallest for the curve with $\zeta = 2$. It is also proven that a larger $\zeta\omega_n$ is good for a fast convergence when the natural frequency is kept constant.

The settling time with varying SET pulse width T for $\zeta < 1$, $\zeta = 1$, and $\zeta > 1$ is shown in Fig. 5, which proves that the settling time increases as the pulse width is increased or $\zeta\omega_n$ is decreased. The longer recovery time is attributed to the wider SET pulse, which deposits more charge into the CPs.

Both ω_n and ζ have an influence on the settling time. As Figure 6 shows, the settling time is a function of the natural frequency for $\zeta < 1$, $\zeta = 1$, and $\zeta > 1$. As ω_n increases, the settling time decreases. And, for the same ω_n, the settling time decreases with increasing ζ. Furthermore, it validates that the exponential decay term $\mathrm{e}^{-\zeta\omega_n t}$ determines the decay process.

4. Circuit simulation results

Transistor level simulations are performed using current pulse stimuli to represent single event strikes to investigate single event transients in CPs within a PLL system. The PLL circuits operating at 1.5 GHz are designed using a 180-nm CMOS process. A current pulse is injected into the charge pump after the PLL gets locked. The circuit simulation is carried out with the Synopsys circuit simulator HSPICE.

As analyzed in the previous section, the VCO control voltage disturbance resulting from the single event strike depends on the PLL loop parameters and the SET strength. Transient simulations confirm this conclusion as shown in Fig. 7. The settling time t_s is listed for the corresponding curves. It can be seen that the recovery time due to SET strikes decreases as the SET pulse width T or the amplitude I_{set} decreases, or as the settling time constant $\zeta\omega_n$ increases. However, the peak control voltage is also affected by the pulse width T, as ob-

served in Fig. 7(a), which is different from the conclusion from the theoretical analysis. Because of the filter capacitance C_2 and parasitic capacitances in the real loop filter, the voltage cannot be changed instantly, implying that a smaller T achieves a smaller peak voltage. Therefore, the peak control voltage deviation depends on the SET pulse width, too. Except for this point, the transient simulations agree with the theoretical analysis.

5. Conclusion

This paper investigates the effects of single-event transients in charge pumps. Based on the relationship between the VCO control voltage and the SET induced current, the SET analysis model is established by means of pulse response to analyze the effects of SETs in CPs. The analysis results indicate that the settling time is proportional to the single event pulse width T and the peak control voltage deviation V_{C_MAX}, and is inversely proportional to the settling time constant $\zeta\omega_n$. These results also show that V_{C_MAX} is dominated by the SET pulse amplitude I_{set} and the loop filter resistance R_P.

The proposed model and conclusions are confirmed by simulations done using MATLAB and HSPICE, except that the peak control voltage also depends on the SET pulse width T. Therefore, in order to mitigate the SET effects, the loop parameters, such as R_P, ζ, and ω_n, should be optimized according to the SET strength. This study is beneficial for the design of radiation-harden PLLs.

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