A low-noise PLL design achieved by optimizing the loop bandwidth*

Bai Chuang(白创)†, Zhao Zhenyu(赵振宇), and Zhang Minxuan(张民选)

(School of Computer, National University of Defense Technology, Changsha 410073, China)

Abstract: This paper describes a low-noise phase-locked loop (PLL) design method to achieve minimum jitter. Based on the phase noise properties extracted from the transistor, and the low-pass or high-pass transfer characteristics of different noise sources to the output, an optimal loop bandwidth design method, derived from a continuous-time PLL model, further improves the jitter characteristics of the PLL. The described method not only finds the optimal loop-bandwidth to minimize the overall PLL jitter, but also achieves optimal loop-bandwidth by changing the value of the resistor or charge pump current. In addition, a phase-domain behavioral model in ADS is presented for accurately predicting improved jitter performance of a PLL at system level. A prototype PLL designed in a 0.18 μm CMOS technology is used to investigate the accuracy of the theoretical predictions. The simulation shows significant performance improvement by using the proposed method. The simulated RMS and peak-to-peak jitter of the PLL at the optimal loop-bandwidth are 10.262 ps and 46.851 ps, respectively.

Key words: continuous-time domain analysis; optimal loop bandwidth; phase-domain behavioral model; timing jitter

DOI: 10.1088/1674-4926/30/8/085011 **EEACC:** 2570

1. Introduction

Phase-locked loops (PLLs) are widely used in high speed digital systems to generate low-jitter on-chip clocks. As system speed increases, more stringent phase noise requirements are imposed on PLLs. Previously, the design of low-jitter PLL focused on reducing jitter caused by the individual PLL component. As a result, building blocks such as low-noise voltage-controlled oscillators (VCOs)[1], deadzone-free phase frequency detectors (PFDs)[2], zero-offset charge pump circuits[3], and low-noise frequency dividers have been widely studied. However, it is not well emphasized that the overall noise performance of the PLL not only depends on the design of the individual components, but also heavily depends on the choice of the loop bandwidth. Therefore, a more thorough analysis of the output jitter, taking into account optimal loop bandwidth selection, is provided in this paper. In addition, compared with the traditional computational method based on a second-order model of PLL, a new method to achieve optimum loop bandwidth, on the basis of a third-order model, by changing the value of the resistor or CP current, is shown here. Behavioral model analysis in ADS has been investigated with its fast-simulation advantage. Thus, a linear phase-domain behavioral model is also proposed here to predict improved phase noise, proving the correctness of the optimal loop-bandwidth design method.

In this paper, the detailed theoretical background of the loop bandwidth analysis is given and a low-noise PLL design example obtained from the proposed optimization method is shown. Section 2 reviews major PLL noise sources and their characteristics, and extracts the relationship between the overall phase noises at the PLL output clock, then presents the bandwidth optimization method based on phase noise analysis in the case of a charge-pump-based PLL. In Section 3, according to optimal loop-bandwidth, circuit parameters are re-derived to improve the noise performance of the PLL while maintaining good stability. Section 4 proposes a linear phase-domain behavioral model to predict noise performance on the basis of actual circuit implementations. Section 5 describes the implementation of the PLL and jitter simulation. Experimental results are compared to verify our analysis in Section 2. Finally, conclusions are drawn in Section 6.

2. PLL phase noise analysis

The overall noise performance of a PLL depends not only on the choice of the loop bandwidth, but also on the performance of the individual components in a PLL. Therefore, the first step in reducing the overall noise of the PLL should be to identify the components generating noise in the PLL. This section begins with a brief discussion on PLL noise sources and their characteristics.

The major noise sources[4] of the charge-pump PLL include frequency divider noise, charge pump noise, low-pass filter noise and VCO internal noise. It has been proven that the excess noise of the frequency divider and charge pump can be modeled as an additive $1/f$ noise[5], which is the foremost part of them, and the corresponding transfer functions of each noise source to the output express low-pass characteristics. VCO noise and equivalent low-pass filter noise mainly have $1/f^2$ noise characteristics[6], which is also of high concern, and the corresponding transfer functions of each noise

* Project supported by the National Natural Science Foundation of China (No. 60873212).

† Corresponding author. Email: abc121384.student@sina.com

Received 16 December 2008, revised manuscript received 23 March 2009

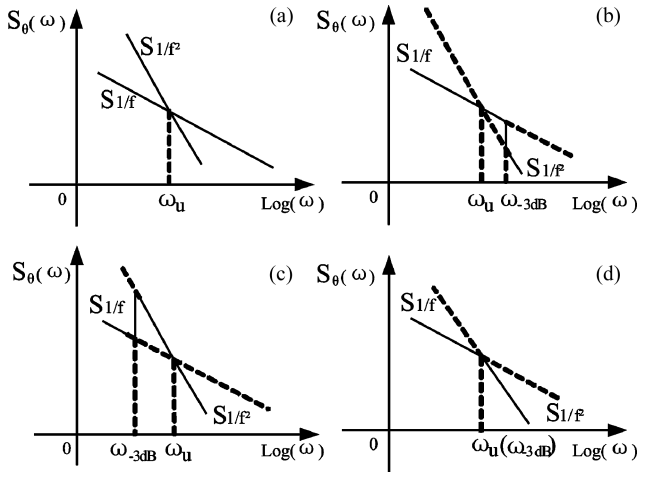

Fig. 1. (a) Power spectral density of phase noise from $1/f$ and $1/f^2$ noise sources; (b) Power spectral density of phase noise when the loop bandwidth is large; (c) Power spectral density of phase noise when the loop bandwidth is small; (d) Optimal power spectral density of phase noise. All power spectral densities of phase noise above are simplified.

source to the output express high-pass characteristics.

$$S_{\mathrm{TOT}} = S_{\mathrm{N}}\left|\frac{G}{1+GH}\right|^2 + S_{\mathrm{CP}}\left(\frac{1}{K_{\mathrm{CP}}}\right)^2\left|\frac{G}{1+GH}\right|^2 + S_{\mathrm{R}}\left|\frac{K_{\mathrm{VCO}}}{S}\frac{1}{1+GH}\right|^2 + S_{\mathrm{VCO}}\left|\frac{1}{1+GH}\right|^2,$$

where S_{TOT} is the total noise power at the output, and S_{N}, S_{CP}, S_{R} and S_{VCO} are the noise power from individual components respectively. G and H are the forward and feedback transfer functions.

It is obvious that the contribution of each noise source to the output depends on the transfer function from that noise to the output. It can also be said that the overall output phase noise varies with different –3dB bandwidth of transfer functions.

As mentioned above, the four noise sources can be easily divided into two groups, which have $1/f$ noise and $1/f^2$ noise characteristics respectively, as shown in Fig. 1(a). Their transfer functions (H_{L} and H_{H}) are low-pass and high-pass functions respectively.

If the loop bandwidth is large, the PLL has a large reduction in $1/f^2$ noise, but cannot have a good suppression of $1/f$ phase noise, as shown in Fig. 1(b). If the loop bandwidth is small, the PLL can have a large $1/f$ noise reduction, as shown in Fig. 1(c), but leaves much of the $1/f^2$ noise unreduced. Therefore, it is desirable to optimize the loop bandwidth such that the PLL has sufficient noise reduction of both $1/f$ and $1/f^2$ noise.

As shown in Fig. 1(a), the crossover frequency is defined as ω_u, where these two PSDs intersect. It seems that an optimum phase noise spectrum can be achieved if ω_{u} is the –3 dB bandwidth for H_{L} and H_{H}. When $\omega < \omega_{\mathrm{u}}$, S_θ is dominated by $1/f^2$ noise; hence, by making $\omega_{-3\mathrm{dB,H}} = \omega_{\mathrm{u}}$, $1/f^2$ noise is suppressed heavily, and $1/f$ noise dominates; when $\omega > \omega_{\mathrm{u}}$, S_θ is dominated by $1/f$ noise; hence, by making $\omega_{-3\mathrm{dB,L}} = \omega_{\mathrm{u}}$, $1/f$ noise is suppressed heavily, and $1/f^2$ noise dominates. Combing the two results, an optimal phase noise spectrum S_θ is achieved, as shown in Fig. 1(d).

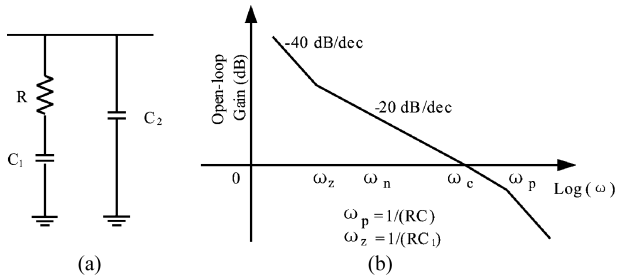

Fig. 2. (a) Low-pass filter component in a given PLL circuit topology; (b) Spectral property of the PLL open-loop transfer function based on a third-order loop. Here ω_{n} is the natural frequency, $\omega_{\mathrm{c}}$is the unity gain frequency, $\omega_c = \omega_{-3\mathrm{dB}}$, $\omega_{-3\mathrm{dB}}$ is the optimal loop bandwidth, which is derived from the previous analysis, and ω_z and ω_{p} is a zero and a pole of the open-loop transfer function.

In other words, the PLL system will attenuate the $1/f^2$ phase noise more at frequencies below ω_{u}, where they are greater than the $1/f$ phase noise. Conversely, it will attenuate the $1/f$ phase noise more at frequencies above ω_{u}, where they are greater than the $1/f^2$ phase noise. In this way, good jitter performance of the PLL is achieved.

3. Circuit parameter design

Compared with the traditional computational method based on a second-order model of PLL, a new method to design circuit parameters, on the basis of a third-order model, is proposed in this section. The values of the resistor or CP current are recalculated to achieve the optimal loop bandwidth more accurately through this method, improving noise performance of the PLL while maintaining good stability and locking speed.

For a third-order loop with a typical low-pass filter shown in Fig. 2(a), the open-loop transfer function can be expressed as

$$H(s)|_{\mathrm{open}} = I_{\mathrm{CP}}\frac{RC_1 s + 1}{RC_1C_2s^2 + (C_1 + C_2)s}\frac{K_{\mathrm{VCO}}}{s}\frac{1}{N},$$

where K_{VCO} is the VCO gain in Hz/V, and N is the frequency-dividing coefficient.

It has been shown in Ref. [7] that for a PLL with an arbitrary loop filter, the unity gain frequency of the resulting open-loop transfer function becomes the –3 dB bandwidth of the closed-loop transfer function. In order to acquire a larger phase margin, the spectral property of the PLL open-loop transfer function should be designed[8] as shown in Fig. 2(b).

According to the open-loop transfer function, the phase margin (PM) can be calculated as

$$\mathrm{PM} = (180/\pi)\left[\tan^{-1}(\omega_{\mathrm{c}}RC_1) - \tan^{-1}(\omega_{\mathrm{c}}RC)\right],$$

where $C = C_1C_2/C_1 + C_2$.

To eliminate peaking, equation $\omega_{\mathrm{c}}/\omega_z = 4$ is assumed, and the ratio of ω_{p} to ω_{c} can be easily written as $\omega_{\mathrm{p}}/\omega_{\mathrm{c}} =$

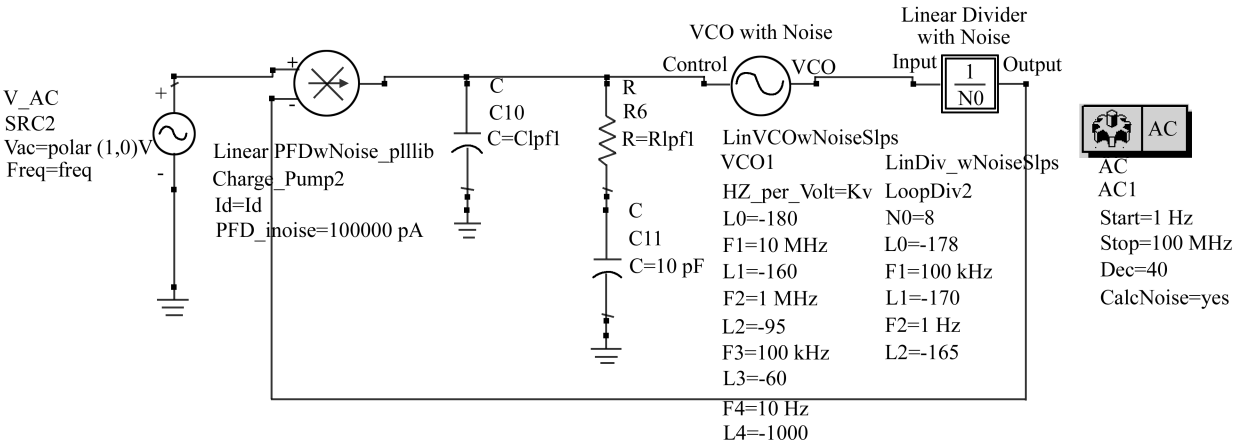

Fig. 3. A linear phase-domain behavioral model for a PLL with phase noise.

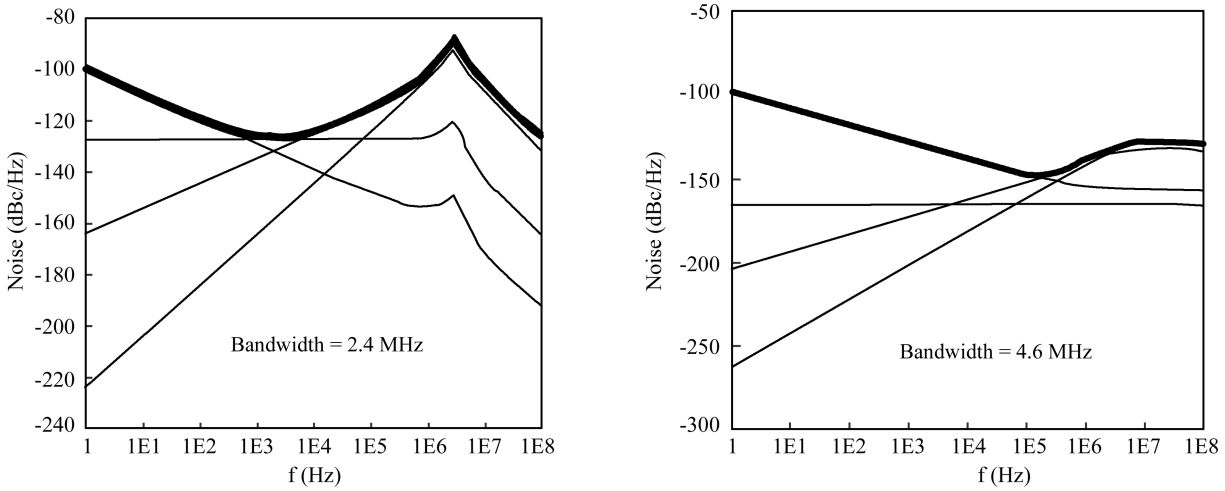

Fig. 4. Measured phase noise versus loop bandwidth of a 400-MHz phase-locked loop. The measured power spectral density of phase noise from previous noise sources at the optimum bandwidth (4.6 MHz) is compared with that at another loop bandwidth (2.4 MHz).

$[\tan(\tan^{-1}(4) - \mathrm{PM})]^{-1}$. Then, according to $\left|H(j\omega_c)|_{\mathrm{open}}\right| = 1$, C_2 can be solved from $C_2 = \dfrac{|I_{\mathrm{CP}}K_{\mathrm{VCO}}(j\omega_c + \omega_z)|}{|N(j\omega_c)^2(j\omega_c + \omega_p)|}$.

Knowing that $\omega_p/\omega_z = (C_1 + C_2)/C_1$ and $\omega_z = (RC_1)^{-1}$, the optimal value of R is obtained.

Alternatively, due to $\omega_p/\omega_z = (C_1 + C_2)/C_1$ and $\omega_z = (RC_1)^{-1}$, C_2 can be solved.

Finally, $I_{\mathrm{CP}} = \dfrac{|C_2N(j\omega_c)^2(j\omega_c + \omega_p)|}{|K_{\mathrm{VCO}}(j\omega_c + \omega_z)|}$, and thus the optimal value of I_{CP} is obtained.

In a word, the charge pump gain or the resistance in the loop filter can be adjusted for achieving the optimal jitter performance of PLL through this method.

4. Behavioral model for PLL

A linear phase-domain behavioral model for a PLL with phase noise in ADS is shown in Fig. 3. These models, including all the components in a PLL, such as PFD, CP, filter, VCO and frequency divider, are linear and analyzed easily in the frequency domain. Moreover, a feature of ADS allows especially simple modeling and measurement of phase noise. All the circuit parameters in this behavioral model are derived through the optimal loop-bandwidth design method, on the basis of actual circuit implementation. The noise power is extracted from transistor simulation.

The phase noise simulation was done by noise analysis in ADS. Figure 4 shows the simulated overall power spectral density of phase noise at different loop bandwidths. The loop bandwidth was varied from 2.4 to 4.6 MHz, which is the optimal loop bandwidth. The contribution of each noise source to the output phase noise can also be seen.

According to the simulation results, the overall phase noise of PLL is about –110 dBc/Hz at 100 kHz offset at the original loop bandwidth, and the overall phase noise at the optimal loop bandwidth is about –150 dBc/Hz at 100 kHz offset. Apparently, there was a 40 dBc improvement at 100 kHz offset in the phase noise power spectrum by choosing the optimal loop bandwidth.

5. Design examples

To verify the correctness of the PLL phase noise analysis, a CMOS 400MHz PLL with previous optimal circuit parameters was designed in a 0.18 μm CMOS process. Figure 5 shows the layout. Table 1 summarizes the simulated results of the phase-locked loop.

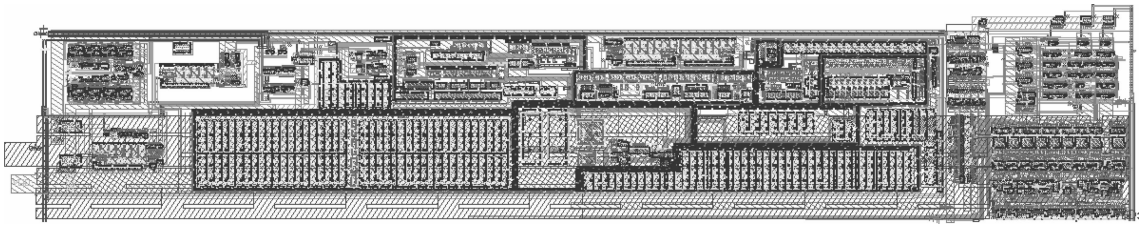

Fig. 5. Layout of a CMOS 400 MHz PLL in a 0.18 μm CMOS process.

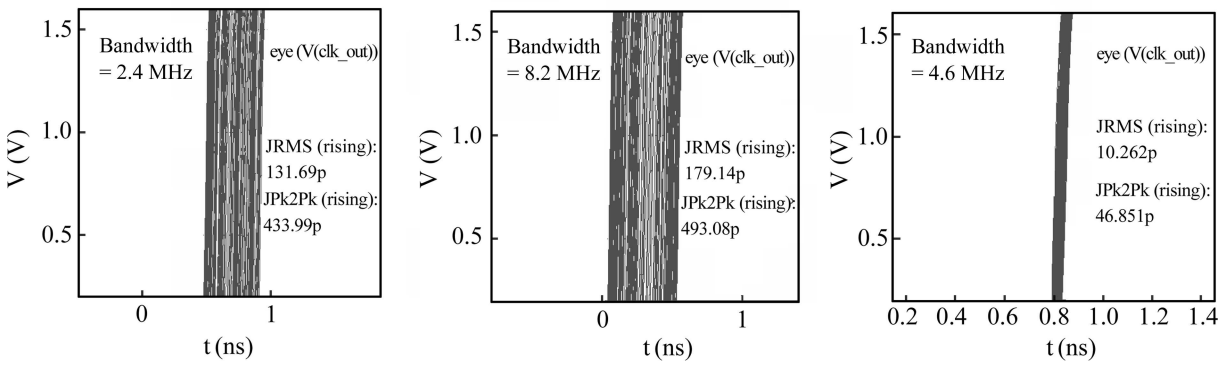

Fig. 6. Measured jitter versus loop bandwidth of a 400-MHz phase-locked loop. The measured jitter histogram at the optimum bandwidth (4.6MHz) is compared with those at loop bandwidths of 2.4 MHz and 8.2MHz.

Table 1. Summary of performance.

Parameter	Value
Technology	0.18 μm CMOS
Area	$923 \times 180\ \mu m^2$
Frequency range	200–600 MHz @ 1.8 V power supply
Output jitter	10.26 ps RMS 46.85 ps peak-to-peak @ 400 MHz
Output duty cycle	50.5%
Supply voltage	1.8 V

The jitter simulation supporting the phase noise analysis was done by Hspice. Figure 6 shows the simulated jitter at different loop bandwidths. The loop bandwidth was varied between 2.4, 8.2 and 4.6 MHz, which is the optimal loop bandwidth from the previous analysis.

According to the experimental results, the simulated RMS and peak-to-peak jitter of the PLL are 131.69 and 433.99 ps, respectively, at a loop bandwidth of 2.4 MHz; 179.14 and 493.08 ps, respectively, at 8.2 MHz; and 10.262 (0.0041UI) and 46.851 ps, respectively, at the optimal loop bandwidth. It is obvious that further improvements of the jitter characteristics can be achieved by choosing the optimum point for the loop bandwidth, with optimized PLL components. The simulation results are consistent with the theoretical estimation and behavioral simulation.

6. Conclusion

In this paper, an approach for the estimation of the RMS phase noise of a PLL output, taking into account five noise sources, is presented, along with behavioral PLL model simulations in ADS verifying the analysis. In various applications such as clock recovery and clock generation, the design of the optimal loop bandwidth with the best noise performance can be achieved by the proposed phase noise model. Jitter simulation by Hspice, using a charge-pump PLL in a 0.18 μm CMOS process, shows good agreement with the theoretical predictions.

References

[1] Razavi B. A study of phase noise in CMOS oscillators. IEEE J Solid-State Circuits, 1996, 31: 331

[2] Novof I, Austin J, Kelkar R, et al. Fully-integrated CMOS phase-locked loop with 15 to 40 MHz locking range and ± 50 ps jitter. ISSCC Dig Tech Papers, 1995: 112

[3] Maneatis J. Low-jitter process-independent DLL and PLL based on self-biased techniques. ISSCC Dig Tech Papers, 1996: 130

[4] Musa F A. Noise analysis of phase locked loops and system trade-offs. http://www-tcad.stanford.edu/tcad/pubs/theses/yizanglu.pdf

[5] He Jie. Research of integrated frequency synthesizer for digital video broadcasting (DVB-T) receiver. PhD Thesis, Fudan University, 2005: 45 (in Chinese)

[6] Hajimiri A, Lee T H. A general theory of phase noise in electrical oscillators. IEEE J Solid-State Circuits, 1998, 33(2): 179

[7] Egan W F. Frequency synthesis by phase lock. New York: Wiley-Inter Science, 1981: 40

[8] Fischette D. First time, every time practical tips for phase locked loop design. 2007: 12. http://www.delroy.com