Current mode ADC design in a 0.5-μm CMOS process

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Abstract: This paper presents a pipelined current mode analog to digital converter (ADC) designed in a 0.5-μm CMOS process. Adopting the global and local bias scheme, the number of interconnect signal lines is reduced numerously, and the ADC exhibits the advantages of scalability and portability. Without using linear capacitance, this ADC can be implemented in a standard digital CMOS process; thus, it is suitable for applications in the system on one chip (SoC) design as an analogue IP. Simulations show that the proposed current mode ADC can operate in a wide supply range from 3 to 7 V and a wide quantization range from ±64 to ±256 μA. Adopting the histogram testing method, the ADC was tested in a 3.3 V supply voltage/±64 μA quantization range and a 5 V supply voltage/±256 μA quantization range, respectively. The results reveal that this ADC achieves a spurious free dynamic range of 61.46 dB, DNL/INL are –0.005 to +0.027 LSB/–0.1 to +0.2 LSB, respectively, under a 5 V supply voltage with a digital error correction technique.

Key words: current mode; analog to digital converter; pipelined
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1. Introduction

With every passing CMOS process generation, the voltage swings for the signals and the power supply are decreasing, and the performance improvement under a low voltage is becoming more difficult[1, 2]. Facing this fact, there is renewed interest in the alternative current mode technique, which maintains performance even at low supply voltages. In current mode circuits, signals are represented by currents, which are insensitive to the voltage variation. Furthermore, no linear capacitance is needed; it is a suitable for digital CMOS processes since current mode circuits are composed only of MOSFETs and resistors. Thus, an IC implemented by using current mode technologies should be compact, and the cost of the ICs is reduced further. The current mode technology also provides a shortcut to the integration of whole systems on one chip (SoC) because the analog module can be realized in a standard digital CMOS process.

As interfaces of analog and digital modules in mixed signal systems, analog-to-digital converters (ADC) are very important and widely used. In many SoC applications, the ADCs are provided as intellectual property (IP) blocks. Compared to an IP, researchers pay more attention to the power dissipation, the chip area, and they are less concern with the reconfigurability, the scalability, and the portability of the analog modules into the SoC design. Usually for an SoC, the ADC is supplied as a core IP; for different supply voltages, the SoC topologies may be the same, but the ADC IP may be re-designed. Most of the present ADCs adopt a voltage mode operation and are sensitive to the variation of the supply voltage. This is equivalent to the case in the ADC IP. By adopting a current mode ADC (IADC) IP instead, this sensitivity to the supply voltage could be overcome due to the fact that the current mode technology is immune to supply voltage variations[3, 4].

This paper puts an emphasize on both versatility and expandability by presenting an 8-bit pipelined IADC, which operates with a 5 V supply voltage in a 0.5-μm CMOS technology. Implemented in the architecture of the global and local bias topology, the interconnection of the reference currents and the bias currents are minimized. An external reference current is added to the global current bias module, and then eight equal bias currents are generated and transmitted to the local bias current circuit in the succeeding stages, in order to serve as the local reference current. Then the local bias current generates various bias and reference currents needed in each stage. Thus, a large part of the interconnection is compressed in each stage cell, and the interconnection between the stages is greatly reduced. 80 bias currents are needed in the whole chip as estimated. If all these currents are provided by the bias circuits, there will be 80 current lines go across the chip, which makes the placement and the layout more complex, as shown in Fig. 1(a). If the proposed global and local bias scheme is adopted, the current lines across the whole chip will be reduced to eight lines and 10 lines in each stage cell for the applications, as shown in Fig. 1(b).

This paper also illustrates the architecture of the proposed IADC. The pipelined IADC consists of seven equal stages and one final flash stage. All these stages are explained in detail.

2. Pipelined IADC architecture

It is well known that the pipelined ADC structure is exactly an open-loop cyclic one. Most of the succeeding stages share the same structure except for the last one. Figure 2 illus-

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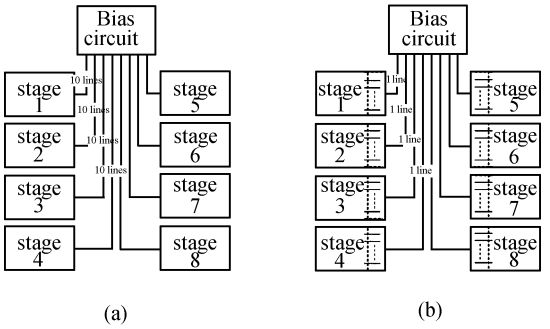


Fig. 1. Bias currents supply schemes: (a) Conventional scheme; (b) The proposed global and local scheme.

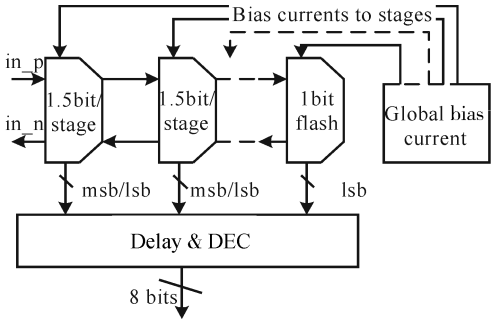


Fig. 2. Architecture of the proposed IADC.

trates the pipelined chain of the pipelined IADC architecture. The chain consists of seven 1.5 bit/stage cells and a 1 bit/stage flashed cell, and the IADC operates in a differential mode. The input current is applied directly to the input terminals, then sampled and compared to the reference currents, and the comparison result serves as the control signal for the MDAC, as well as the output msb/lsb of the stage. All the output digital bits are transmitted to the delay and digital error correction (DEC) circuits, which output the final eight digital codes.

3. Stage cell structure

All stages have the same structure except for the last stage, as shown in Fig. 3. The input signal $I_{\rm in}$ is injected from the left terminal, then sampled and held in the S & H cell, while, during the sampling period, the input signal is copied to the comparator to generate the output digital codes and to the common mode feedback (CMFB) circuit to eliminate the common mode error and to be doubled up. The comparison results control the MDAC and cause it to inject or to sink a current twice as large as the reference from the CMFB circuit during the hold mode. In addition, the output signal $I_{\rm out}$ is sampled as the input signal to the next stage.

3.1. Sample-and-hold and CMFB

The sample-and-hold circuit in each stage is composed out of a regulated class A current memory cell[5]. Figure 4 illustrates the sample-and-hold circuit, together with the CMFB; all transistors and bias currents are shown in the simple mode instead of the cascade configuration for simplicity. In this work, the sampling switch consists of an NMOSFET and

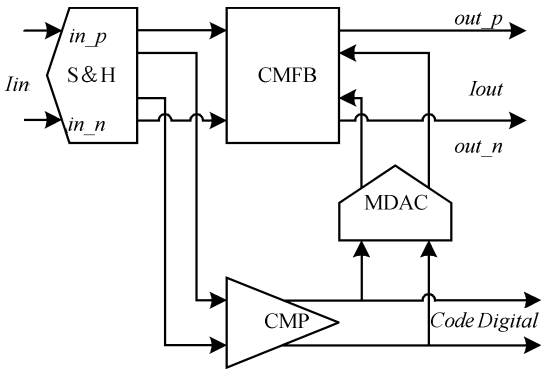


Fig. 3. Stage cell architecture.

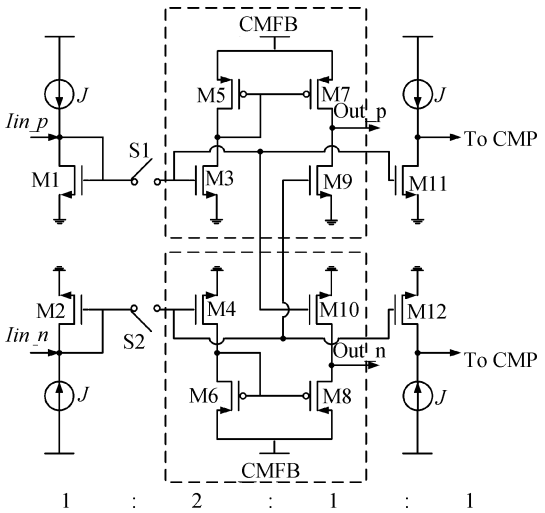


Fig. 4. Sample/hold and CMFB circuits.

dummy one for compensation. This configuration can maximize the operation speed, but the charge injection error and the clock feed-through cause a large error in the output current. To reduce the nonlinearity, the memory transistor is enlarged to provide a larger parasitic gate-source capacitance to minimize the injection charge error caused by the NMOS switch; and the differential operation mode also improves the linearity of the sample-and-hold circuit by extending the dynamic signal swings. In this way, the error current is considered to be quasi-signal-independent, and is eliminated by the CMFB.

For brevity, the upper half of the sample/hold circuit is taken as an example in the description of the sample/hold process. During the sampling period, the switch S1 closes, and a current mirror composed of M1, M3, and M11 is formed. The input current $I_{\rm in\_p}$ is injected into the transistor M1. Thus, the drain currents of M1, M3, and M11 can be expressed as

$$I_{\rm d1} = I_{\rm d3} = I_{\rm d11} = I_{\rm in\_p} + J\,. \tag{1}$$

While the drain current of M_9 is:

$$I_{\rm d9} = I_{\rm in\_n} + J\,. \tag{2}$$

M11 copies the input current $I_{\rm in\_p}$ and transmits it to the comparators to complete the current comparison. The current comparison is finished before the end of the sampling period. Thus, the performance of the M11 can not disturb the sample/hold block.

During the holding mode, the switch S1 opens and the gates of M3 and M11 keep floating. The charge in the gate source capacitor is sustained; thus, the input current $I_{\text{in\_p}}$ is held during the holding period. The operation of the switch S1 causes an injection error, and this error introduces a signal-dependent error current in the output signal. Notice that the gates of M1, M3, and M11 are connected together during the sampling period; thus, the injection error caused by S1 is distributed to these three transistors and reduces the error current in the memory transistor M3. The CMFB mechanism can also reduce the error current caused by the injection error of the switch.

Suppose the error current caused by S1 is i_{S1}, and the error current caused by S2 is i_{S2}, then the drain currents of M3 and M4 during the holding mode can be expressed as

$$\begin{cases} I_{\text{d3}} = I_{\text{d10}} = I_{\text{d11}} = I_{\text{in\_p}} + J + i_{\text{S1}}, \\ I_{\text{d4}} = I_{\text{d9}} = I_{\text{d12}} = I_{\text{in\_n}} + J + i_{\text{S2}}. \end{cases} \tag{3}$$

And the output currents at the node Out_p and Out_n are as follows:

$$\begin{cases} I_{\text{Out\_p}} = I_{\text{d3}} - I_{\text{d9}} = (I_{\text{in\_p}} - I_{\text{in\_n}}) - (i_{\text{S1}} - i_{\text{S2}}), \\ I_{\text{Out\_n}} = I_{\text{d4}} - I_{\text{d10}} = (I_{\text{in\_n}} - I_{\text{in\_p}}) - (i_{\text{S2}} - i_{\text{S1}}). \end{cases} \tag{4}$$

The input currents $I_{\text{in\_p}}$ and $I_{\text{in\_n}}$ are a couple of differential currents, and can be expressed as

$$\begin{cases} I_{\text{in\_p}} = I_{\text{offset}} + I_{\text{sig}}, \\ I_{\text{in\_n}} = I_{\text{offset}} - I_{\text{sig}}. \end{cases} \tag{5}$$

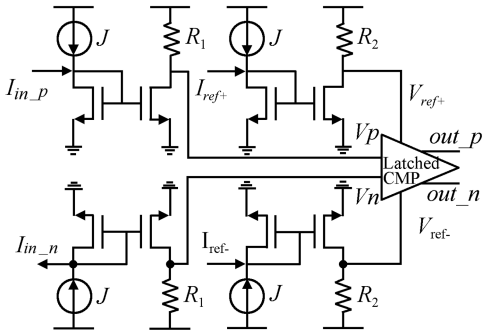
Substituting Eq. (5) into Eq. (4), Eq. (6) can be derived,

$$\begin{cases} I_{\text{Out\_p}} = 2I_{\text{sig}} - (i_{\text{S1}} - i_{\text{S2}}), \\ I_{\text{Out\_n}} = 2I_{\text{sig}} + (i_{\text{S2}} - i_{\text{S1}}). \end{cases} \tag{6}$$

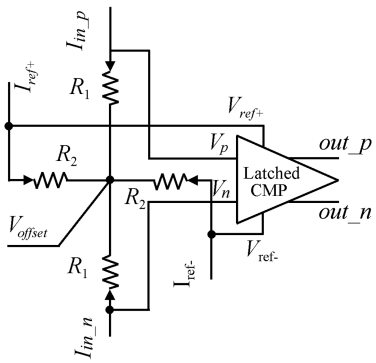
Compared to Eq. (5), the output current of the sample/hold circuit is amplified twice, and the error current caused by the switches S1 and S2 is partially reduced by $i_{\text{S1}} - i_{\text{S2}}$. During the design of the sample/hold circuit, we must ensure that the value of $i_{\text{S1}} - i_{\text{S2}}$ is less than 0.5 lsb. We notice that the DC offset current is removed in Eq. (6), and the output signal current of the sample/hold circuit should be coupled to a DC offset current I_{offset} before being injected into the next stage. In this design, a class AB operation is used, and the DC offset current is 0; thus, no coupling circuit is needed.

3.2. Differential current comparison scheme

Usually the current signal is converted into a voltage mode through a current mirror and a resistor before the comparison, as shown in Fig. 5(a). In this work, the ADC operates in a differential mode, and there should be four voltages generated by input signals and reference currents for comparison.



(a)



(b)

Fig. 5. Differential current comparison schemes: (a) Conventional comparison scheme; (b) The proposed scheme in this work.

For the comparator in Fig. 5(a), the input signals V_{p}, V_{n} and the references $V_{\text{ref+}}$, $V_{\text{ref-}}$ can be derived as

$$\begin{cases} V_{\text{p}} = V_{\text{dd}} - I_{\text{in\_p}} R_1, \\ V_{\text{n}} = V_{\text{dd}} - I_{\text{in\_n}} R_1, \\ V_{\text{ref+}} = V_{\text{dd}} - I_{\text{ref+}} R_2, \\ V_{\text{ref-}} = V_{\text{dd}} - I_{\text{ref-}} R_2. \end{cases} \tag{7}$$

One of the drawbacks of the scheme in Fig. 5(a) is that the direction of the input current is fixed, and for a bi-directional operation, a large bias current is needed, which increases the power dissipation. Another drawback is that the resistors R_1 and R_2 may be relatively large when considering the DC operation requirements of the differential comparator. For example, if a DC operation point of the differential voltage is $V_{\text{dd}}/2$, and the bias currents of the input branch and the reference branch are I_0 and I_{ref0}, respectively, then, according to Eq. (7), R_1 and R_2 should be $V_{\text{dd}}/2I_0$ and $V_{\text{dd}}/2I_{\text{ref0}}$, respectively. For this design, the supply voltage is 5 V, and the dynamic range is $\pm 512\ \mu$A; taking a modulation factor of 0.5, the bias current should be 256 μA. Then R_1 and R_2 are about 10 kΩ, and the resistors occupy a large area. Additionally, the dynamic range is also related to R_1, R_2, and I_{ref0}, I_0. Thus, there is a compromise between the bias currents and the resistors R_1, R_2, when the dynamic range and the DC operation node are considered.

The schematic shown in Fig. 5(b) overcomes the drawbacks mentioned above. The input voltages of the differential comparator can be expressed as

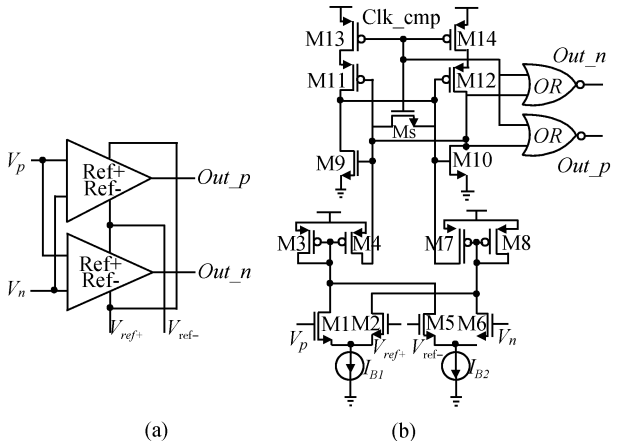


Fig. 6. Fully differential comparator: (a) Scheme of the differential comparator; (b) Comparator in (a).

$$\begin{cases} V_{\mathrm{p}} = V_{\mathrm{offset}} + I_{\mathrm{in\_p}} R_1, \\ V_{\mathrm{n}} = V_{\mathrm{offset}} - I_{\mathrm{in\_n}} R_1, \\ V_{\mathrm{ref+}} = V_{\mathrm{offset}} + I_{\mathrm{ref+}} R_2, \\ V_{\mathrm{ref-}} = V_{\mathrm{offset}} - I_{\mathrm{ref-}} R_2. \end{cases} \tag{8}$$

It is obvious that the input currents can be exchanged and there is no limitation on the directions of the current for both input and reference currents. Furthermore, no bias current is needed for the current branches. The offset voltage node is a floating node and can be set to any value by a voltage bias. Thus, the input DC operation nodes of the differential comparator is set to V_{offset}. In this work, a diode connected NMOS and a current source are used for the DC operation node set. Another advantage of this scheme is that the dynamic range and the DC operation node can be set, respectively, by using the V_{offset} to set the DC operation node, while the bias current I_0 and the resistor R_1 are used to define the dynamic range of the comparator.

3.3. Differential comparator and MDAC

The differential comparator used in this work is a conventional comparator, which consists of two voltage comparators, as shown in Fig. 6(a). The schematic of the voltage comparator is illustrated in Fig. 6(b). The voltage comparator is composed of two NMOS differential pairs and a dynamic latch, which is a common configuration for fully differential voltage comparison.

The output signals of the comparator not only present the results of the current comparison and generate the msb and the lsb for each stage, but they also control the operation of the MDAC to get proper input signals for the next stage circuit. The MDAC used in this work is illustrated in Fig. 7. It is a conventional structure in current steering DACs.

The high/low cross voltage latches represented as control modules in Fig. 7(a) are used to ensure a small voltage surge at the source coupling nodes of the MDAC. As shown in Fig. 7(b), the high cross voltage latch outputs a pair of complementary control signals, which cross at a relatively high voltage (4 V in this work). This high cross voltage guarantees that at least

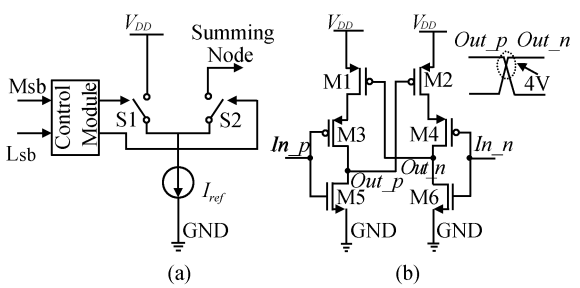


Fig. 7. MDAC: (a) Diagram of MDAC; (b) High/low cross latch.

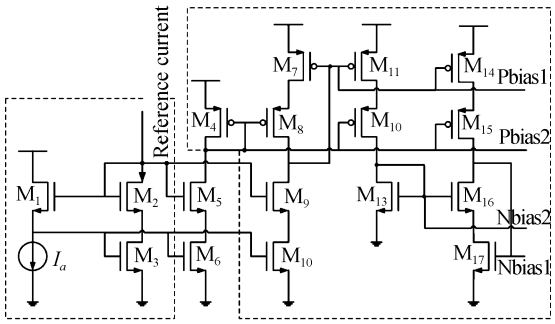


Fig. 8. Bias circuit.

one of the switches in Fig. 7(a) is always on; thus, a small surge is ensured.

3.4. Global and local bias current scheme

In a current mode circuit, a precise bias current circuit is needed because the signals and the references are in the current mode. In this paper, an external current is used as the global reference bias, and it generates bias currents as the references of the local bias circuit. A precise low voltage current mirror[6] together with a high swing current mirror make up both the global and the local bias circuits, as shown in Fig. 8. Considering the reusability, the bias circuits share the same structure and MOSFET size.

The global and local scheme for the bias current generation mainly focuses on the reduction of the process mismatch. Usually, the methods of DEM algorithms and some switching methodologies are popular in the current steering DACs design[7]. These methods build a basic current source array and connect the basic cells in a special manner to average the error caused by a possible process mismatch. However, the connections and interconnections are complex for all the current sources needed by different blocks, which are located in a specific area. It is difficult for designers to do the routing in a full-custom-manner. In the proposed global and local scheme, all the current sources are classified into two levels: the global bias currents, which provide the reference current to each stages, and the local bias currents, which generates current sources in the stage cells. Thus, the interconnections of the stages are minimized. In this design, there are nine interfaces (two analog inputs, two analog outputs, two digital outputs, two clock inputs, and one reference current input) in a standard stage cell, except for the former eight interfaces, which are necessary in any kind of configuration. The reduction of the interconnections to one reference current speeds up the

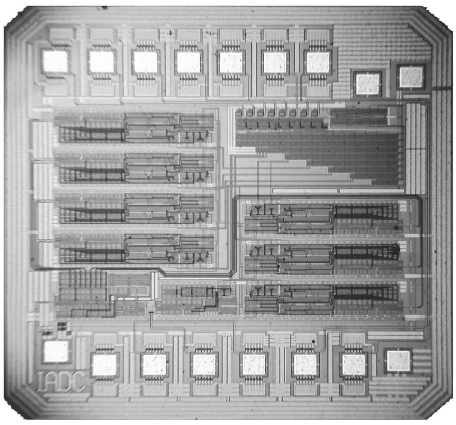


Fig. 9. Picture of the IADC.

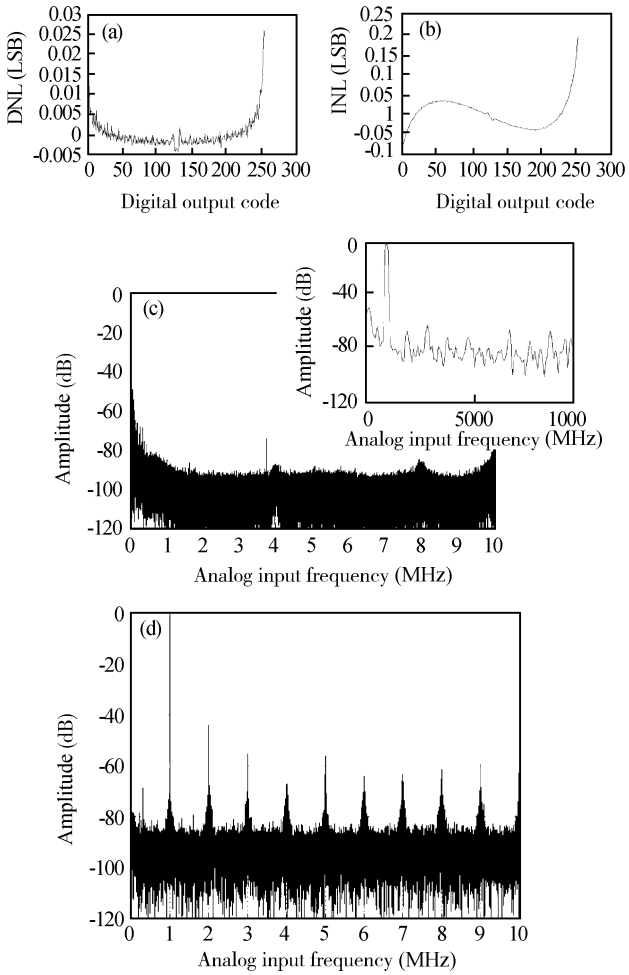


Fig. 10. Measurements of the IADC under 5 V: (a) DNL; (b) INL; (c) FFT plot (@ f_{in} = 1 kHz); (d) FFT plot (@ f_{in} = 1 MHz).

routing of the current mode circuits. Also, in the global and local bias circuits, the connection of the current sources follows the gradient switching method to minimize the gradient mismatch.

3.5. Delay and digital error correction circuit

In this work, a DEC method is utilized for better performance; thus, a delay array and a DEC circuit are necessary. The delay array is composed by a set of D-triggers, which are controlled by two complementary clocks and which realize a proper delay of the msb and lsb from each stage. The DEC circuit consists of several full adders. The adoption of the DEC circuit decreases the difficulties of the comparator design[8, 9].

Table 1. Performance of the IADC.

Parameter		Value	
Process		CSMC 0.5-μm CMOS	
Conversion rate		20 MSamples/s	
Core area (mm^2)		1.1 × 1.2	
Supply voltage		5 V	3.3 V
DNL (LSB)		–0.005/+0.027	–1.8/+1.8
INL (LSB)		–0.1/+0.2	–0.8/+1.2
Missing code		No	No
SFDR (dB)	f_{in} = 1 kHz	61.46	52.30
	f_{in} = 1 MHz	44.63	40.70
SNR (dB)	f_{in} = 1 kHz	42.60	42.22
	f_{in} = 1 MHz	41.02	40.25
SINAD (dB)	f_{in} = 1 kHz	42.40	37.92
	f_{in} = 1 MHz	39.22	37.80
Effective bits		6.8	6.1
THD (dB)		58.36	49.93
Power dissipation (mW)		375	69.3

3.6. Voltage to current converter

For a current mode signal, it cannot be realized that current signals are injected into the IADC directly through the bonding pad, because of the existence of a parasitic capacitance of the pad. A voltage to current converter is necessary for the IADC test, or the IADC is used as a discrete device in a system on board. In this design, a voltage to current converter, based on the structure in Ref. [10], is utilized. The SNR of the proposed VTC in this design is 61.8 dB, and this does not disturb the dynamic performance of an 8 bit ADC, whose ideal SNR is 49.92 dB.

4. Measurement and conclusion

The IADC proposed in this paper is designed in a 0.5-μm CMOS process. Its picture is shown in Fig. 9. The code density histogram measurement method is adopted for a static parameter test[11]. A differential sine signal is inputted into the ADC, and the output digital code of the IADC is collected through a logic analyzer. MATLAB is used for the data processing. Sampled at 20 M samples/s, the DNL and INL are within the range of –0.005 to +0.027 LSB, –0.1 to +0.2 LSB when using a 5 V power supply, respectively. For dynamic parameter measurements, an FFT analysis based on MATLAB is utilized. The measurements are illustrated in Fig. 10. Detailed performance parameters are listed in Table 1.

The SINAD of the IADC is relatively smaller, compared to the ideal value of 49.92 dB for 8 bits ADC; this is mainly caused by the signal source in this design. During the measurement of the IADC, an Agilent 33220A signal source is used. Its SNR of the output signal is only 44.6 dB (about 7.1 bits) and, thus, cannot fulfill the requirement that the source should be 2 bits higher than the resolution of the ADC under test. Also, the clock jitter and the jitter on the supply and on

the ground line will deteriorate the measurement. Moreover, the duty cycle of the clock generated by an active oscillator is about 48%, not 50%, and this also impacts the results of the dynamic parameters.

The SFDR, the SNR, and the SINAD are becoming worse when the input signal goes from 1 kHz up to 1 MHz. This is mainly because the noise level is higher in the input signals. In this test, the differential input signals are generated through a video amplifier (LM733) and coupled into the IADC by a capacitance. The test circuit is realized on a single layer PCB, which generates a relatively large noise, and degrades the quality of the input signals. Also, the DIP package of the IADC and IC sockets on the PCB cause noise coupling.

The IADC in this paper can operate in a wide supply voltage range (3 to 7 V), and retains an ordinary performance. A lower voltage (below 1 V) is expected in a future work through the adoption of some advanced technologies. The measurements reveal that the current mode technique can be used in high performance analog circuit design. The structure of the IADC is simplified further. The current mode circuit is an alternative to the traditional voltage mode design techniques for a smaller area, a lower cost and a better compatibility with the digital process.

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